RJK0456DPB

40V, 50A, 3.2mΩ max.
Silicon N Channel Power MOS FET
Power Switching

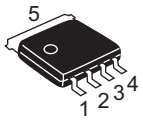
R07DS1051EJ0300
(Previous: REJ03G1879-0200)
Rev.3.00
Apr 09, 2013

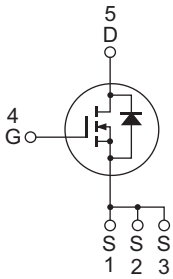
Features

- High speed switching
- Low drive current
- Low on-resistance
  $R_{DS(on)}$ = 2.6 mΩ typ. (at V_{GS} = 10 V)
- Pb-free
- Halogen-free
- High density mounting

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)





1, 2, 3	Source
4	Gate
5	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$ Note1	200	A
Body-drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP} Note 2	50	A
Avalanche energy	E_{AS} Note 2	20	mJ
Channel dissipation	Pch Note3	65	W
Channel to Case Thermal Resistance	θch-C	1.92	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at L=10uH, Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

Electrical Characteristics

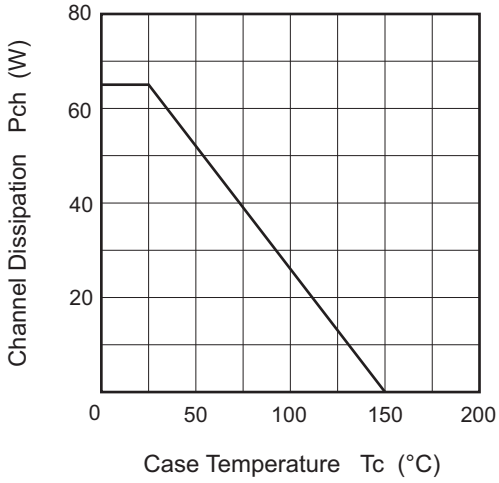
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	I_D = 10 mA, V_{GS} = 0 V
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	2.6	3.2	mΩ	I_D = 25 A, V_{GS} = 10 V Note4
Forward transfer admittance	$\|y_{fs}\|$	—	67	—	S	I_D = 25 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	3000	—	pF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz
Output capacitance	Coss	—	900	—	pF	
Reverse transfer capacitance	Crss	—	260	—	pF	
Gate Resistance	Rg	—	0.5	—	Ω	
Total gate charge	Qg	—	39	—	nC	V_{DD} = 10 V, V_{GS} = 10 V, I_D = 50 A
Gate to source charge	Qgs	—	13	—	nC	
Gate to drain charge	Qgd	—	6.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	V_{GS} = 10 V, I_D = 25 A, V_{DD} ≅ 10 V, R_L = 0.4 Ω, Rg = 4.7 Ω
Rise time	t_r	—	6.8	—	ns	
Turn-off delay time	$t_{d(off)}$	—	34	—	ns	
Fall time	t_f	—	8.0	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.8	1.1	V	I_F = 50 A, V_{GS} = 0 V Note4
Body–drain diode reverse recovery time	t_{rr}	—	41	—	ns	I_F = 50 A, V_{GS} = 0 V di_F/dt = 100 A/μs

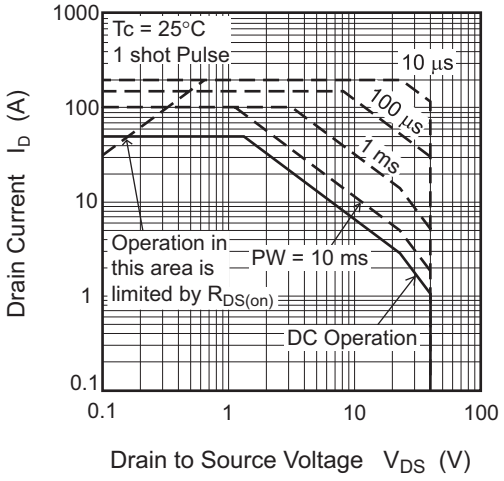
Notes: 4. Pulse test

Main Characteristics

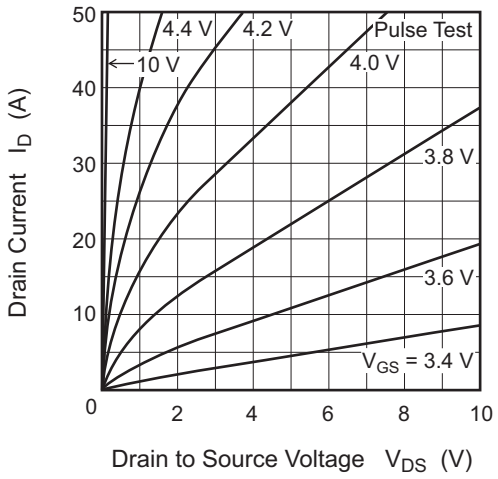
Power vs. Temperature Derating



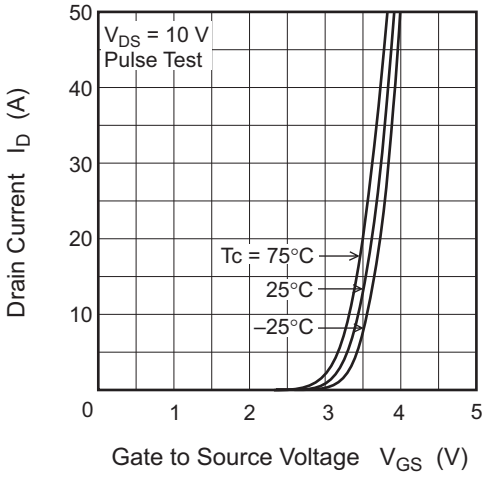
Maximum Safe Operation Area



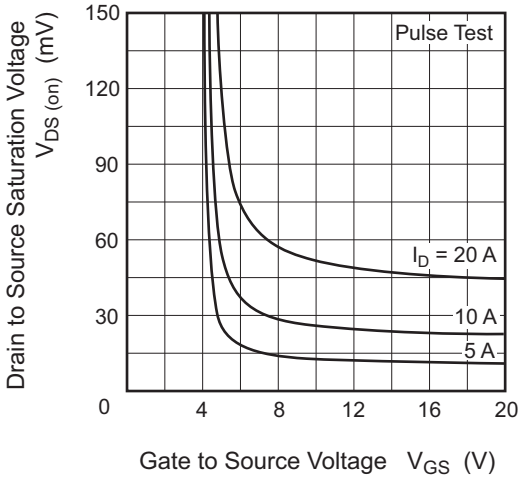
Typical Output Characteristics



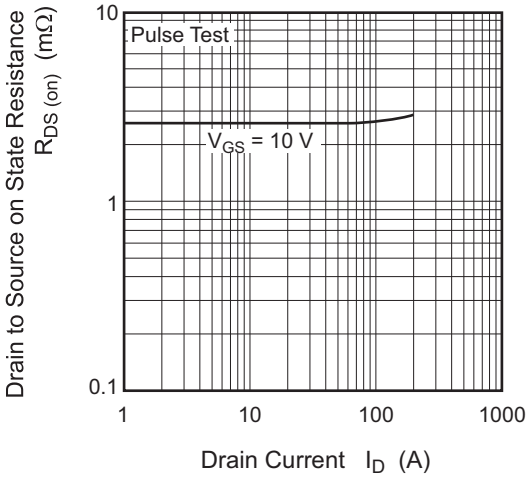
Typical Transfer Characteristics



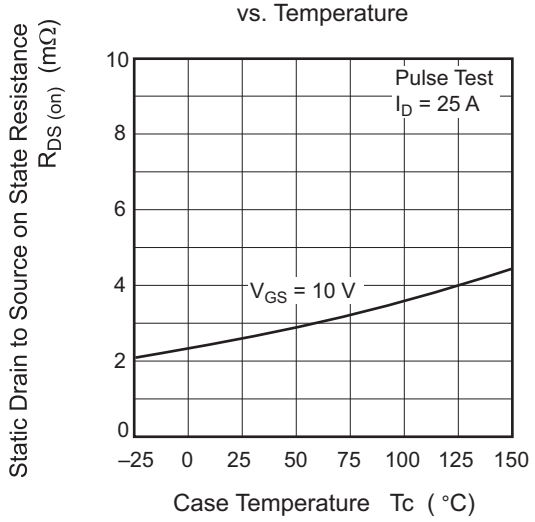
Drain to Source Saturation Voltage vs. Gate to Source Voltage



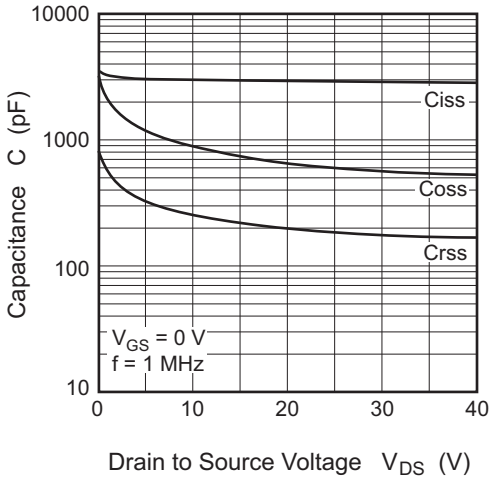
Static Drain to Source on State Resistance vs. Drain Current



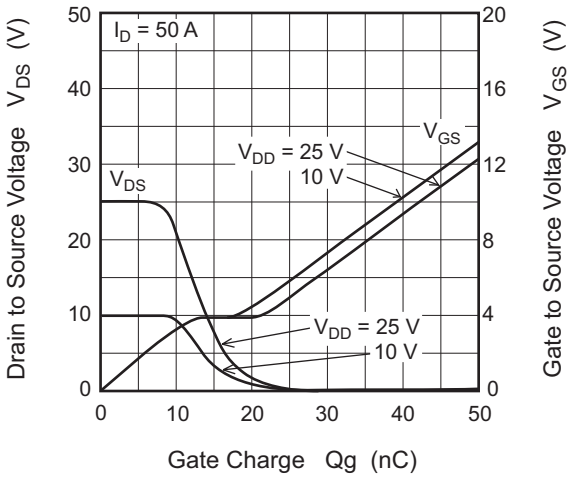
Static Drain to Source on State Resistance vs. Temperature



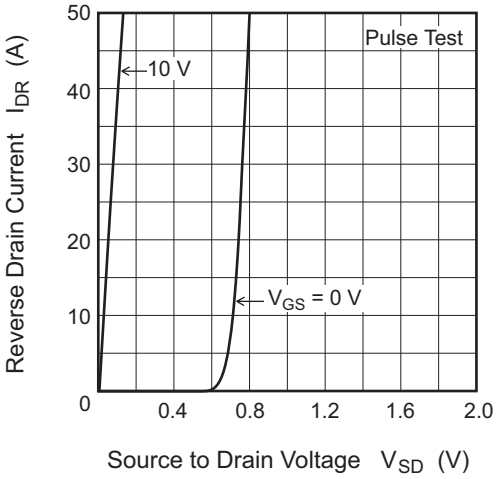
Typical Capacitance vs. Drain to Source Voltage



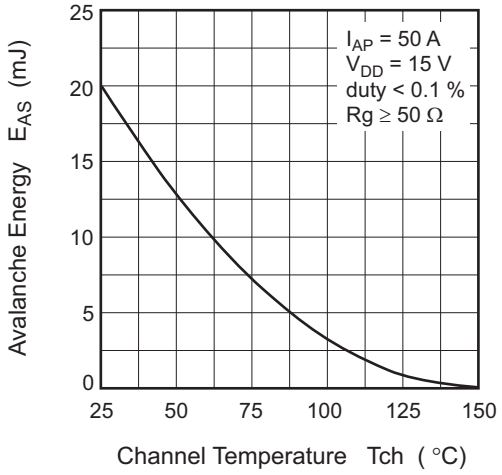
Dynamic Input Characteristics



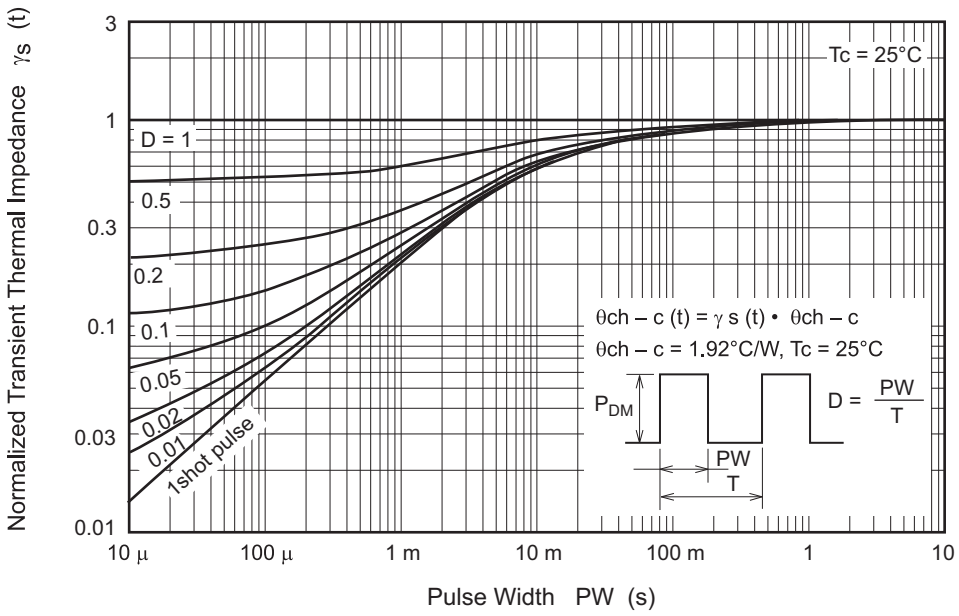
Reverse Drain Current vs. Source to Drain Voltage



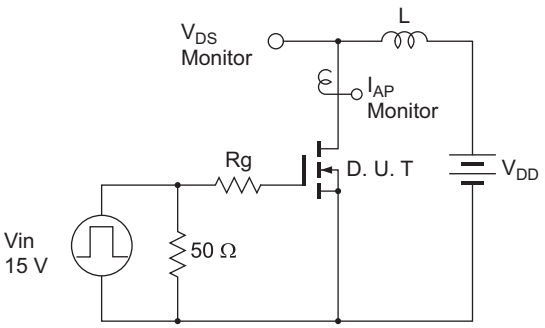
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

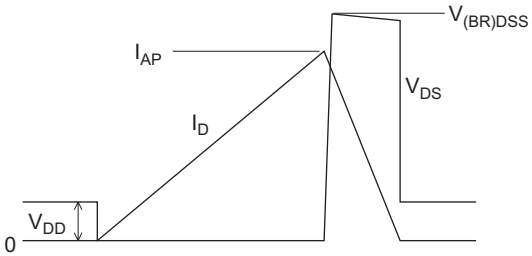


Avalanche Test Circuit

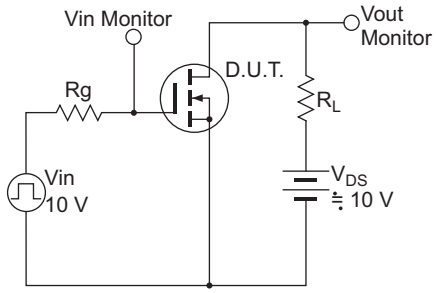


Avalanche Waveform

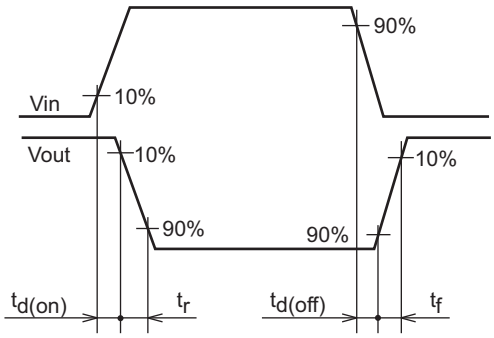
$$E_{AS} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



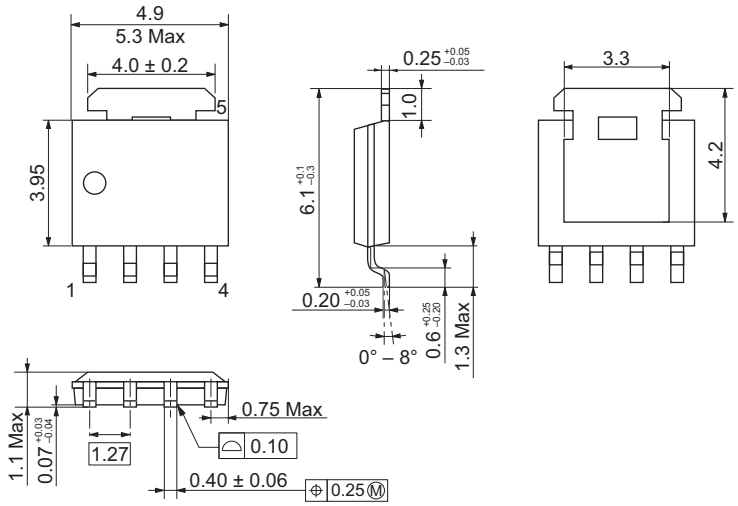
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LFPAK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part No.	Quantity	Shipping Container
RJK0456DPB-00-J5	2500 pcs	Taping

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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