*RP105Q (SC-88A) is the discontinued product as of April, 2018.

NISSHINBO

RP105x Series

Low Voltage 400 mA LDO Regulator

No. EA-179-221027

OUTLINE

The RP105x is a 400 mA output type CMOS-based voltage regulator with capability of low input voltage (Min. 0.9 V) and low output voltage (Min. 0.6 V). This device is remarkably improved the performance at low input voltage compared with conventional low voltage LDOs, and two power supply voltage type. (Another power source, V_{BIAS} pin voltage must be Min. 2.4 V). The device consists of a voltage reference unit, an error amplifier, resistor-net for voltage setting, a current limit circuit to avoid the destruction, a UVLO circuit with monitoring input voltage, and so on.
The RP105x has the ultra-low on resistance output driver, the on resistance is Typ. 0.4 Ω (V_{OUT} = 0.8 V, I_{OUT} = 300 mA). The built-in driver is Nch MOSFET, thus the load transient response is excellent, (under the condition of the current between 1 mA and 400 mA, tr = 0.5 μs, the undershoot level is approximately 50 mV).
The output voltage of this device is fixed with high accuracy. Since the packages for the device are DFN(PL)1212-6, DFN1212-5, SOT-23-5 and SC-88A therefore high density mounting of the IC on boards is possible.

FEATURES

- Supply Current ..... Typ. 28 μA
- Standby Current ..... Typ. 0.1 μA
- Ripple Rejection ..... Typ. 80 dB (f = 1 kHz, V_{IN} Ripple)
  Typ. 50 dB (f = 1 kHz, V_{BIAS} Ripple)
- Output Voltage Range ..... 0.6 V to 1.5 V (0.1 V step)
  For other voltages, refer to *MARKING SPECIFICATION*
- Input Voltage Range (V_{BIAS}) ..... 2.4 V to 5.25 V (V_{OUT} < 0.8 V)
  Set V_{OUT} + 1.6 V to 5.25 V (V_{OUT} ≥ 0.8 V)
- Input Voltage Range (V_{IN}) ..... RP105xxxxB/D: 0.9 V to V_{BIAS} (V_{OUT} < 0.8 V)
  Set V_{OUT} + 0.1 V to V_{BIAS} (V_{OUT} ≥ 0.8 V)
  RP105xxxxE/F: 0.9 V to V_{BIAS}
- Output Voltage Accuracy ..... Typ. ±15 mV (Ta = 25°C)
- Temperature-Drift Coefficient of Output Voltage ..... Typ. ±50 ppm/°C
- Dropout Voltage ..... DFN1212-5: Typ. 105 mV
  (I_{OUT} = 400 mA, V_{OUT} = 1.5 V, V_{BIAS} = 3.6 V)
- Line Regulation ..... Typ. 0.02%/V
- Packages ..... DFN(PL)1212-6, SC-88A, SOT-23-5, DFN1212-5
- Built-in Fold Back Protection Circuit ..... Typ. 120 mA (Current at short mode)
- Ceramic capacitors are recommended ..... C_{BIAS} = C_{IN} = 1.0 μF or more, C_{OUT} = 2.2 μF or more

APPLICATIONS

- Power source for battery-powered equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for portable communication equipment.

No. EA-179-221027

SELECTION GUIDE

The output voltage, the UVLO circuit, the auto-discharge function(1), the package, and the taping type for the device are user-selectable options.

Selection Guide

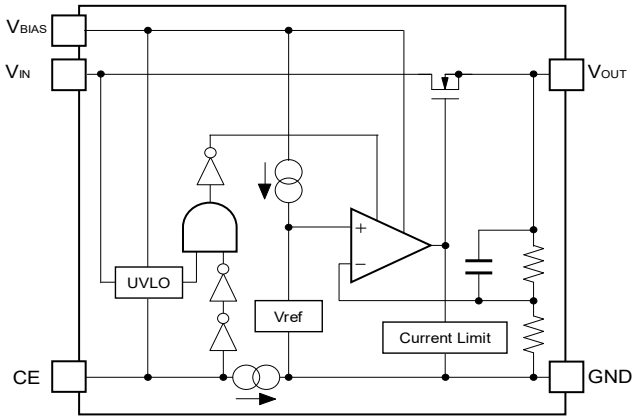
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP105Kxx1∗-TR	DFN(PL)1212-6	5,000 pcs	Yes	Yes
RP105Qxx2∗-TR-FE (2)	SC-88A	3,000 pcs	Yes	Yes
RP105Nxx1∗-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes
RP105Lxx1∗-TR	DFN1212-5	5,000 pcs	Yes	Yes

xx : The set output voltage (V_{SET}) can be designated within the range of 0.6 V (06) to 1.5 V (15) in 0.1 V step.

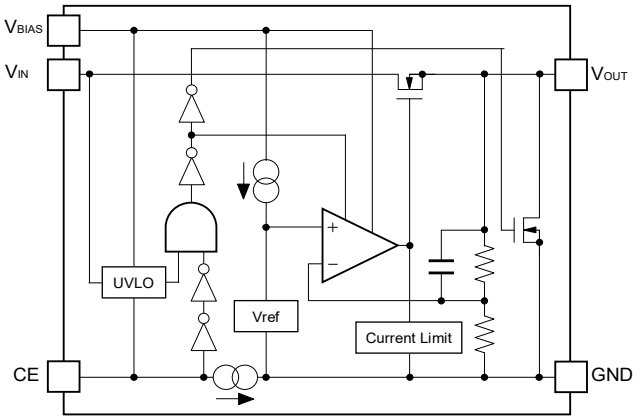
If the set output voltage (V_{SET}) is designated in 0.01 V step, indicate the product name as follows.
1.05 V: RP105x10x∗5-TR

∗ : CE pin polarity and auto-discharge function of the product can be defined as follows.
(B) "H" active, auto-discharge function is not included, UVLO is included
(D) "H" active, auto-discharge function is included, UVLO is included
(E) "H" active, auto-discharge function is not included, UVLO is not included
(F) "H" active, auto-discharge function is included, UVLO is not included

BLOCK DIAGRAMS



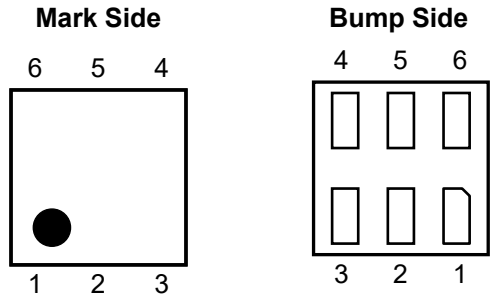
RP105xxxxB/E Block Diagram



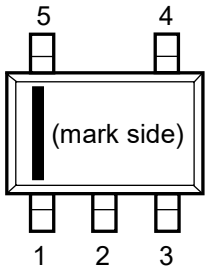
RP105xxxxD/F Block Diagram

(1) Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.
(2) RP105Qxx2∗-TR-FE supports only RP105Qxx2B/D.

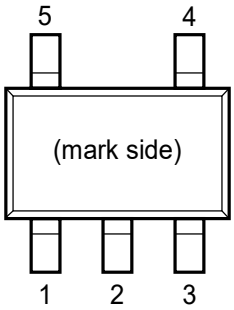
PIN DESCRIPTIONS



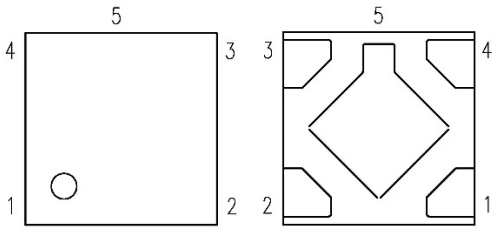
DFN(PL)1212-6 Pin Configuration



SC-88A
Pin Configuration



SOT-23-5
Pin Configuration



DFN1212-5 Pin Configuration

DFN(PL)1212-6 Pin Description

Pin No	Symbol	Pin Description
1	V_{BIAS}	Input Pin 1
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	V_{IN}	Input Pin 2
5	NC	No Connection
6	V_{OUT}	Output Pin

SC-88A Pin Description

Pin No	Symbol	Pin Description
1	V_{BIAS}	Input Pin 1
2	GND	Ground Pin
3	V_{OUT}	Output Pin
4	V_{IN}	Input Pin 2
5	CE	Chip Enable Pin ("H" Active)

SOT-23-5 Pin Description

Pin No	Symbol	Pin Description
1	V_{IN}	Input Pin 2
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	V_{BIAS}	Input Pin 1
5	V_{OUT}	Output Pin

DFN1212-5 Pin Description

Pin No	Symbol	Pin Description
1	V_{OUT}	Output Pin
2	V_{BIAS}	Input Pin 1
3	CE	Chip Enable Pin ("H" Active)
4	V_{IN}	Input Pin 2
5	GND	Ground Pin

ABSOLUTE MAXIMUM RATINGS

Aboslute Maximum Ratings

Symbol	Item			Rating	Unit
V_{BIAS}	Input Voltage			6.0	V
V_{IN}	Input Voltage (for Driver)			−0.3 to V_{BIAS} + 0.3	V
V_{CE}	Input Voltage (CE Pin)			6.0	V
V_{OUT}	Output Voltage			−0.3 to V_{IN} + 0.3	V
I_{OUT}	Output Current			500	mA
P_D	Power Dissipation(1)	DFN(PL)1212-6	JEDEC STD. 51-7 Test Land Pattern	450	mW
		SC-88A	Standard Test Land Pattern	380	
		SOT-23-5	JEDEC STD. 51-7 Test Land Pattern	660	
		DFN1212-5	JEDEC STD. 51-7 Test Land Pattern	560	
Tj	Junction Temperature Range			−40 to 125	°C
Tstg	Storage Temperature Range			−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{BIAS}	Input Voltage Range	2.4 to 5.25	V
V_{IN}		0.9 to V_{BIAS}	V
		V_{SET} + 0.1 to V_{BIAS} (RP105xxxxB/D and when V_{SET} ≥ 0.8 V)	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = V_{CE} = 3.6 V, V_{IN} = Set V_{OUT} + 0.5 V, I_{OUT} = 1 mA, C_{BIAS} = C_{IN} = 1.0 µF, C_{OUT} = 2.2 µF, unless otherwise noted.
The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP105x (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta = 25°C	Set V_{OUT} −15 mV		Set V_{OUT} + 15 mV	V
		−40°C ≤ Ta ≤ 85°C	Set V_{OUT} −20 mV		Set V_{OUT} + 20 mV	V
I_{OUT}	Output Current		400			mA
ΔV_{OUT} /ΔI_{OUT}	Load Regulation (K, Q, N package)	1 mA ≤ I_{OUT} ≤ 400 mA		30	50	mV
	Load Regulation (L package)	1 mA ≤ I_{OUT} ≤ 400 mA		15	35	mV
V_{DIF}	Dropout Voltage	Refer to *PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS*				
I_{SS}	Supply Current	I_{OUT} = 0 mA		28	40	µA
Istandby	Standby Current	V_{CE} = 0 V		0.1	3.0	µA
ΔV_{OUT} /ΔV_{IN}	Line Regulation	2.4 V ≤ V_{BIAS} ≤ 5.0 V		0.02	0.1	%/V
		Set V_{OUT} + 0.3 V ≤ V_{IN} ≤ 2.4 V		0.02	0.1	
RR	Ripple Rejection	I_{OUT} = 30 mA, f = 1 kHz V_{IN} Ripple 0.2 Vp-p		80		dB
		I_{OUT} = 30 mA, f = 1 kHz V_{BIAS} Ripple 0.2 Vp-p		50		
V_{BIAS}	Input Voltage(1)	V_{OUT} < 0.8 V	2.4		5.25	V
		V_{OUT} ≥ 0.8 V	Set V_{OUT} + 1.6		5.25	
V_{IN}	Input Voltage (for Driver)(1)	RP105xxxxB/D, V_{OUT} < 0.8 V	0.9		V_{BIAS}	V
		RP105xxxxB/D, V_{OUT} ≥ 0.8 V	Set V_{OUT} + 0.1		V_{BIAS}	
		RP105xxxxE/F	0.9		V_{BIAS}	
ΔV_{OUT} /ΔTa	Output Voltage Temperature Coefficient	−40°C ≤ Ta ≤ 85°C		±50		ppm /°C
I_{SC}	Short Current Limit	V_{OUT} = 0 V		120		mA
I_{CEPD}	CE Pull-down Current			1.0		µA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient.

(1) The maximum Input Voltage listed under Electrical Characteristics is 5.25 V. If for any reason the input voltage exceeds 5.25 V, it has to be no more than 5.5 V with 500 hours of the total operating time.

ELECTRICAL CHARACTERISTICS (continued)

V_{BIAS} = V_{CE} = 3.6 V, V_{IN} = Set V_{OUT} + 0.5 V, I_{OUT} = 1 mA, C_{BIAS} = C_{IN} = 1.0 µF, C_{OUT} = 2.2 µF, unless otherwise noted.
The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP105x (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{CEH}	CE Input Voltage "H"		0.8			V
V_{CEL}	CE Input Voltage "L"				0.3	V
$V_{IN\ UVLO}$	V_{IN} Under Voltage Lock Out (only RP105xxxxB/D)	I_{OUT} = 1.0 µA		Set V_{OUT} + 50 mV	Set V_{OUT} + 100 mV	V
tdelay	Detector Delay Time (only RP105xxxxB/D)			100		µs
en	Output Noise	BM = 10 Hz to 100 kHz I_{OUT} = 30 mA, Set V_{OUT} = 0.6 V		70		µVrms
R_{LOW}	Nch On Resistance For auto-discharge (only RP105xxxxD/F)	V_{BIAS} = 3.6 V, V_{CE} = "L"		50		Ω

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient.

PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS

DFN(PL)1212-6, SC-88A, SOT-23-5

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C

Dropout Voltage

Set V_{OUT} (V)	V_{BIAS} (V)	V_{GS} (V)	V_{DIF} (I_{OUT} = 300 mA) (V)		V_{DIF} (I_{OUT} = 400 mA) (V)	
			Typ.	Max.	Typ.	Max.
0.6	3.6	3.0	0.115	0.180	0.180	0.320
0.7	3.6	2.9	0.120	0.190	0.180	0.320
0.8	3.6	2.8	0.120	0.190	0.180	0.300
0.9	3.6	2.7	0.120	0.190	0.180	0.300
1.0	3.6	2.6	0.120	0.190	0.180	0.280
1.1	3.6	2.5	0.120	0.190	0.180	0.280
1.2	3.6	2.4	0.130	0.200	0.180	0.280
1.3	3.6	2.3	0.130	0.200	0.180	0.260
1.4	3.6	2.2	0.130	0.200	0.180	0.260
1.5	3.6	2.1	0.130	0.200	0.180	0.260

Dropout Voltage (V_{GS} (V), V_{DIF} (V), I_{OUT} = 200 mA) (Ta = 25°C)

Set V_{OUT} (V)	V_{BIAS} = 2.5 V		V_{BIAS} = 3.0 V		V_{BIAS} = 3.3 V		V_{BIAS} = 3.6 V		V_{BIAS} = 4.2 V		V_{BIAS} = 5.0 V	
	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)
0.6	1.9	-	2.4	-	2.7	-	3.0	-	3.6	-	4.4	-
0.7	1.8	-	2.3	-	2.6	-	2.9	-	3.5	-	4.3	-
0.8	1.7	0.098	2.2	0.093	2.5	0.093	2.8	0.092	3.4	0.092	4.2	0.092
0.9	1.6	0.098	2.1	0.094	2.4	0.093	2.7	0.092	3.3	0.092	4.1	0.092
1.0	⧅	⧅	2.0	0.094	2.3	0.093	2.6	0.092	3.2	0.092	4.0	0.092
1.1	⧅	⧅	1.9	0.096	2.2	0.094	2.5	0.094	3.1	0.093	3.9	0.093
1.2	⧅	⧅	1.8	0.098	2.1	0.096	2.4	0.095	3.0	0.095	3.8	0.094
1.3	⧅	⧅	1.7	0.098	2.0	0.096	2.3	0.095	2.9	0.095	3.7	0.095
1.4	⧅	⧅	1.6	0.098	1.9	0.096	2.2	0.095	2.8	0.095	3.6	0.095
1.5	⧅	⧅	⧅	⧅	1.8	0.096	2.1	0.095	2.7	0.095	3.5	0.095

All of units are tested and specified under load conditions such that Tj ≈ Ta = 25°C except for Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient items.

⧅ V_{BIAS} pin voltage must be equal or more than Set V_{OUT} + 1.6 V.

DFN1212-5

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C

Dropout Voltage

Set V_{OUT} (V)	V_{BIAS} (V)	V_{GS} (V)	V_{DIF} (I_{OUT} = 300 mA) (V)		V_{DIF} (I_{OUT} = 400 mA) (V)	
			Typ.	Max.	Typ.	Max.
0.6	3.6	3.0	-	-	-	-
0.7	3.6	2.9	-	-	-	-
0.75	3.6	2.85	-	-	-	0.170
0.8	3.6	2.8	0.077	0.130	0.105	0.170
0.9	3.6	2.7	0.077	0.130	0.105	0.170
0.95	3.6	2.65	0.077	0.130	0.105	0.170
1.0	3.6	2.6	0.077	0.130	0.105	0.170
1.05	3.6	2.55	0.077	0.130	0.105	0.170
1.1	3.6	2.5	0.077	0.130	0.105	0.170
1.2	3.6	2.4	0.077	0.130	0.105	0.170
1.3	3.6	2.3	0.077	0.130	0.105	0.170
1.4	3.6	2.2	0.077	0.130	0.105	0.170
1.5	3.6	2.1	0.077	0.130	0.105	0.170

Dropout Voltage (V_{GS} (V), V_{DIF} (V), I_{OUT} = 200 mA) (Ta = 25°C)

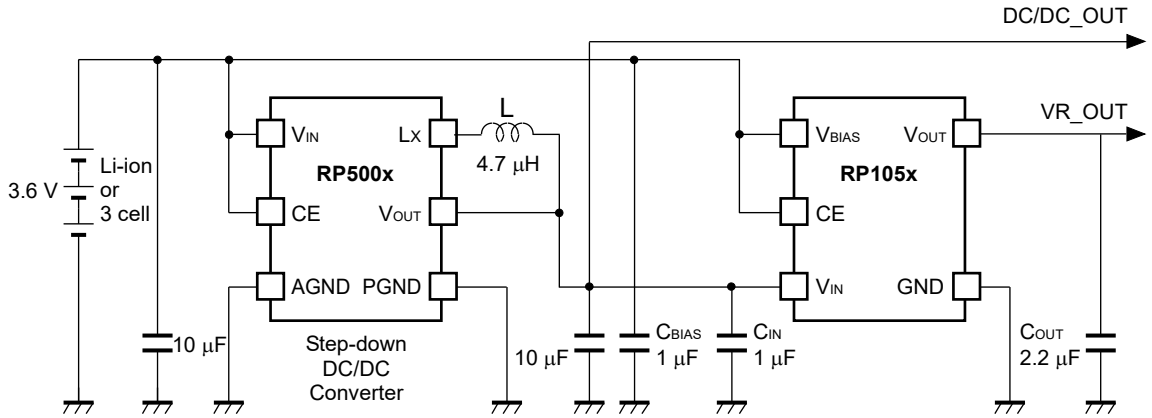
Set V_{OUT} (V)	V_{BIAS} = 2.5 V		V_{BIAS} = 3.0 V		V_{BIAS} = 3.3 V		V_{BIAS} = 3.6 V		V_{BIAS} = 4.2 V		V_{BIAS} = 5.0 V	
	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)
0.6	1.9	-	2.4	-	2.7	-	3.0	-	3.6	-	4.4	-
0.7	1.8	-	2.3	-	2.6	-	2.9	-	3.5	-	4.3	-
0.75	1.75	-	2.25	-	2.55	-	2.85	-	3.45	-	4.25	-
0.8	1.7	-	2.2	-	2.5	-	2.8	-	3.4	-	4.2	-
0.9	1.6	0.059	2.1	0.054	2.4	0.053	2.7	0.051	3.3	0.050	4.1	0.048
0.95			2.05	0.054	2.35	0.053	2.65	0.051	3.25	0.050	4.05	0.048
1.0			2.0	0.054	2.3	0.053	2.6	0.051	3.2	0.050	4.0	0.048
1.05			1.95	0.054	2.25	0.053	2.55	0.051	3.15	0.050	3.95	0.048
1.1			1.9	0.054	2.2	0.053	2.5	0.051	3.1	0.050	3.9	0.048
1.2			1.8	0.054	2.1	0.053	2.4	0.051	3.0	0.050	3.8	0.048
1.3			1.7	0.054	2.0	0.053	2.3	0.051	2.9	0.050	3.7	0.048
1.4			1.6	0.054	1.9	0.053	2.2	0.051	2.8	0.050	3.6	0.048
1.5					1.8	0.053	2.1	0.051	2.7	0.050	3.5	0.048

All of units are tested and specified under load conditions such that Tj ≈ Ta = 25°C except for Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient items.

▨ V_{BIAS} pin voltage must be equal or more than Set V_{OUT} + 1.6 V.

APPLICATION INFORMATION

TYPICAL APPLICATION



External Components

Symbol	Descriptions
C_{OUT}	2.2 µF, Ceramic Capacitor, GRM155B30J225ME15, MURATA
C_{BIAS}, C_{IN}	1.0 µF, Ceramic Capacitor, GRM155B31A105KE15, MURATA

TECHNICAL NOTES

UVLO (Undervoltage Lockout)

In RP105xxxxB/D, UVLO detects and turns off the output when the input voltage V_{IN} drops lower than or equal to V_{SET} + 50 mV (Typ.) while CE = “H”. Since RP105xxxxE/F does not have UVLO, it continues to output even if V_{IN} drops to V_{SET} + 50 mV (Typ.) or lower.

When V_{IN} drops below the set output voltage V_{SET}, UVLO does not turn off the output in RP105xxxxE/F while CE = “H”, therefore the current flows from V_{BIAS} pin to V_{IN} pin via the inside IC. This will not be generated in RP105xxxxB/D since UVLO turns off the output when V_{IN} is lower than or equal to V_{SET} + 50 mV (Typ).

Phase Compensation

In this device, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor for C_{OUT} with the capacity of equal or more than 2.2 μF.
If tantalum capacitors are connected as C_{OUT}, and if the equivalent series resistance (ESR) value is large, the operation might be unstable. Because of this, test the device with as same external components as ones to be used on the PCB.

PCB Layout

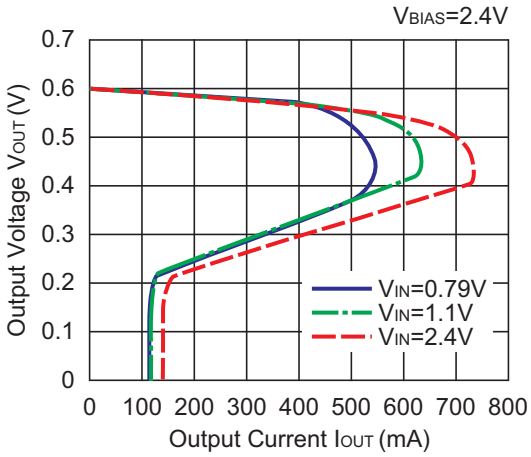
Make V_{BIAS}, V_{IN}, and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor with a capacitance value as much as 1.0 μF or more between V_{BIAS} pin and GND, between V_{IN} pin and GND, and as close as possible to the pins.
Set external components, especially the output capacitor, as close as possible to the device, and make wiring as short as possible. V_{IN} source is supposed to be the output of the DC/DC converter. The value should be equal or lower than V_{BIAS} voltage.

TYPICAL CHARACTERISTICS

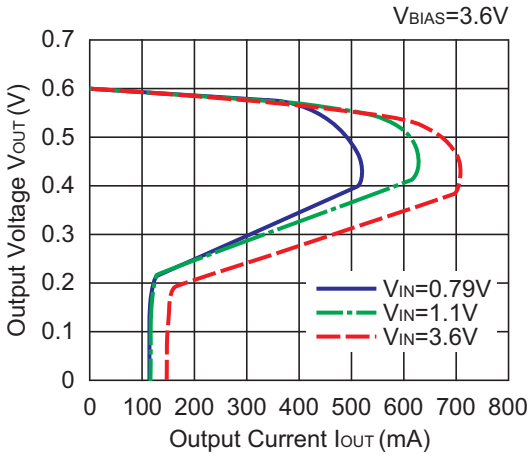
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current (C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, Ta = 25°C)

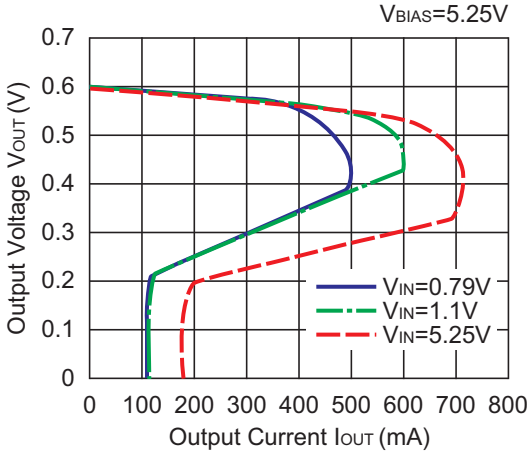
RP105x06xx



RP105x06xx



RP105x06xx



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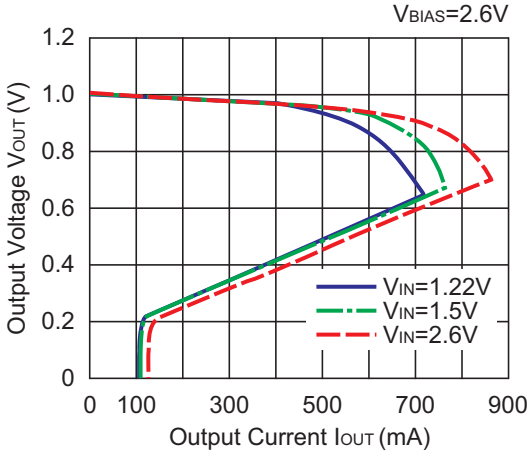

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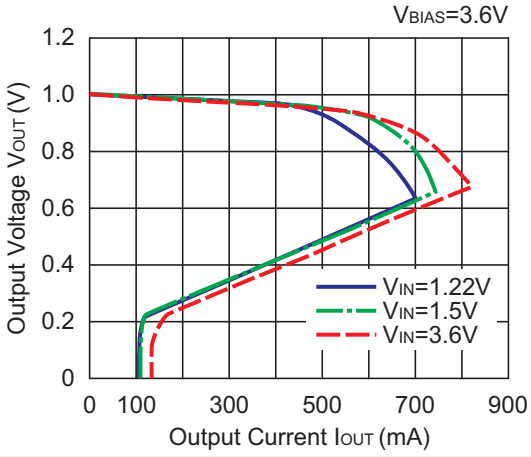

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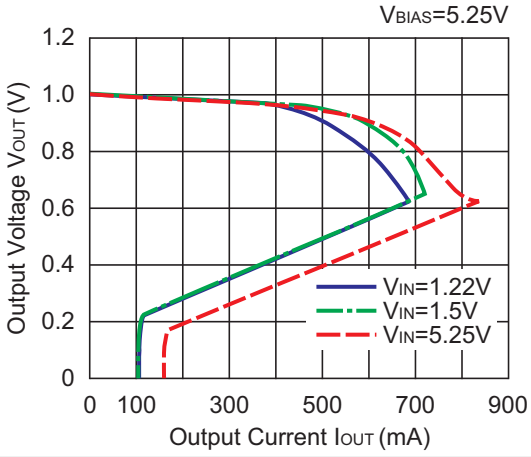

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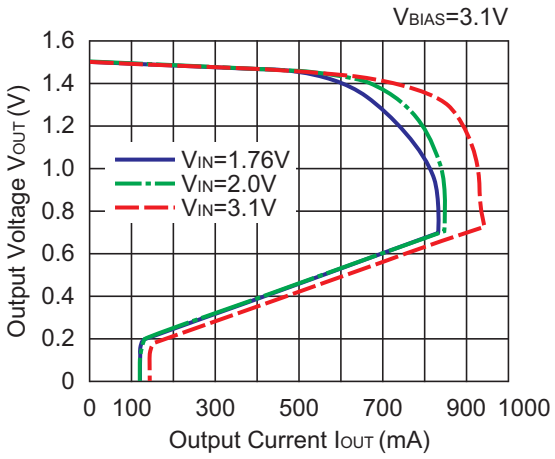

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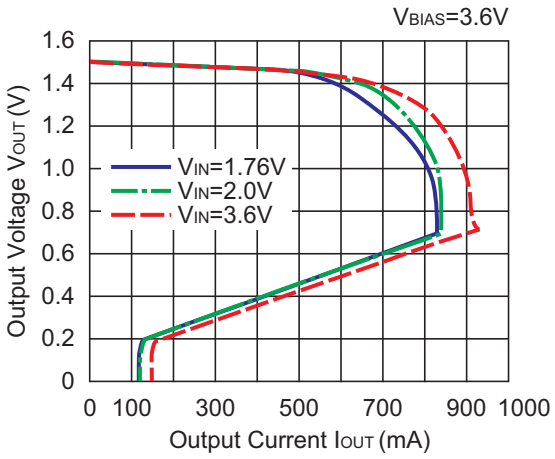

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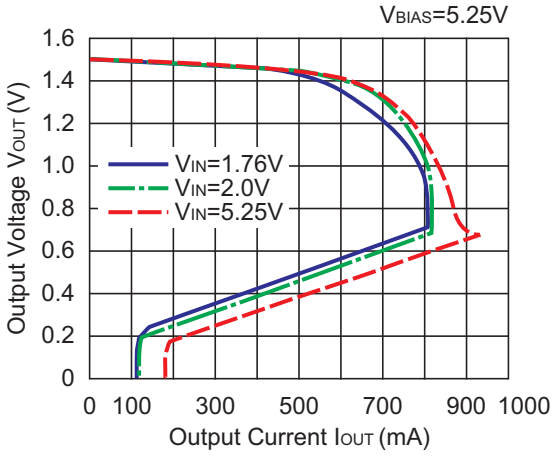
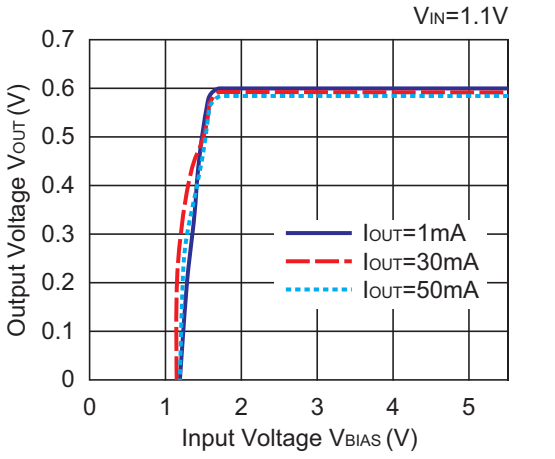


2) Output Voltage vs. Input Voltage (C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, Ta = 25°C)

RP105x06xx



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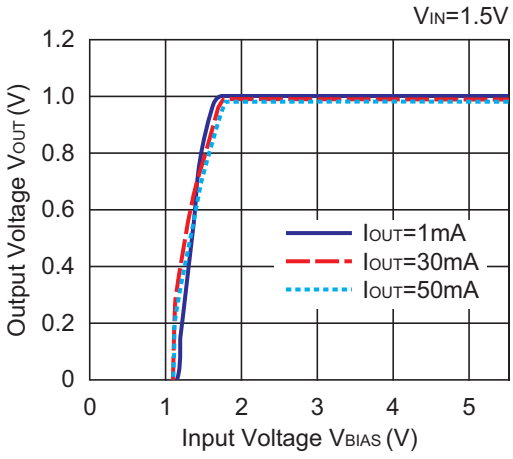

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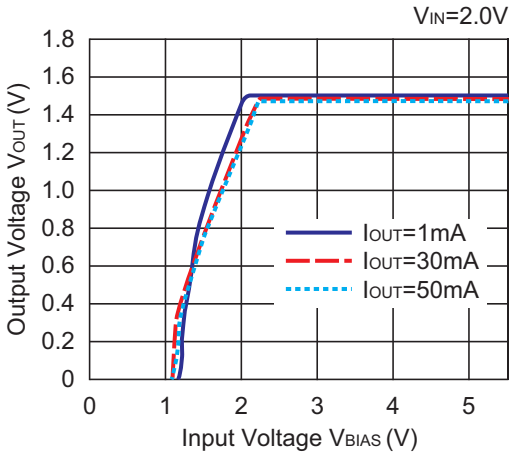

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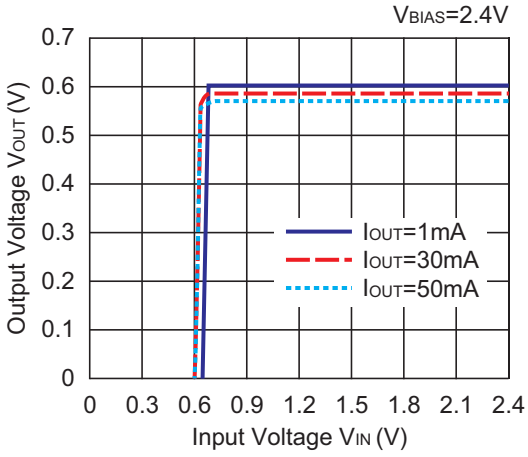

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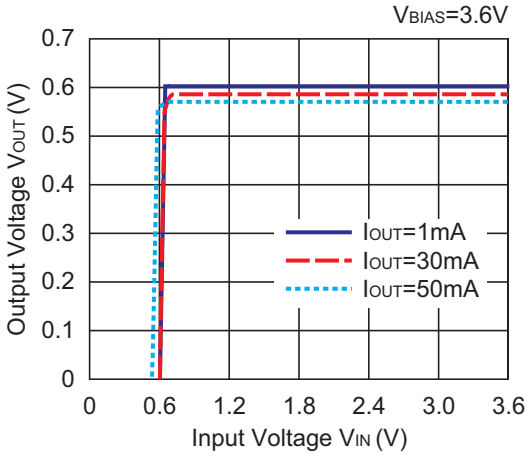

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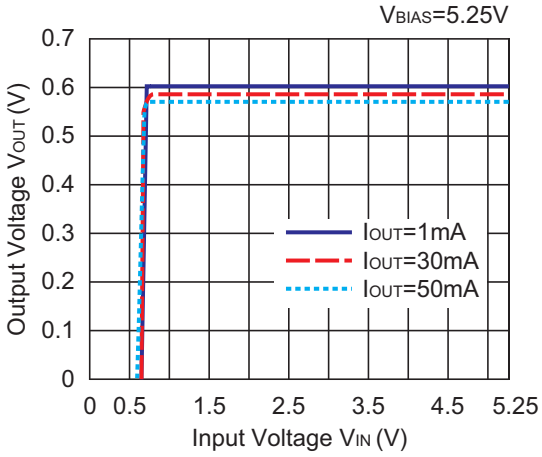

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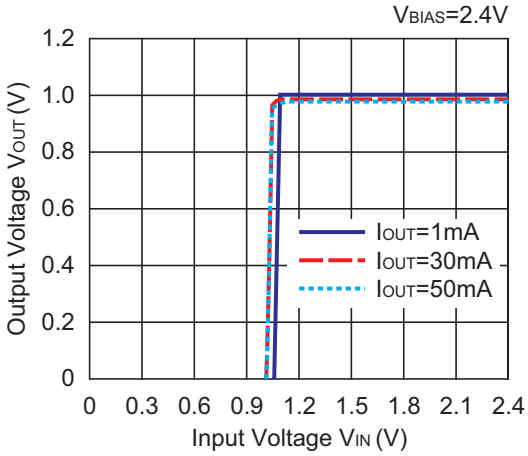

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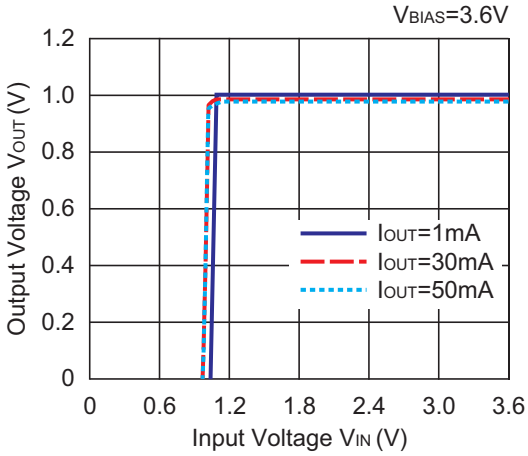

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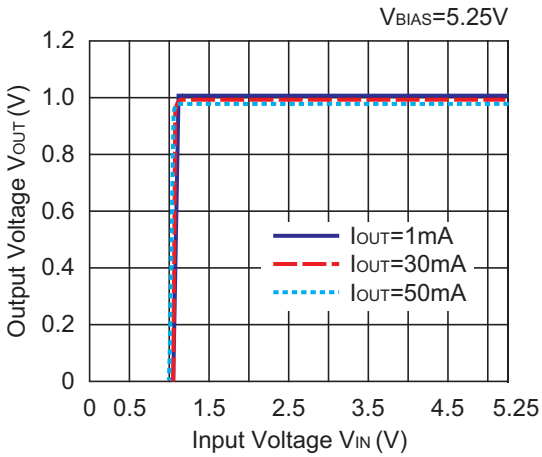

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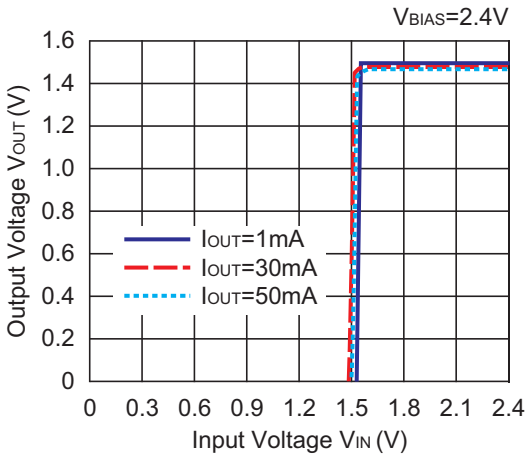

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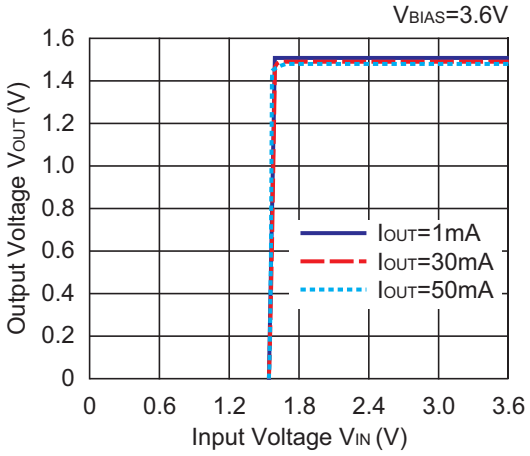

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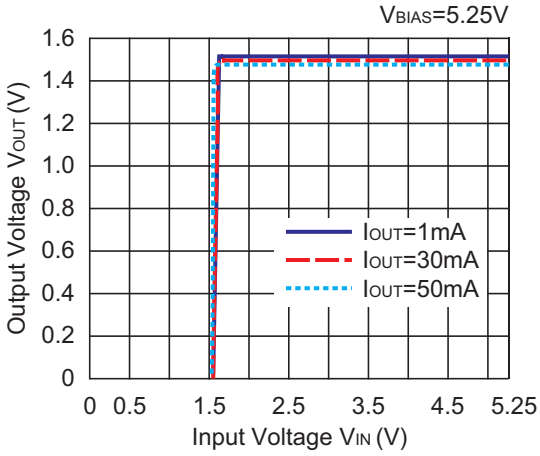

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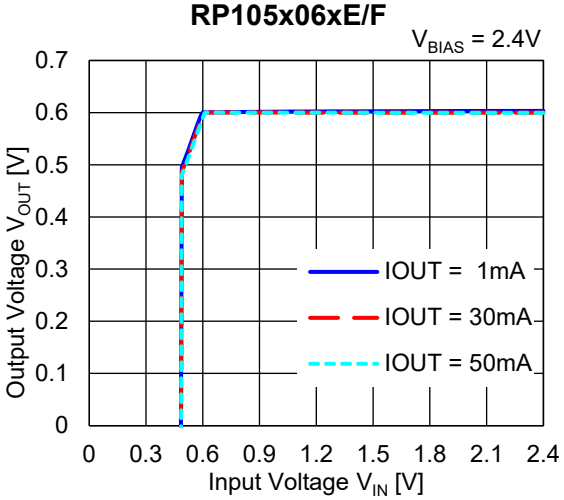

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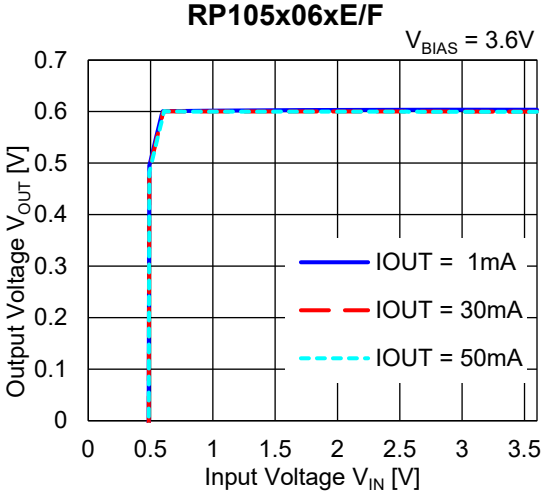

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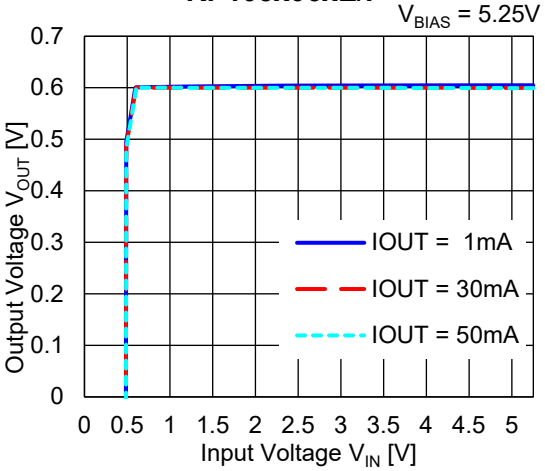

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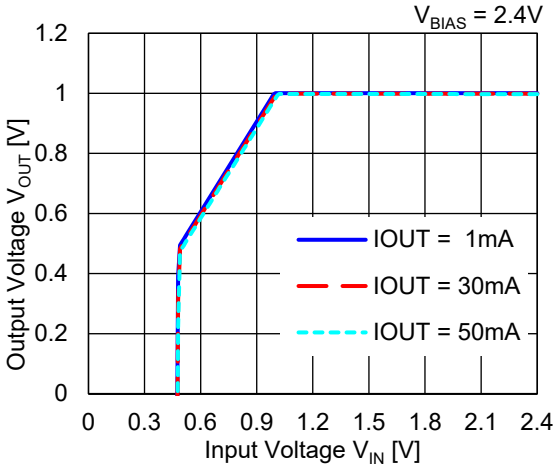

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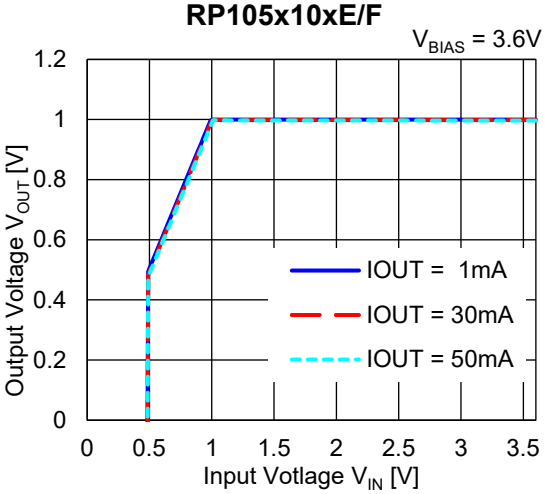

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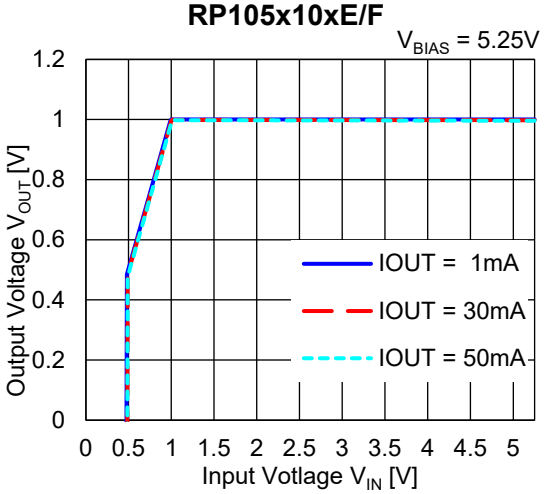

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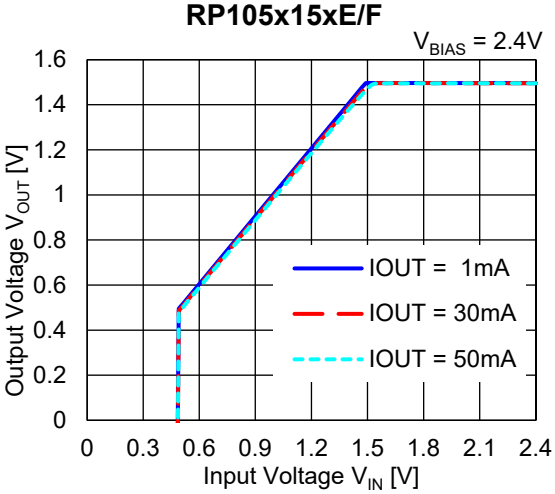

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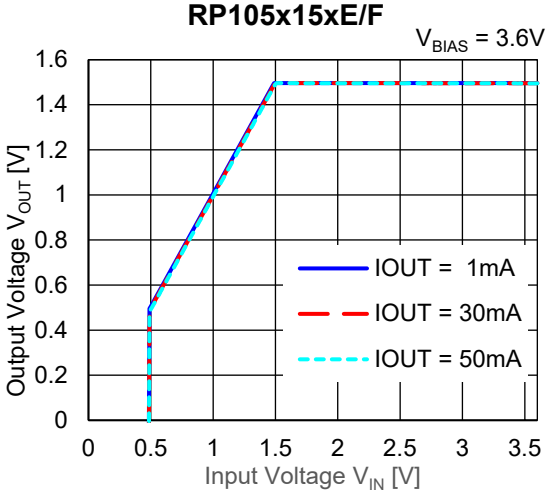
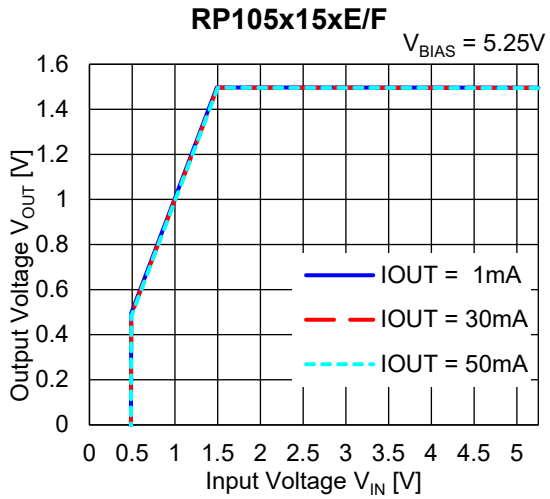
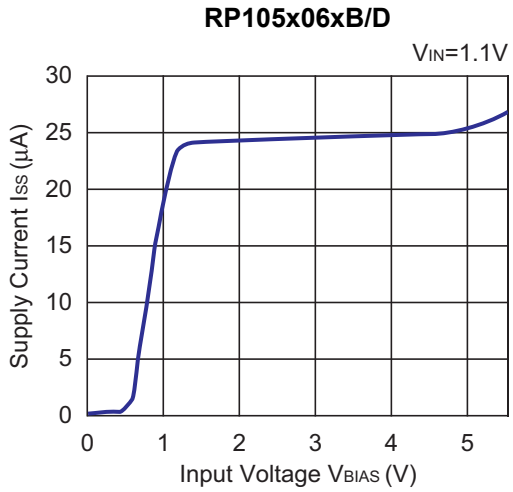
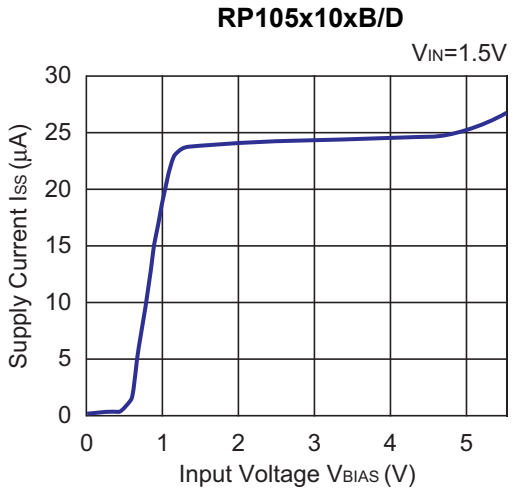
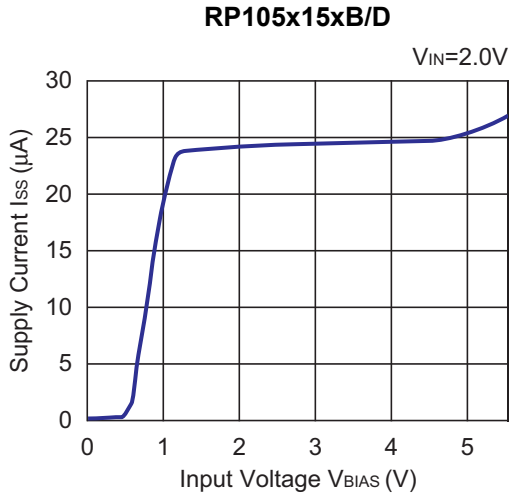


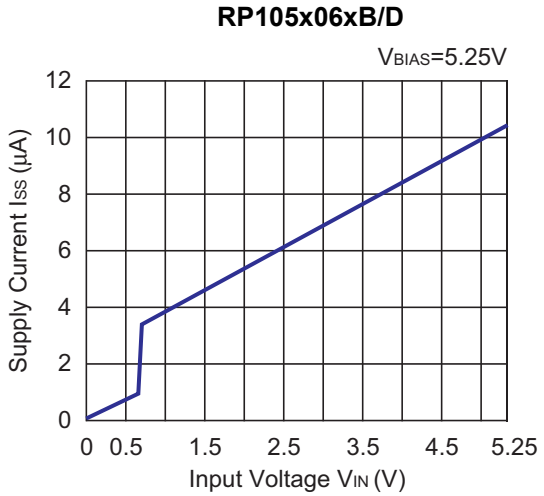


3) Supply Current vs. Input Voltage (C_{BIAS} = C_{IN} = C_{OUT} = none, Ta = 25°C)









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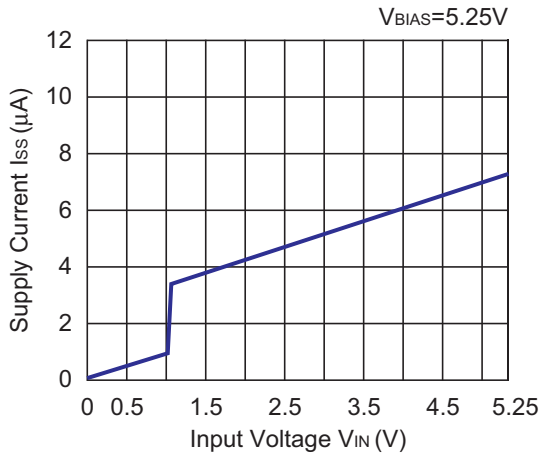

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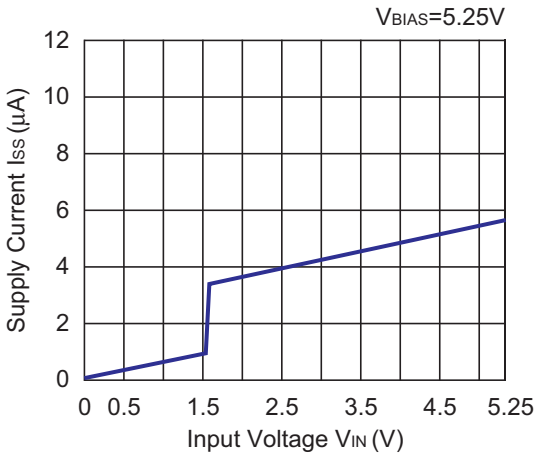

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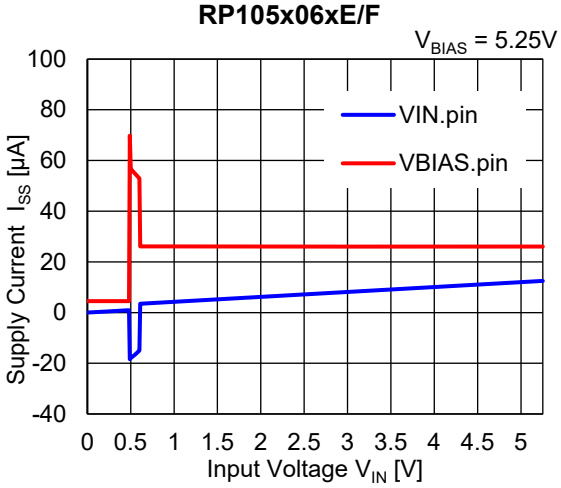

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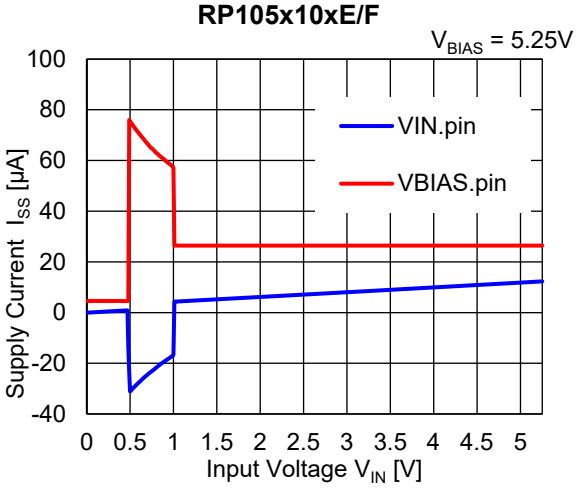

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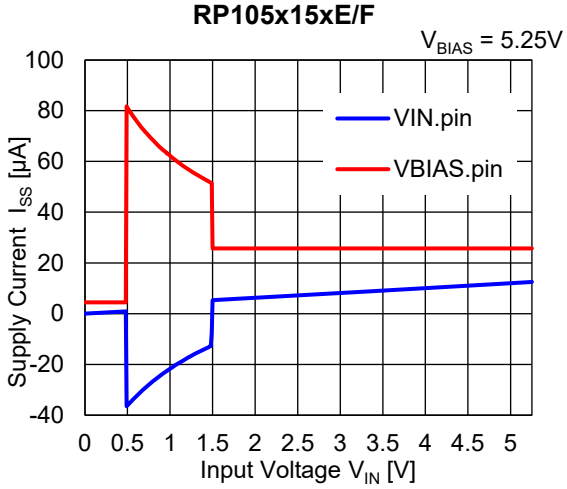
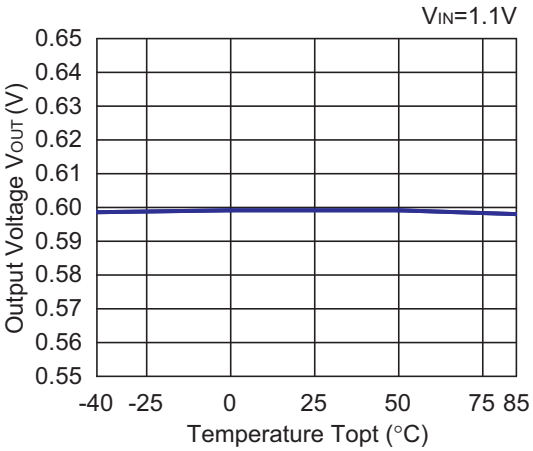


In RP105xxxxE/F, the current flows from V_{BIAS} pin to V_{IN} pin via the inside IC when the input voltage V_{IN} drops below the set output voltage V_{SET}.

4) Output Voltage vs. Temperature (C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, I_{OUT} = 1 mA, V_{BIAS} = 3.6 V)

RP105x06xx



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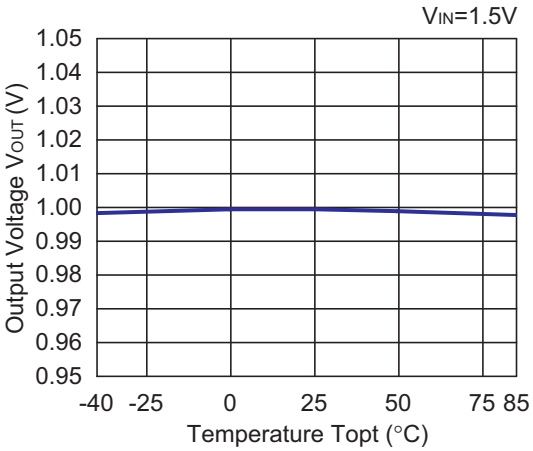

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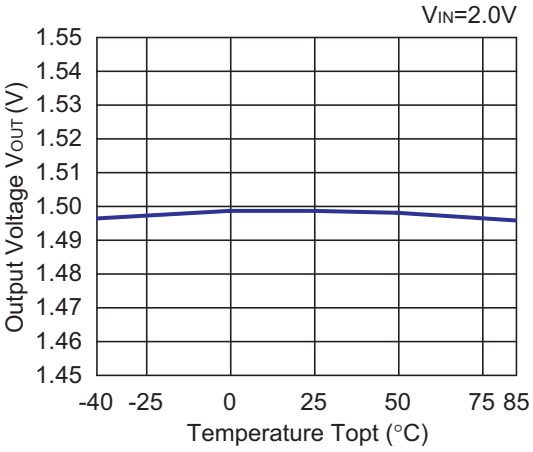
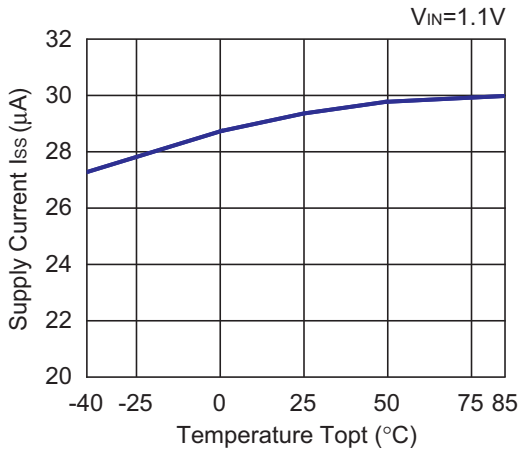


5) Supply Current vs. Temperature (C_{BIAS} = C_{IN} = C_{OUT} = none, V_{BIAS} = 3.6 V)

RP105x06xx



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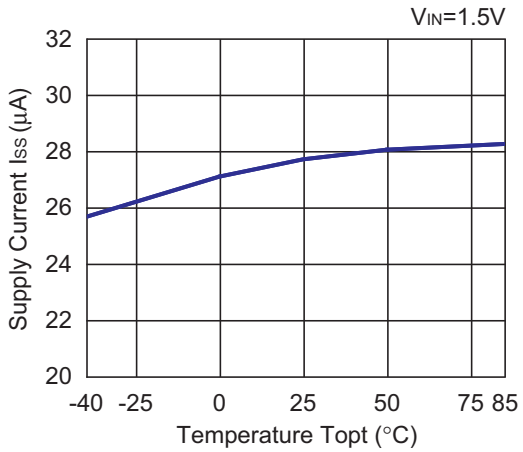
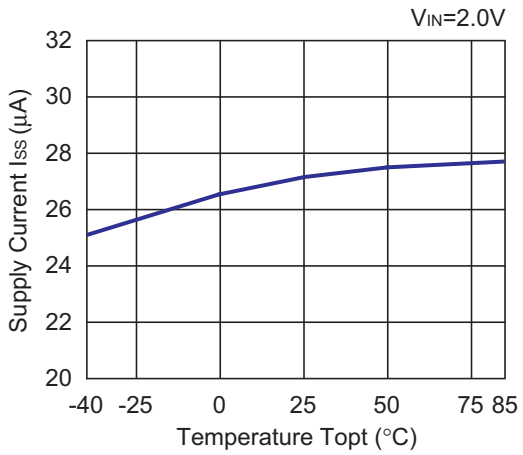
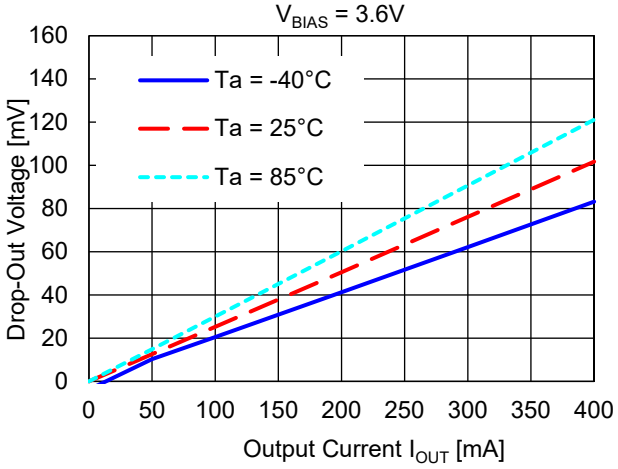


RP105x15xx

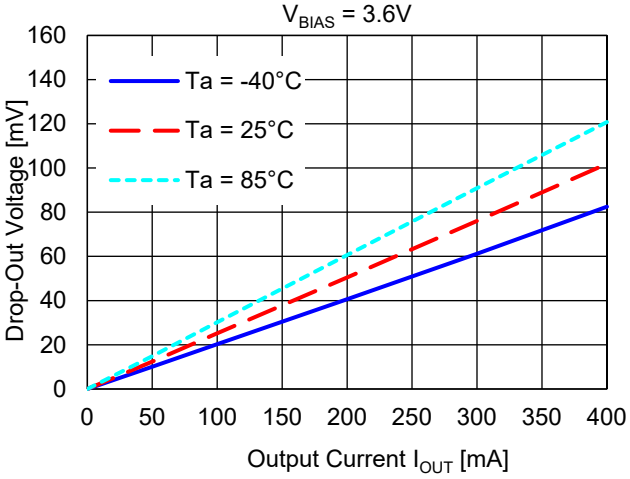


6) Dropout Voltage vs. Output Current (C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF)

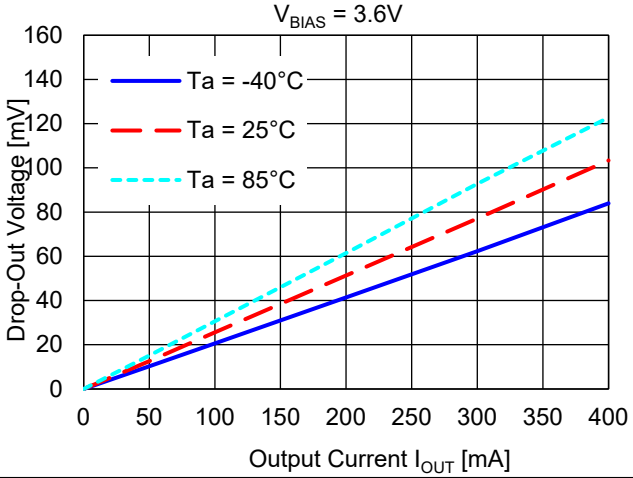
RP105L061E/F



RP105L101E/F

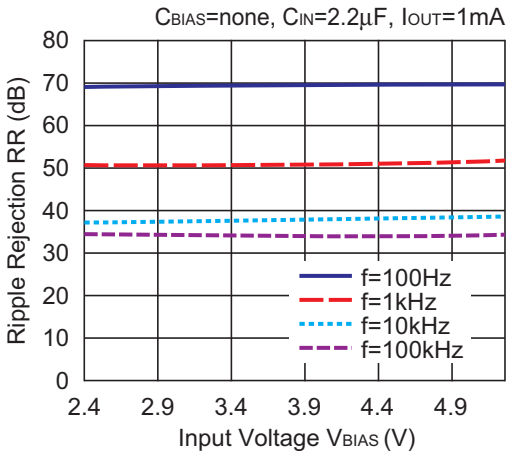


RP105L151E/F



7) Ripple Rejection vs. Input Bias Voltage (C_{OUT} = 2.2 µF, Ripple = 0.2 Vp-p, Ta = 25°C)

RP105x10xx



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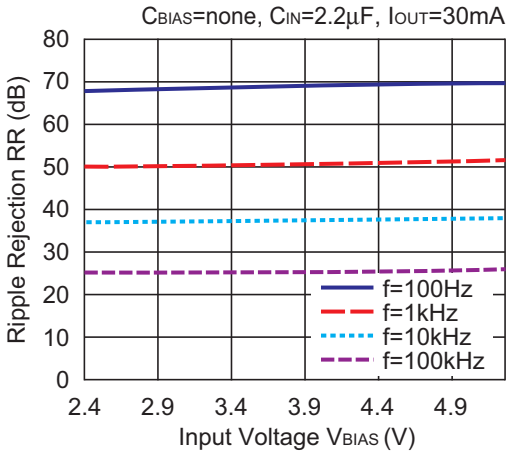

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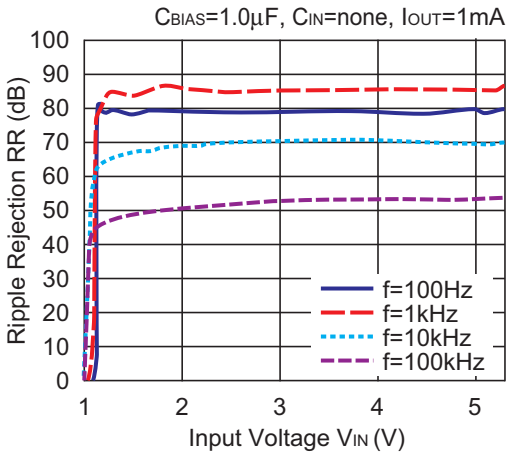

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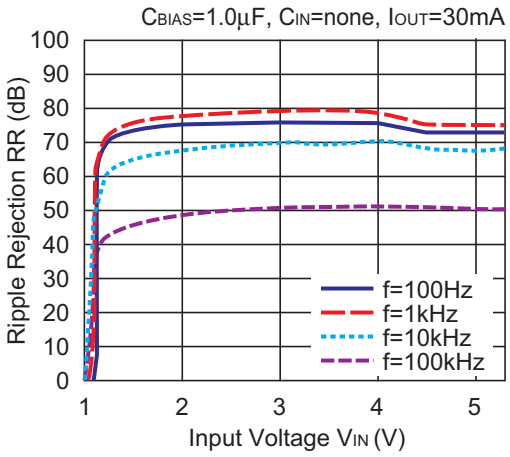
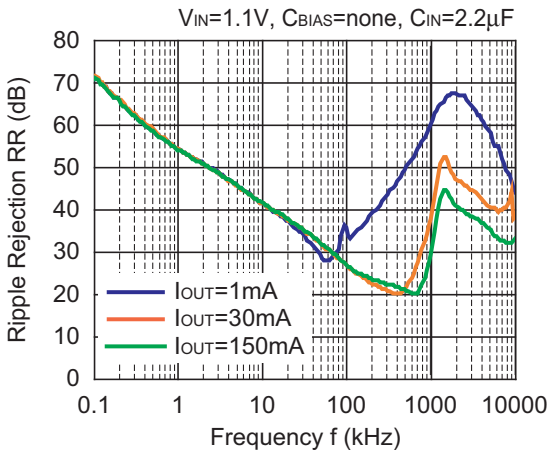


8) Ripple Rejection vs. Frequency (V_{BIAS} = 3.6 V, C_{OUT} = 2.2 µF, Ta = 25°C)

RP105x06xx



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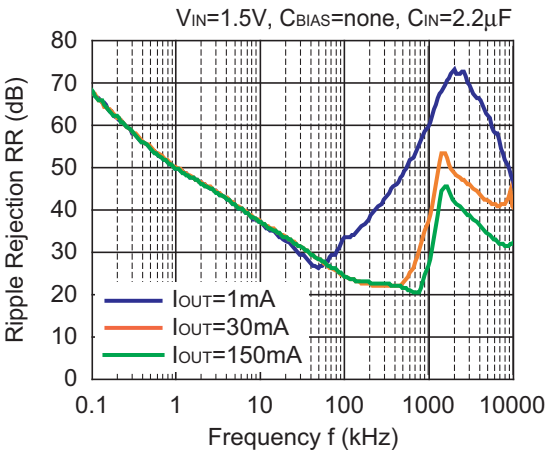

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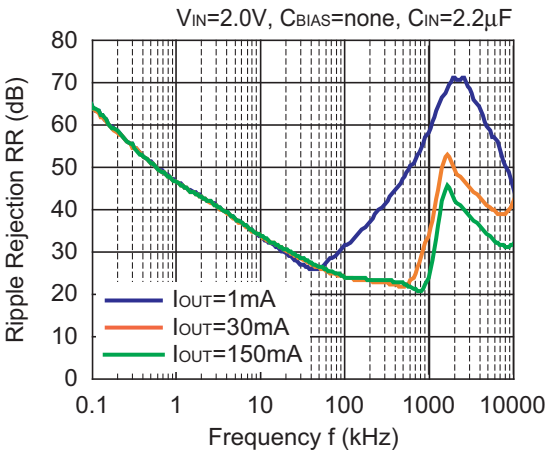

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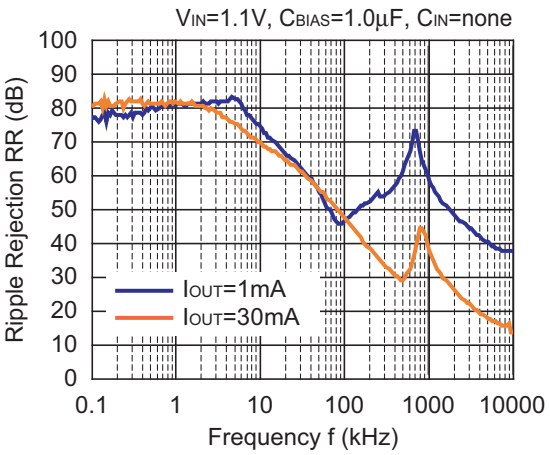

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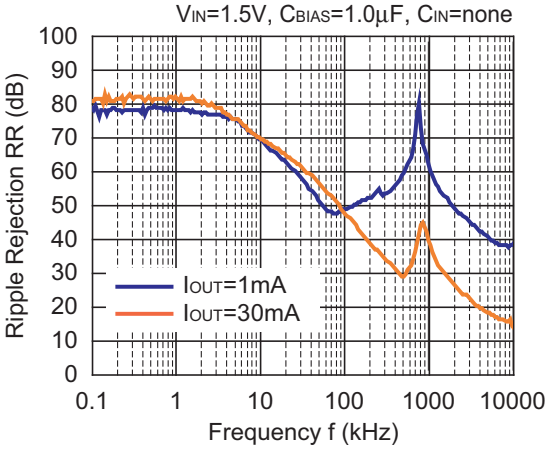
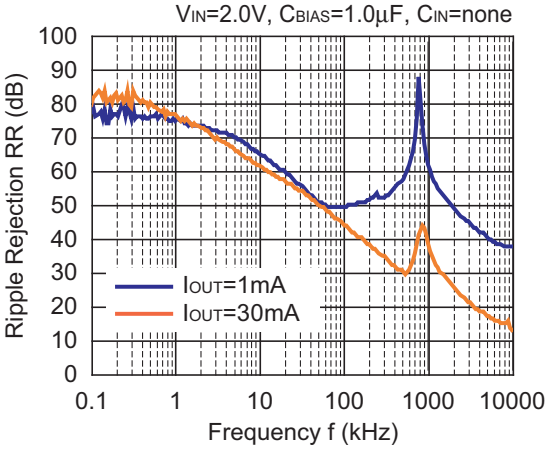
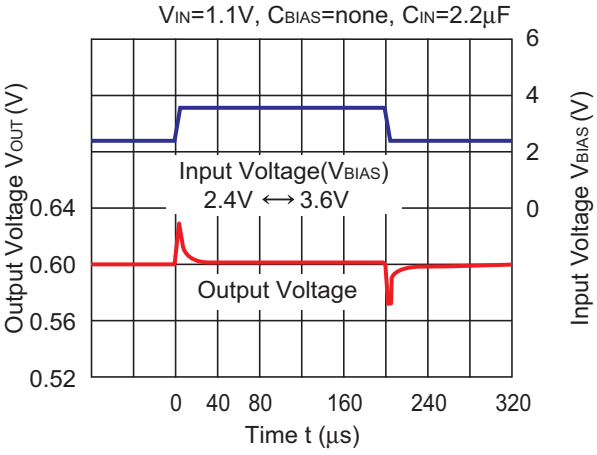


RP105x15xx

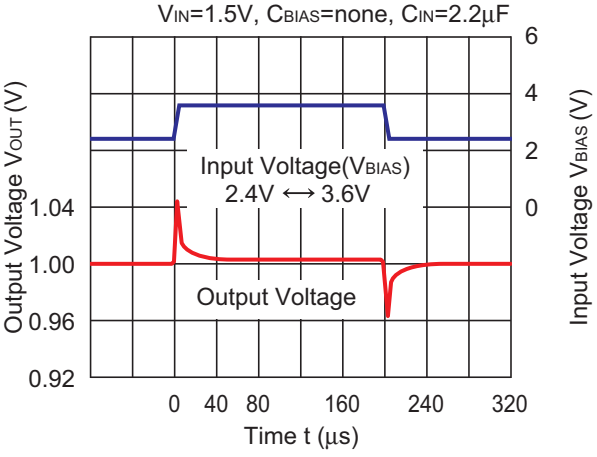


9) Input Transient Response (I_{OUT} = 30 mA, C_{OUT} = 1.0 µF, tr = tf = 5 µs, Ta = 25°C)

RP105x06xx



RP105x10xx



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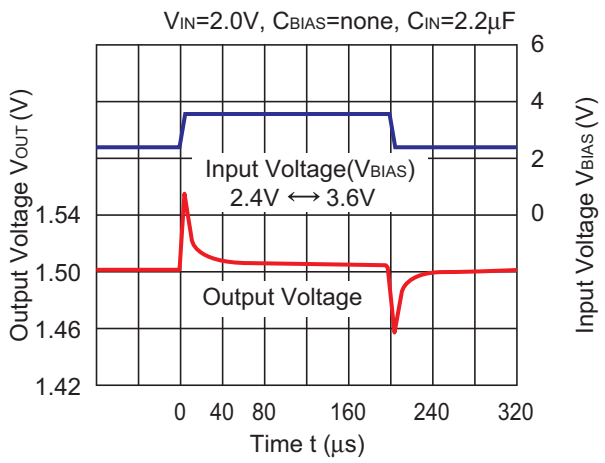

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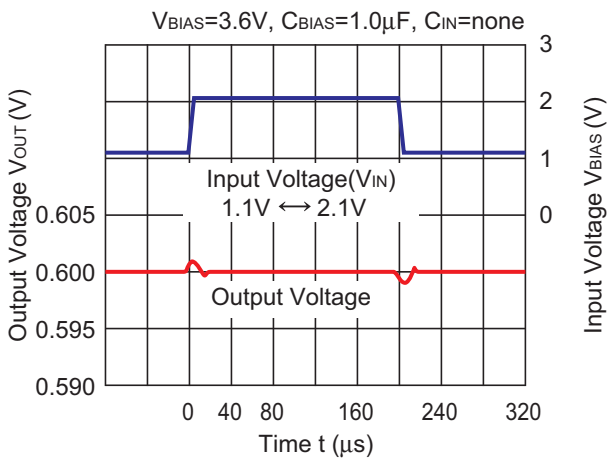

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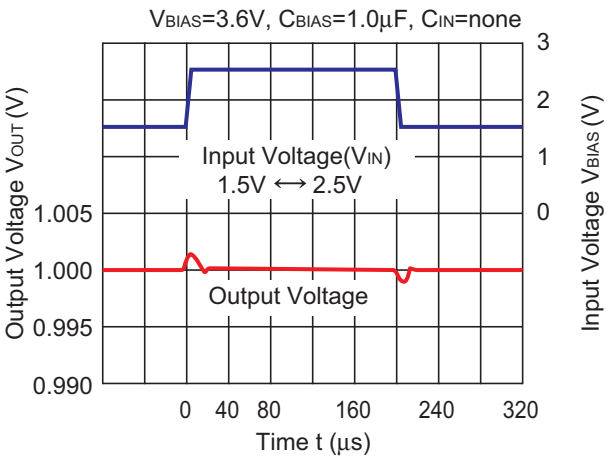

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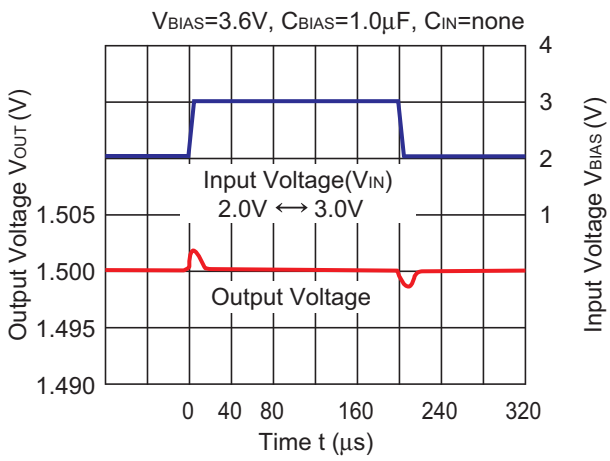
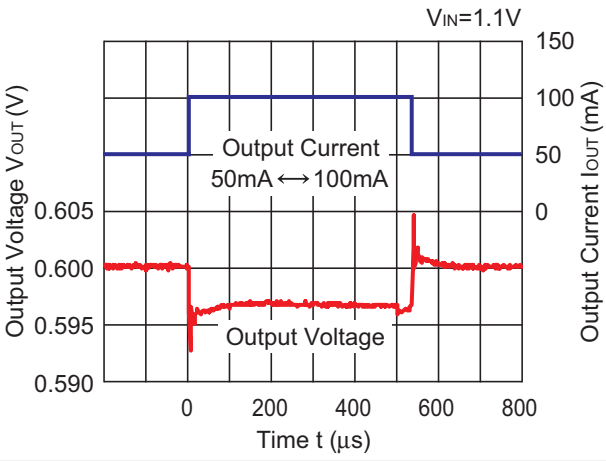
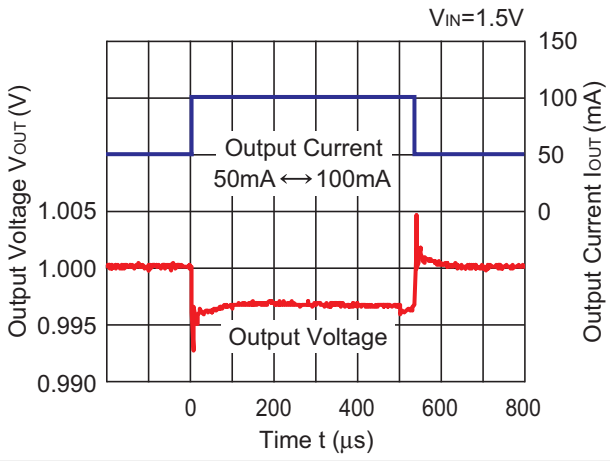


10) Load Transient Response (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, tr = tf = 0.5 µs, Ta = 25°C)

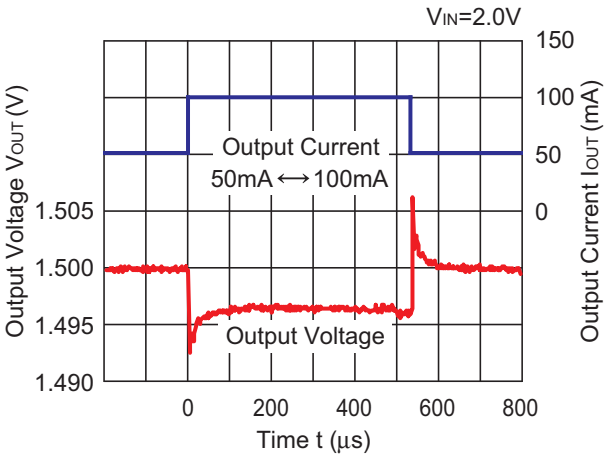
RP105x06xx



RP105x10xx



RP105x15xx



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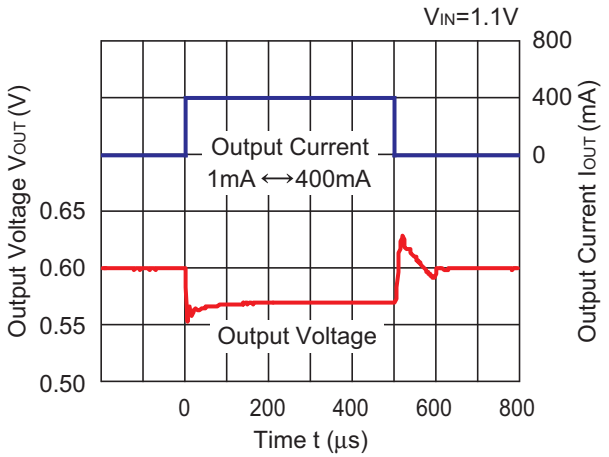

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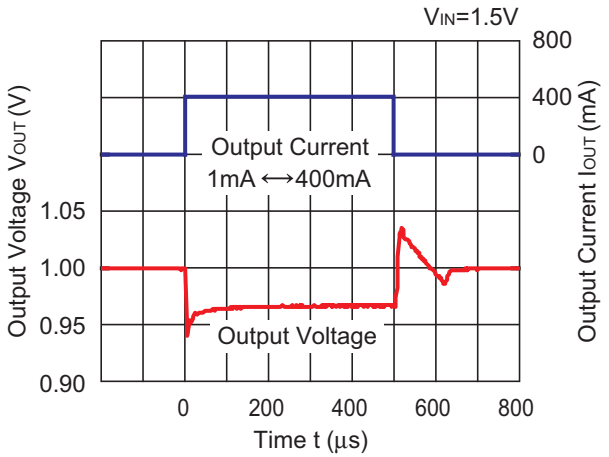

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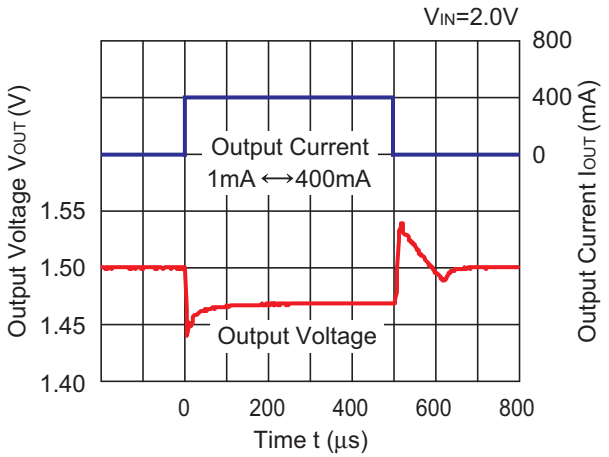
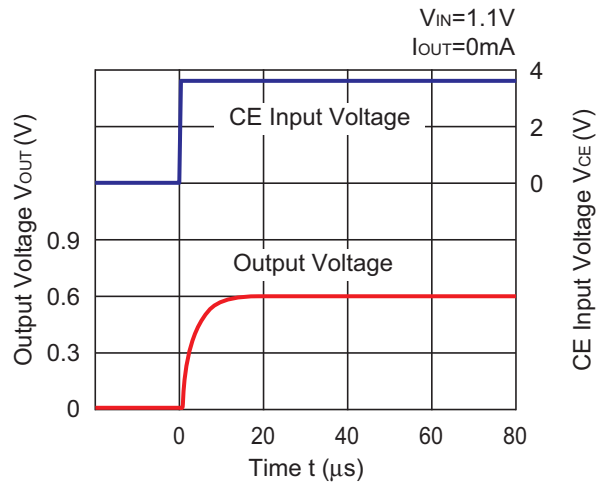
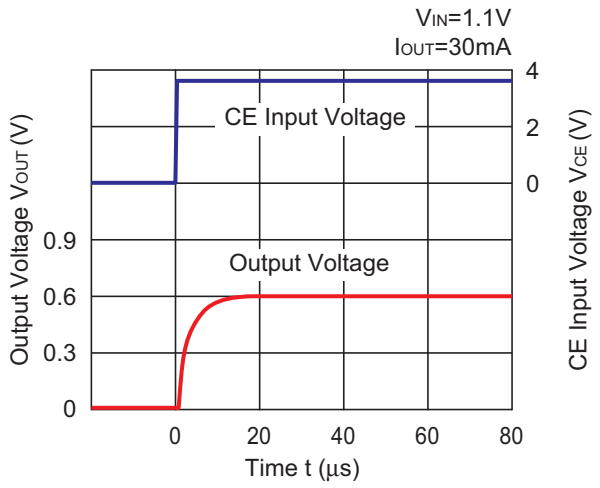


11) Turn On Speed with CE pin (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, Ta = 25°C)

RP105x06xx



RP105x06xx



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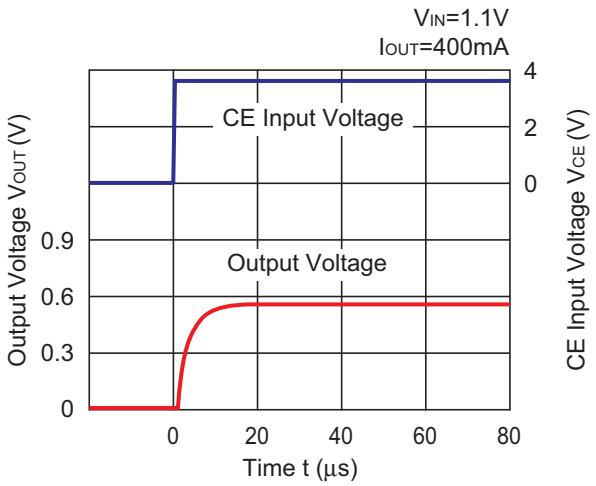
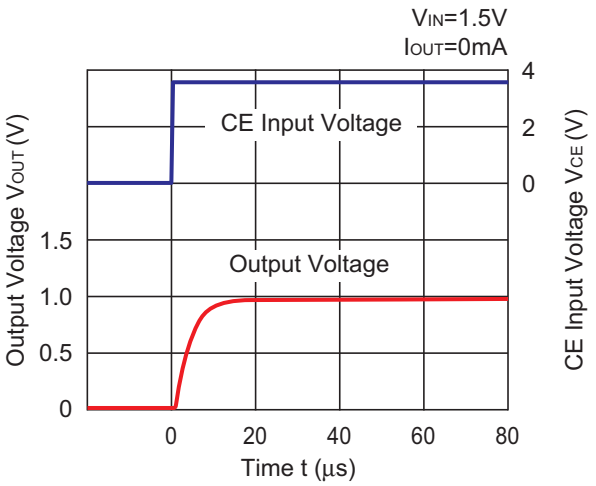
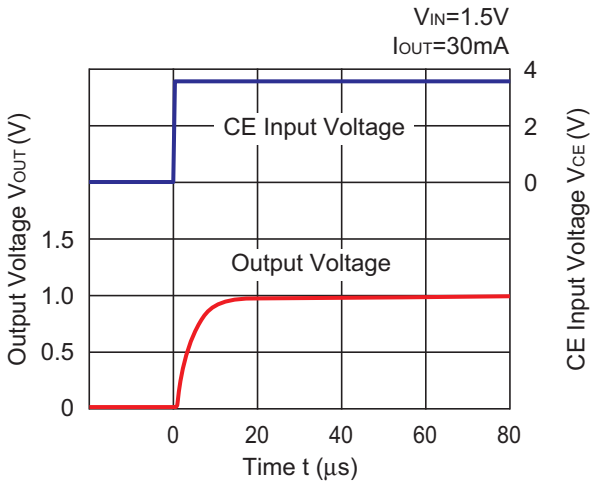


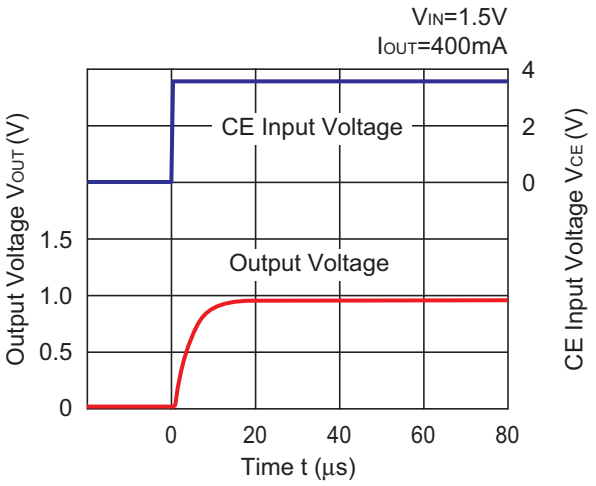
RP105x10xx



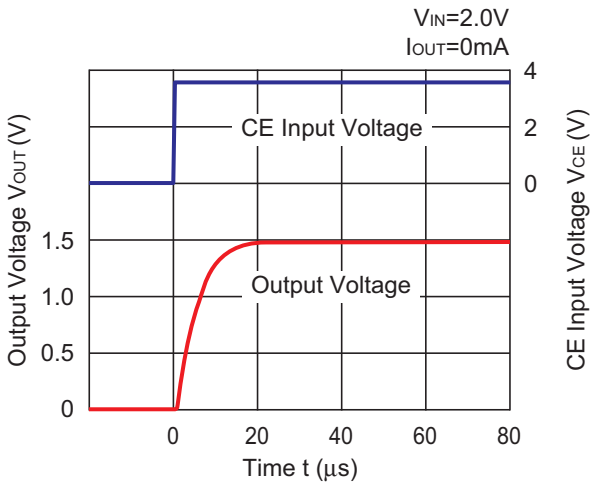
RP105x10xx



RP105x10xx



RP105x15xx



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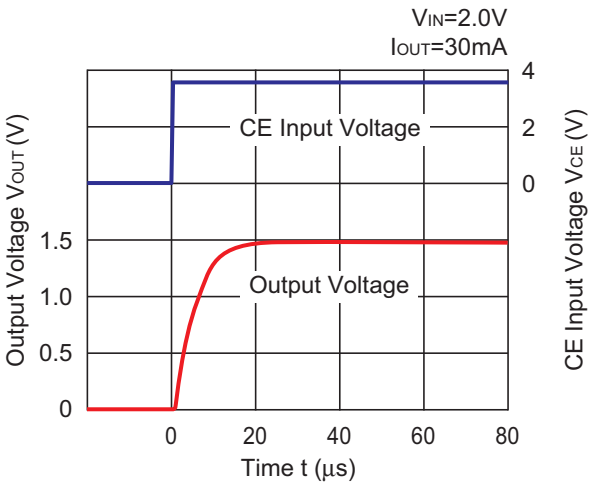
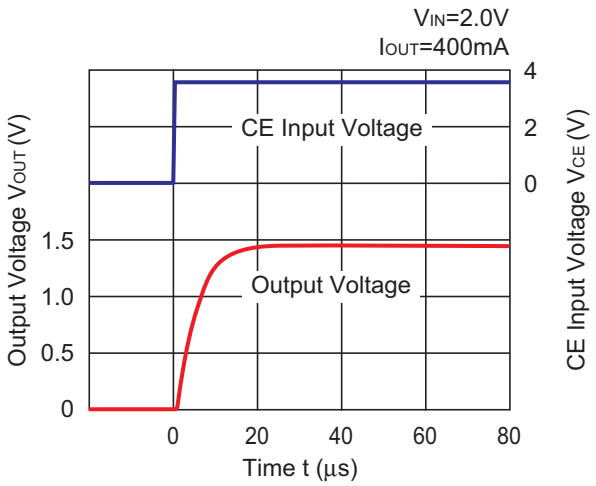
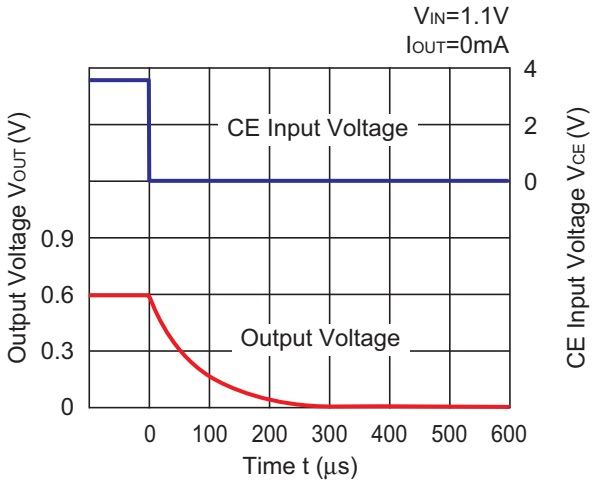


RP105x15xx

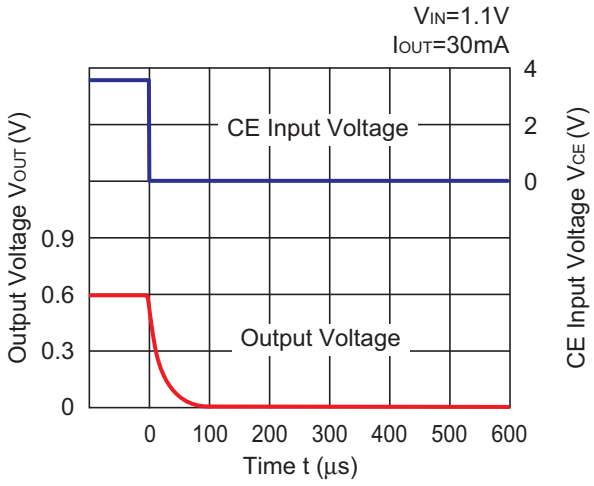


12) Turn Off Speed with CE Pin (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, Ta = 25°C)

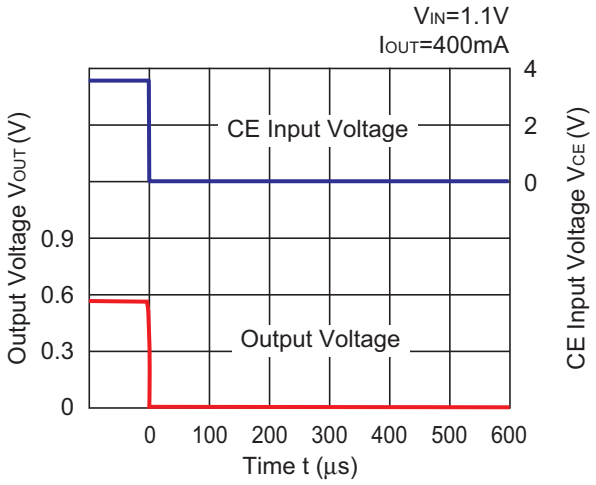
RP105x06xD/F



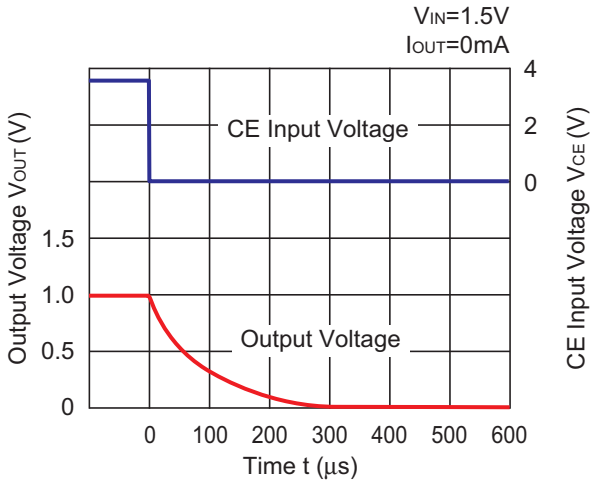
RP105x06xD/F



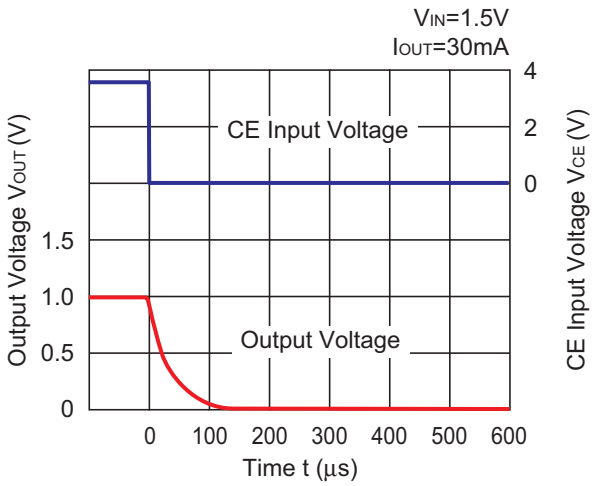
RP105x06xD/F



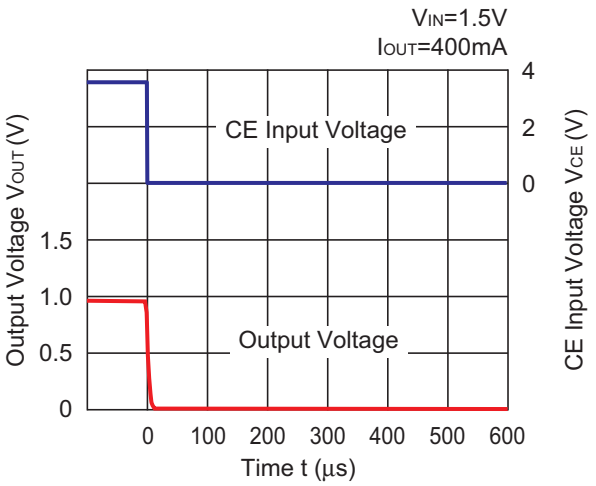
RP105x10xD/F



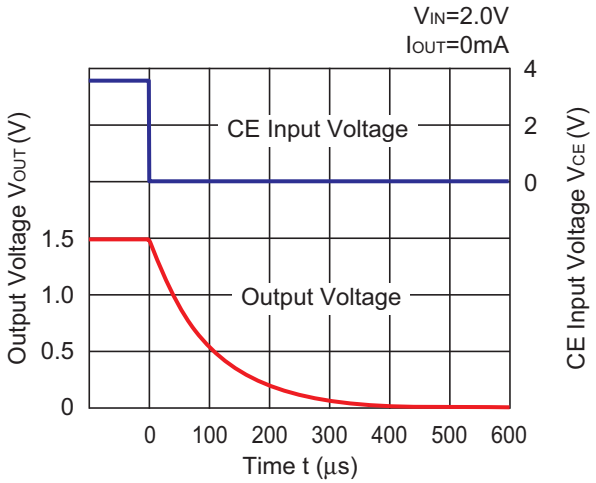
RP105x10xD/F



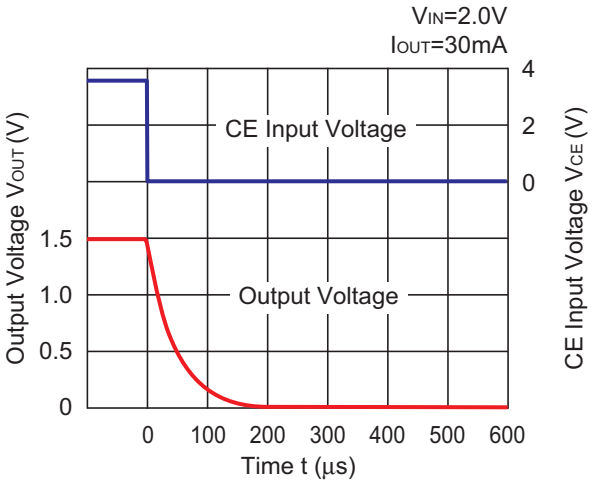
RP105x10xD/F



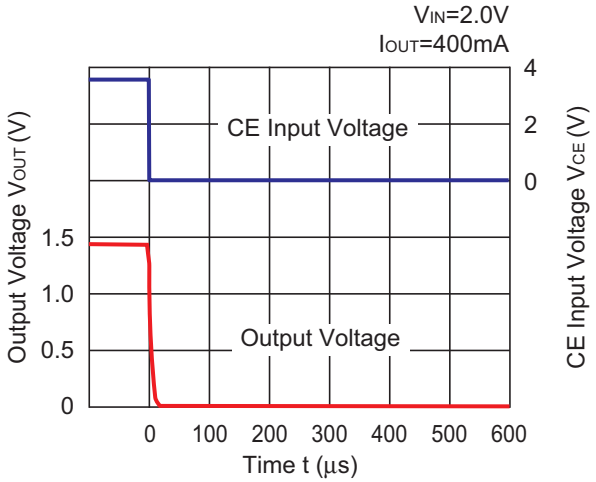
RP105x15xD/F



RP105x15xD/F

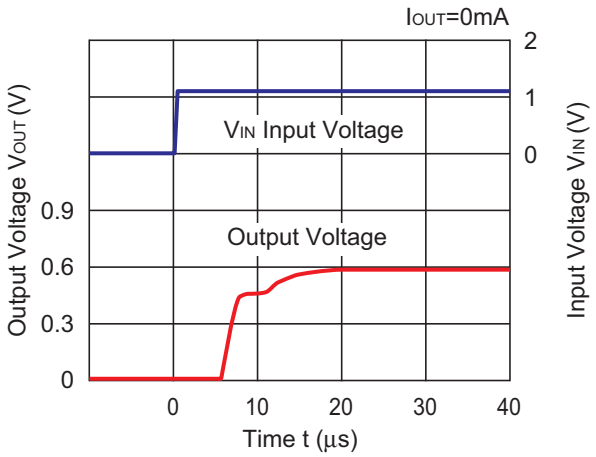


RP105x15xD/F

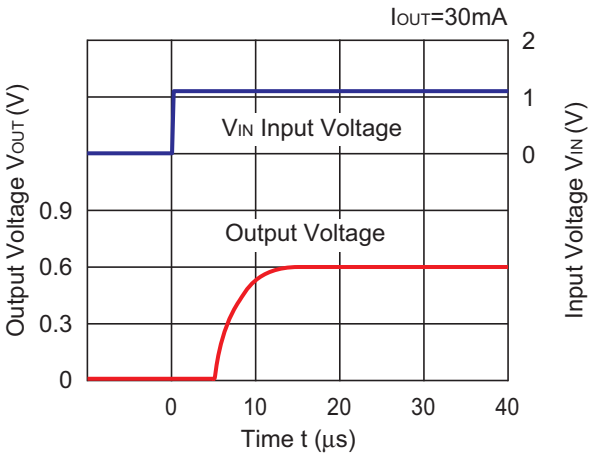


13) Turn On Transient with V_{IN} pin (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 µF, C_{IN} = none, C_{OUT} = 2.2 µF, Ta = 25°C)

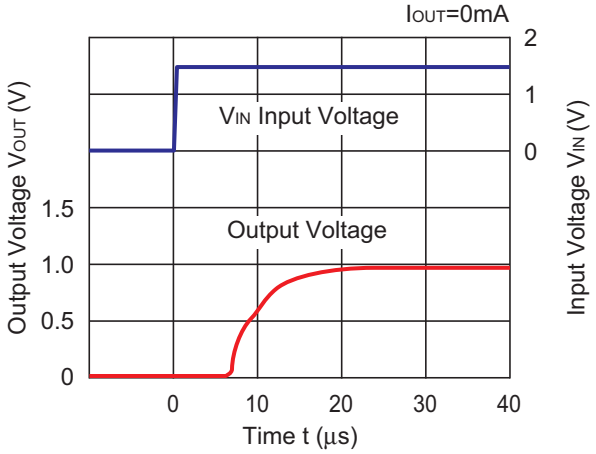
RP105x06xx



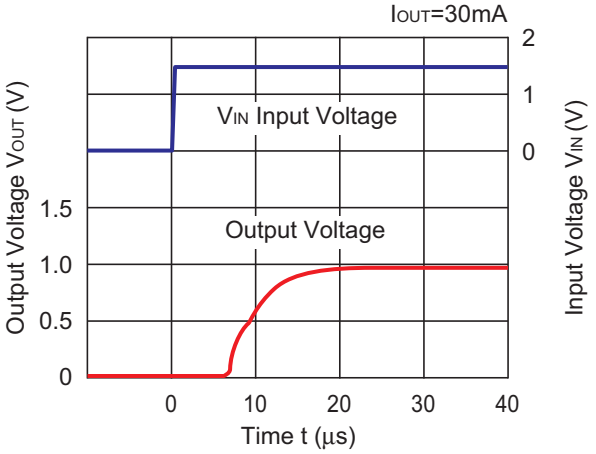
RP105x06xx



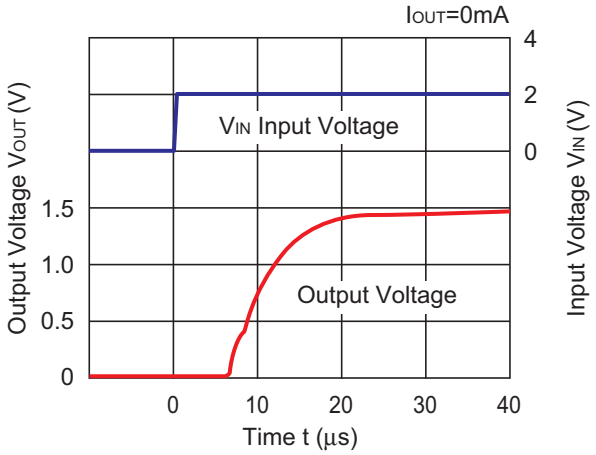
RP105x10xx



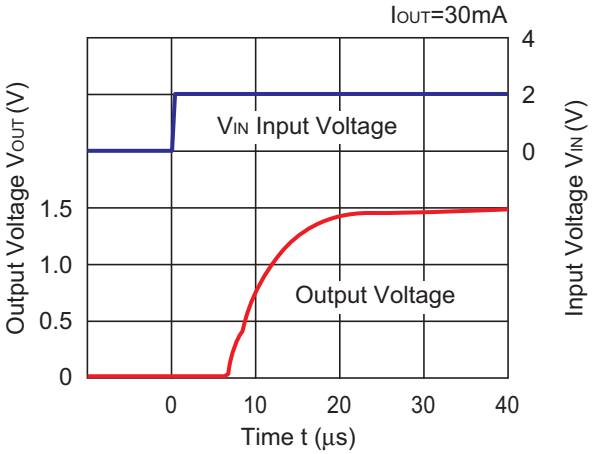
RP105x10xx



RP105x15xx



RP105x15xx

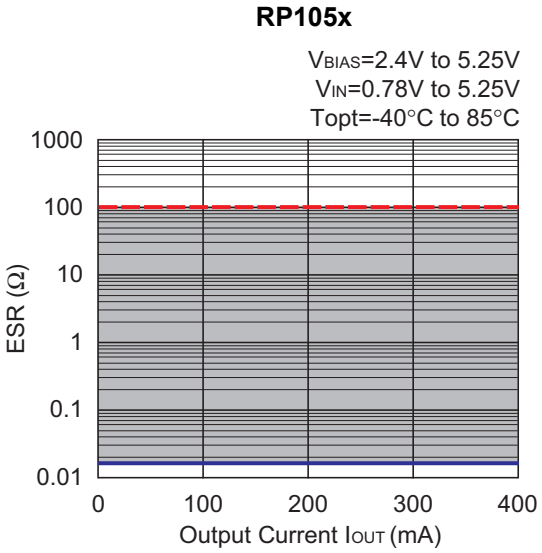


ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The conditions when the white noise level is under 40 μV (Avg.) are marked as the hatched area in the graph.

Measurement conditions

Frequency Band : 10 Hz to 2 MHz
Temperature : −40°C to 85°C
Hatched Area : Noise level is under 40 μV (Avg.)
C_{BIAS}, C_{IN} : 1.0 μF
C_{OUT} : 2.2 μF



PD-DFN(PL)1212-6-(85 125)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

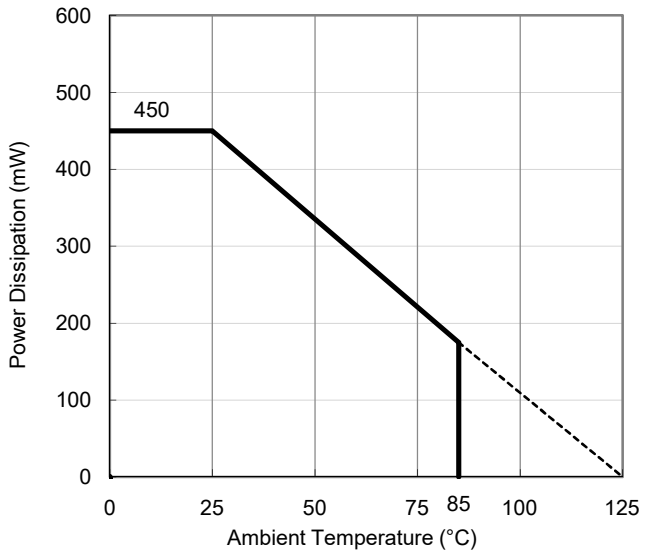
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.2 mm × 14 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

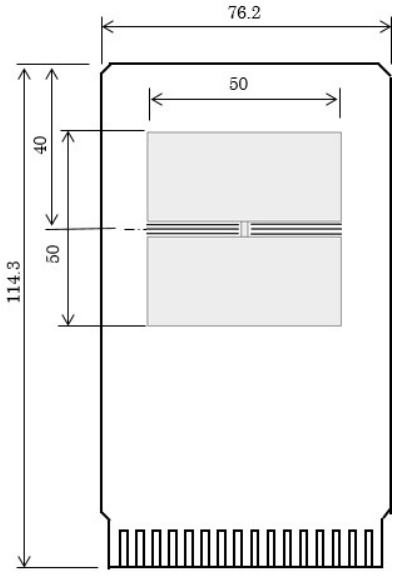
Item	Measurement Result
Power Dissipation	450 mW
Thermal Resistance (θja)	θja = 218°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 105°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

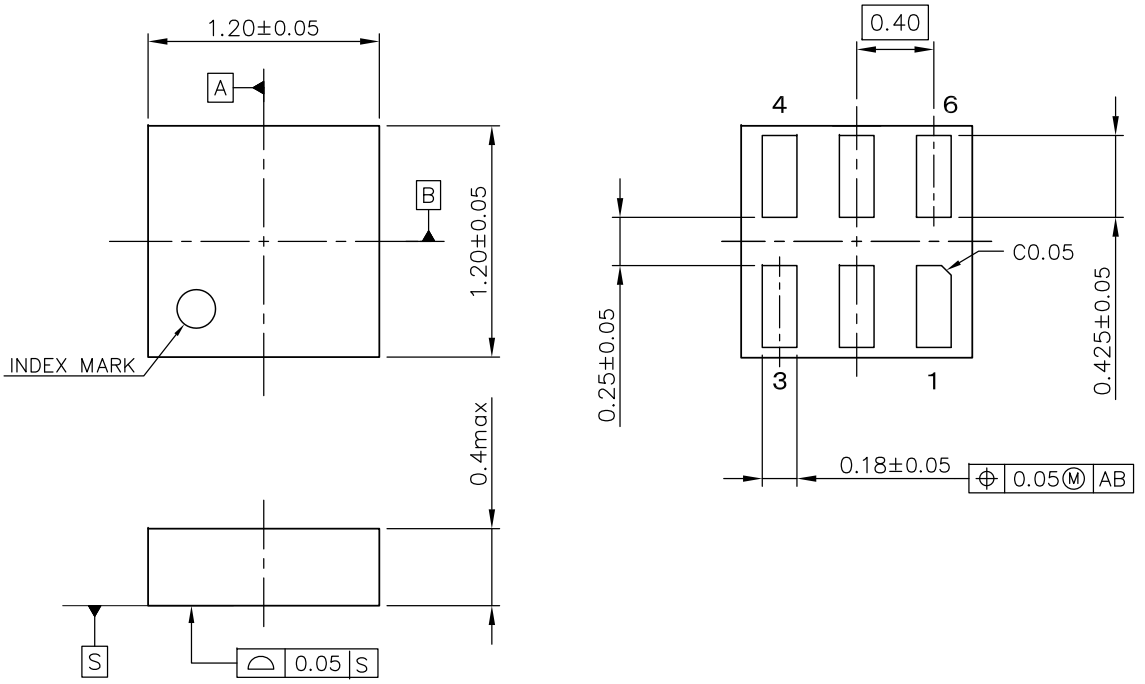


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

DM-DFN(PL)1212-6-JE-B



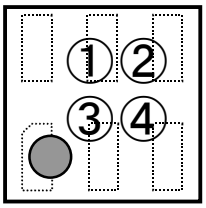
UNIT: mm

DFN(PL)1212-6 Package Dimensions

MK-RP105K-JE-B

①②: Product Code ⋯ Refer to *Part Marking List*

③④: Lot Number ⋯ Alphanumeric Serial Number



DFN(PL)1212-6 Part Markings

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

RP105K Part Marking List

RP105KxxxB

Product Name	① ②	V_{SET}
RP105K061B	A A	0.6 V
RP105K071B	A B	0.7 V
RP105K081B	A C	0.8 V
RP105K091B	A D	0.9 V
RP105K101B	A E	1.0 V
RP105K121B	A F	1.2 V
RP105K131B	A G	1.3 V
RP105K141B	A H	1.4 V
RP105K151B	A J	1.5 V
RP105K111B	A K	1.1 V

RP105KxxxD

Product Name	① ②	V_{SET}
RP105K061D	B A	0.6 V
RP105K071D	B B	0.7 V
RP105K081D	B C	0.8 V
RP105K091D	B D	0.9 V
RP105K101D	B E	1.0 V
RP105K121D	B F	1.2 V
RP105K131D	B G	1.3 V
RP105K141D	B H	1.4 V
RP105K151D	B J	1.5 V
RP105K111D	B K	1.1 V

RP105KxxxE

Product Name	① ②	V_{SET}
RP105K061E	9 A	0.6 V
RP105K071E	9 B	0.7 V
RP105K081E	9 C	0.8 V
RP105K091E	9 D	0.9 V
RP105K101E	9 E	1.0 V
RP105K121E	9 F	1.2 V
RP105K131E	9 G	1.3 V
RP105K141E	9 H	1.4 V
RP105K151E	9 J	1.5 V
RP105K111E	9 K	1.1 V

RP105KxxxF

Product Name	① ②	V_{SET}
RP105K061F	0 A	0.6 V
RP105K071F	0 B	0.7 V
RP105K081F	0 C	0.8 V
RP105K091F	0 D	0.9 V
RP105K101F	0 E	1.0 V
RP105K121F	0 F	1.2 V
RP105K131F	0 G	1.3 V
RP105K141F	0 H	1.4 V
RP105K151F	0 J	1.5 V
RP105K111F	0 K	1.1 V

PD-SC-88A(85125)-JE-B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

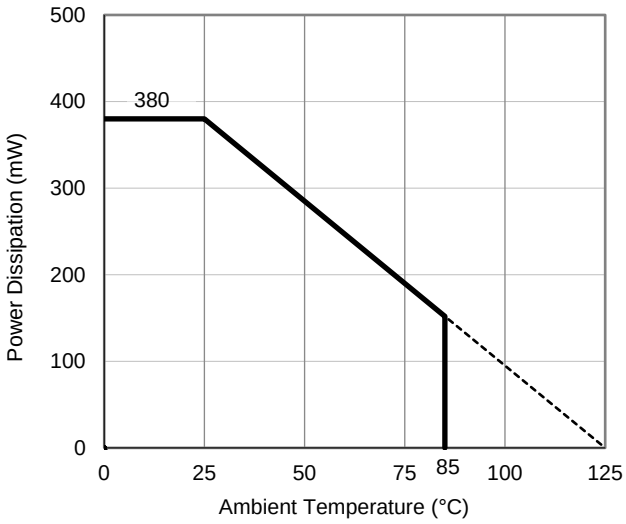
Item	Standard Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-Sided Board)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top Side: Approx. 50% Bottom Side: Approx. 50%
Through-holes	ϕ 0.5 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

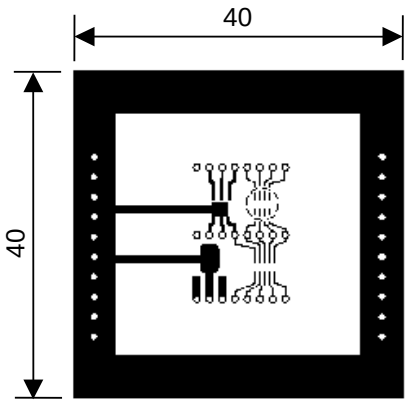
Item	Standard Test Land Pattern
Power Dissipation	380 mW
Thermal Resistance (θja)	θja = 263°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 75°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

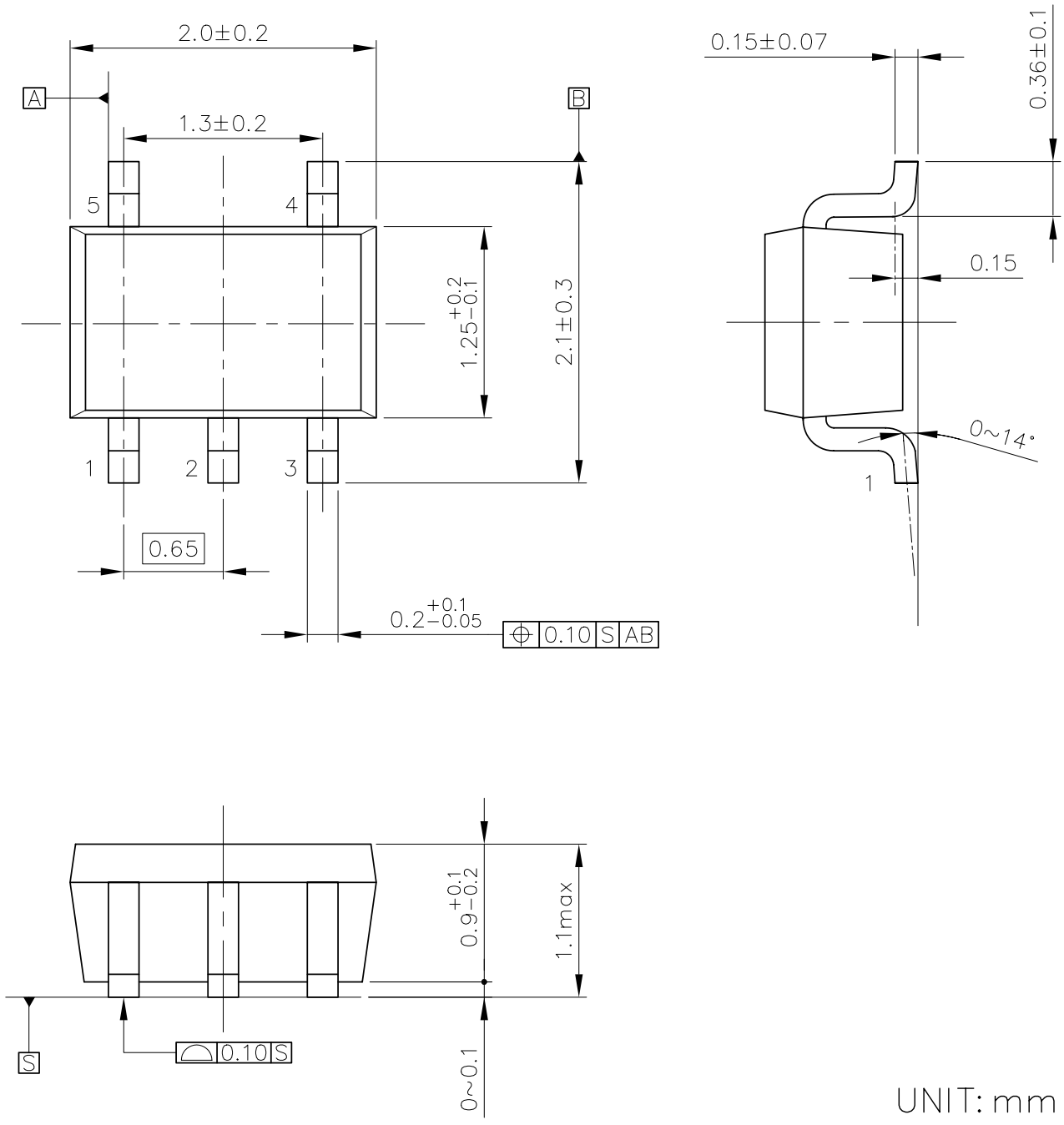


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

DM-SC-88A-JE-A



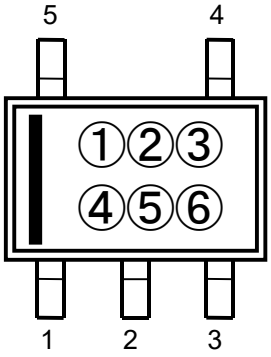
UNIT: mm

SC-88A Package Dimensions

MK-RP105Q-JBEC

①②③④: Product Code ⋯ Refer to *Part Marking List*

⑤⑥: Lot Number ⋯ Alphanumeric Serial Number



SC-88A Part Markings

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

RP105Q Part Marking List

RP105QxxxB

Product Name	① ② ③ ④	V_{SET}
RP105Q062B	E 0 0 1	0.6 V
RP105Q072B	E 0 0 2	0.7 V
RP105Q082B	E 0 0 3	0.8 V
RP105Q092B	E 0 0 4	0.9 V
RP105Q102B	E 0 0 5	1.0 V
RP105Q122B	E 0 0 6	1.2 V
RP105Q132B	E 0 0 7	1.3 V
RP105Q142B	E 0 0 8	1.4 V
RP105Q152B	E 0 0 9	1.5 V
RP105Q112B	E 0 1 0	1.1 V

RP105QxxxD

Product Name	① ② ③ ④	V_{SET}
RP105Q062D	F 0 0 1	0.6 V
RP105Q072D	F 0 0 2	0.7 V
RP105Q082D	F 0 0 3	0.8 V
RP105Q092D	F 0 0 4	0.9 V
RP105Q102D	F 0 0 5	1.0 V
RP105Q122D	F 0 0 6	1.2 V
RP105Q132D	F 0 0 7	1.3 V
RP105Q142D	F 0 0 8	1.4 V
RP105Q152D	F 0 0 9	1.5 V
RP105Q112D	F 0 1 0	1.1 V

PD-SOT-23-5-(85125)-JE-B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

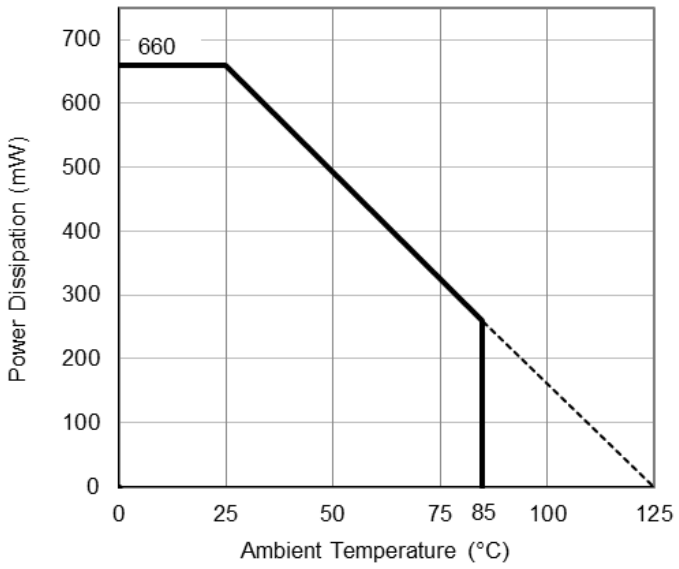
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 7 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

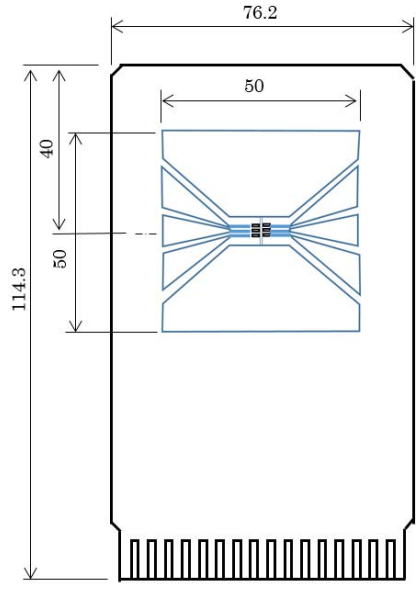
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

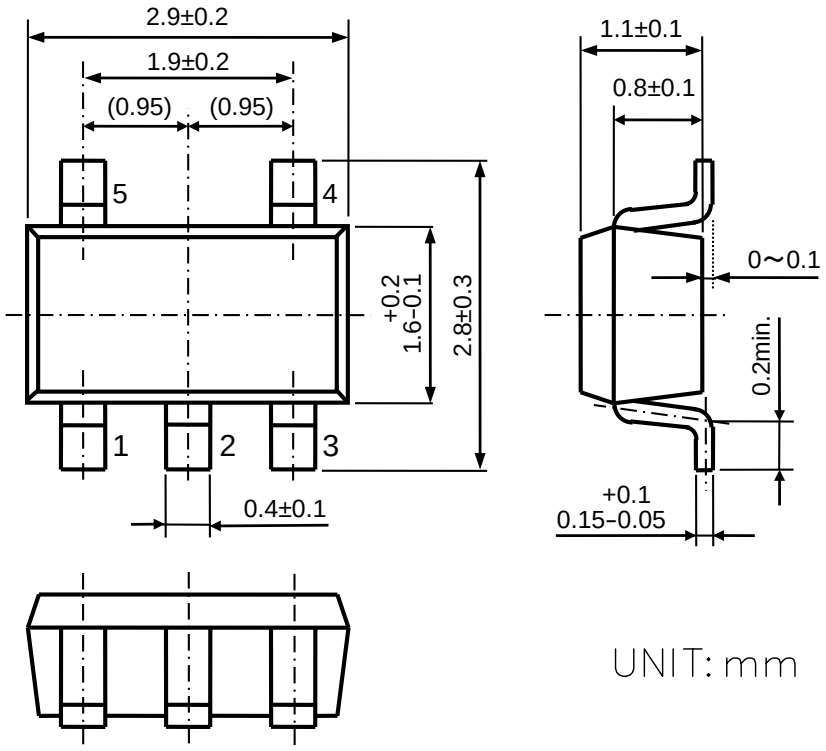
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



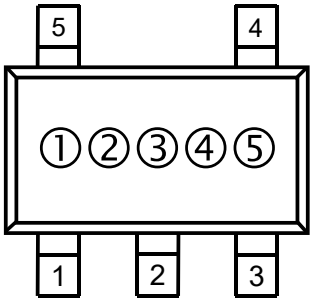
Measurement Board Pattern



SOT-23-5 Package Dimensions

①②③: Product Code ⋯ Refer to *Part Marking List*

④⑤: Lot Number ⋯ Alphanumeric Serial Number



SOT-23-5 Part Markings

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

RP105N Part Marking List

RP105NxxxB

Product Name	①	②	③	V_{SET}
RP105N061B	R	0	A	0.6 V
RP105N071B	R	0	B	0.7 V
RP105N081B	R	0	C	0.8 V
RP105N091B	R	0	D	0.9 V
RP105N101B	R	0	E	1.0 V
RP105N121B	R	0	F	1.2 V
RP105N131B	R	0	G	1.3 V
RP105N141B	R	0	H	1.4 V
RP105N151B	R	0	J	1.5 V
RP105N111B	R	0	K	1.1 V

RP105NxxxD

Product Name	①	②	③	V_{SET}
RP105N061D	R	1	A	0.6 V
RP105N071D	R	1	B	0.7 V
RP105N081D	R	1	C	0.8 V
RP105N091D	R	1	D	0.9 V
RP105N101D	R	1	E	1.0 V
RP105N121D	R	1	F	1.2 V
RP105N131D	R	1	G	1.3 V
RP105N141D	R	1	H	1.4 V
RP105N151D	R	1	J	1.5 V
RP105N111D	R	1	K	1.1 V

RP105NxxxE

Product Name	①	②	③	V_{SET}
RP105N061E	R	2	A	0.6 V
RP105N071E	R	2	B	0.7 V
RP105N081E	R	2	C	0.8 V
RP105N091E	R	2	D	0.9 V
RP105N101E	R	2	E	1.0 V
RP105N121E	R	2	F	1.2 V
RP105N131E	R	2	G	1.3 V
RP105N141E	R	2	H	1.4 V
RP105N151E	R	2	J	1.5 V
RP105N111E	R	2	K	1.1 V

RP105NxxxF

Product Name	①	②	③	V_{SET}
RP105N061F	R	3	A	0.6 V
RP105N071F	R	3	B	0.7 V
RP105N081F	R	3	C	0.8 V
RP105N091F	R	3	D	0.9 V
RP105N101F	R	3	E	1.0 V
RP105N121F	R	3	F	1.2 V
RP105N131F	R	3	G	1.3 V
RP105N141F	R	3	H	1.4 V
RP105N151F	R	3	J	1.5 V
RP105N111F	R	3	K	1.1 V

PD-DFN1212-5-JEDEC(85125)-D-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

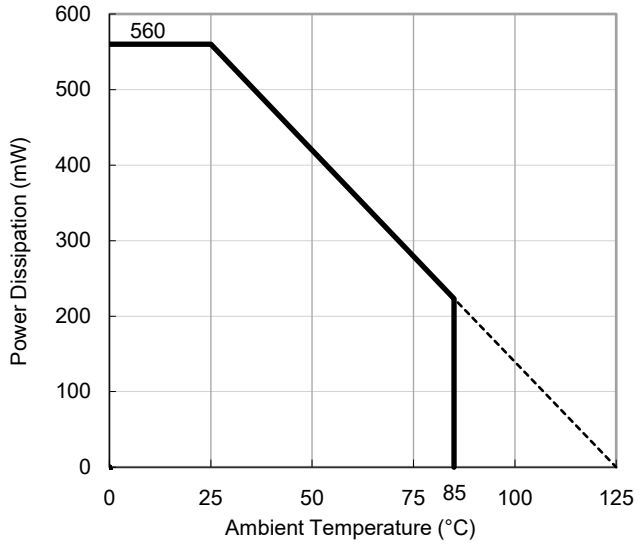
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.2 mm × 14 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

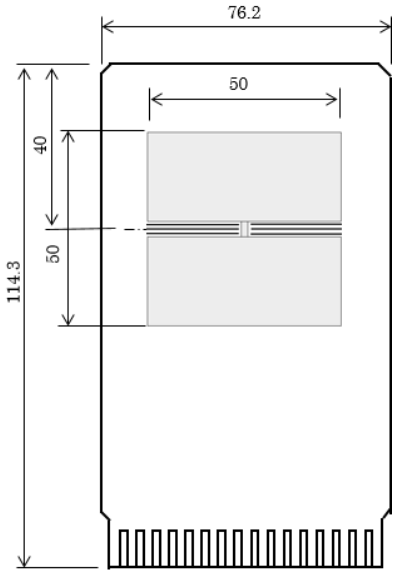
Item	Measurement Result
Power Dissipation	560 mW
Thermal Resistance (θja)	θja = 178°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 105°C/W

θja: Junction-to-Ambient Thermal Resistance

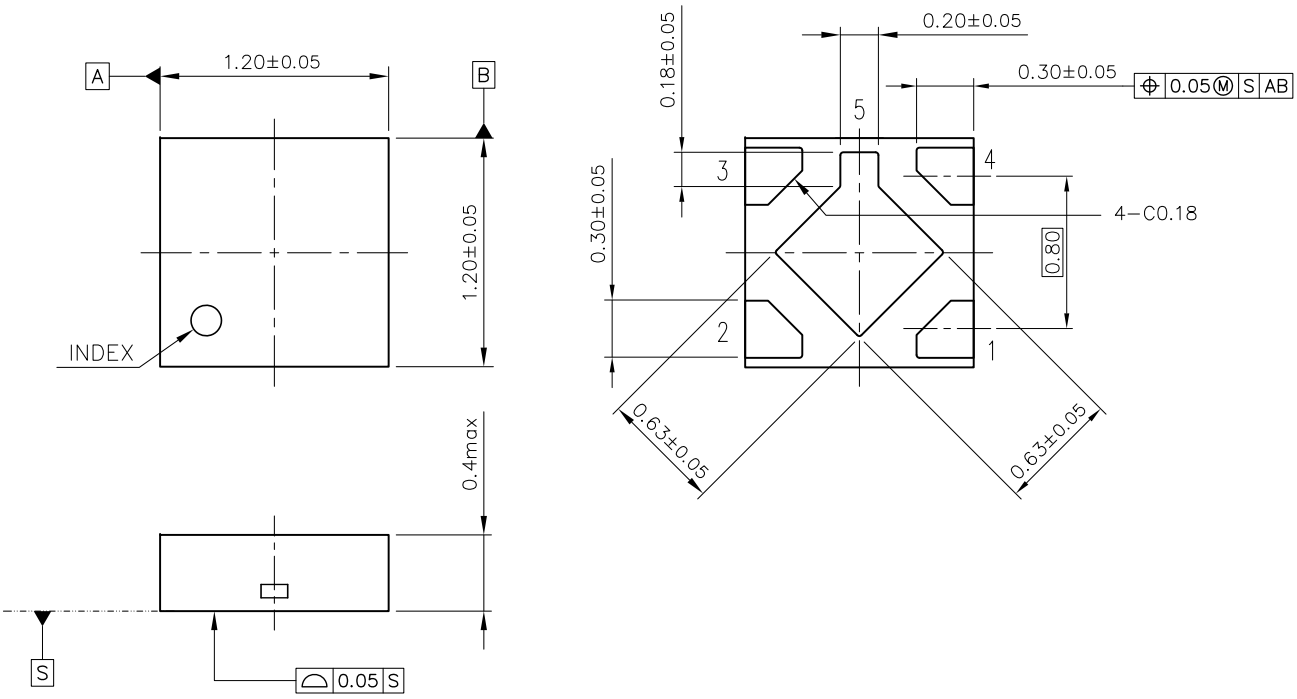
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



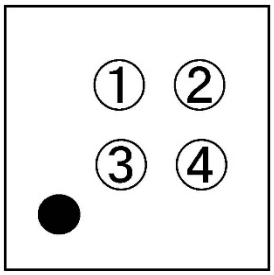
Measurement Board Pattern



DFN1212-5 Package Dimensions (Unit: mm)

①②: Product Code ⋯ Refer to *Part Marking List*

③④: Lot Number ⋯ Alphanumeric Serial Number



DFN1212-5 Part Markings

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

RP105L Part Marking List

RP105LxxxB

Product Name	① ②	V_{SET}
RP105L061B	T A	0.6 V
RP105L071B	T B	0.7 V
RP105L071B5	T N	0.75V
RP105L081B	T C	0.8 V
RP105L091B	T D	0.9 V
RP105L091B5	T M	0.95 V
RP105L101B	T E	1.0 V
RP105L101B5	T L	1.05 V
RP105L111B	T F	1.1 V
RP105L121B	T G	1.2 V
RP105L131B	T H	1.3 V
RP105L141B	T J	1.4 V
RP105L151B	T K	1.5 V

RP105LxxxD

Product Name	① ②	V_{SET}
RP105L061D	U A	0.6 V
RP105L071D	U B	0.7 V
RP105L071D5	U N	0.75V
RP105L081D	U C	0.8 V
RP105L091D	U D	0.9 V
RP105L091D5	U M	0.95 V
RP105L101D	U E	1.0 V
RP105L101D5	U L	1.05 V
RP105L111D	U F	1.1 V
RP105L121D	U G	1.2 V
RP105L131D	U H	1.3 V
RP105L141D	U J	1.4 V
RP105L151D	U K	1.5 V

RP105LxxxE

Product Name	① ②	V_{SET}
RP105L061E	V A	0.6 V
RP105L071E	V B	0.7 V
RP105L071E5	V N	0.75V
RP105L081E	V C	0.8 V
RP105L091E	V D	0.9 V
RP105L091E5	V M	0.95 V
RP105L101E	V E	1.0 V
RP105L101E5	V L	1.05 V
RP105L111E	V F	1.1 V
RP105L121E	V G	1.2 V
RP105L131E	V H	1.3 V
RP105L141E	V J	1.4 V
RP105L151E	V K	1.5 V

RP105LxxxF

Product Name	① ②	V_{SET}
RP105L061F	W A	0.6 V
RP105L071F	W B	0.7 V
RP105L071F5	W N	0.75V
RP105L081F	W C	0.8 V
RP105L091F	W D	0.9 V
RP105L091F5	W M	0.95 V
RP105L101F	W E	1.0 V
RP105L101F5	W L	1.05 V
RP105L111F	W F	1.1 V
RP105L121F	W G	1.2 V
RP105L131F	W H	1.3 V
RP105L141F	W J	1.4 V
RP105L151F	W K	1.5 V

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    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
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    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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