N-Channel 2.5-V (G-S) MOSFET

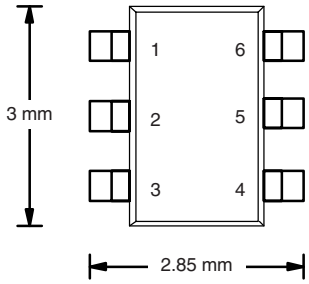
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.057 at V_{GS} = 4.5 V	4.2
	0.090 at V_{GS} = 2.5 V	3.4

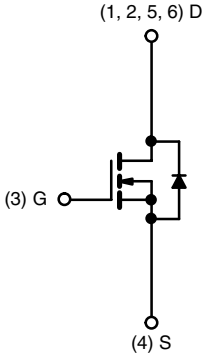
FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

TSOP-6
Top View





N-Channel MOSFET

Ordering Information: Si3442BDV-T1-E3 (Lead (Pb)-free)
Si3442BDV-T1-GE3 (Lead (Pb)-free and Halogen-free)

Marking Code: 2Bxxx

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**5 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	4.2	3.0	A
	T_A = 70 °C		3.4	2.4	
Pulsed Drain Current		I_{DM}	20		
Continuous Source Current (Diode Conduction)[a]		I_S	1.4	0.72	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	1.67	0.86	W
	T_A = 70 °C		1.07	0.55	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	75	100	°C/W
	Steady State		120	145	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	70	85	

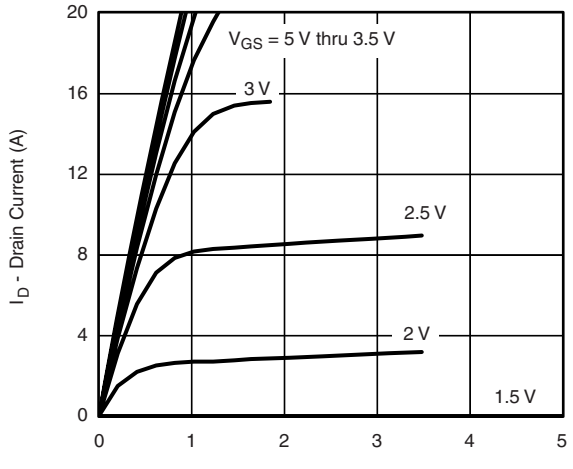
Note:
a. Surface Mounted on FR4 board, t ≤ 5 s.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.6		1.8	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	10			A
		V_{DS} = 5 V, V_{GS} = 2.5 V	4			
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4 A		0.045	0.057	Ω
		V_{GS} = 2.5 V, I_D = 3.4 A		0.070	0.090	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.0 A		11.3		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.6 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		295		pF
Output Capacitance	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			45		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.0 A		3	5	nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			0.95		
Gate Resistance	R_g	f = 1 MHz		2.7		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_g = 6 Ω		35	55	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.6 A, dI/dt = 100 A/µs		30	60	

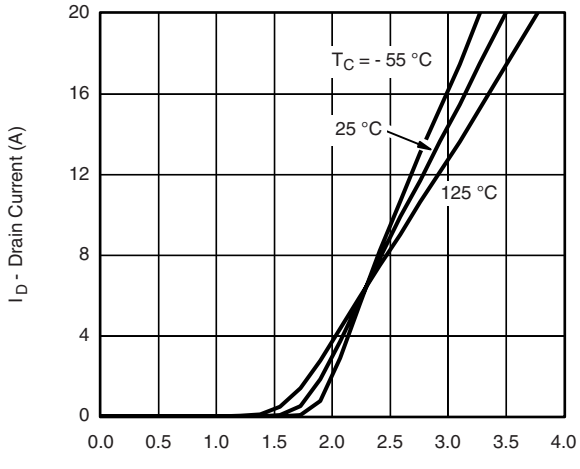
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

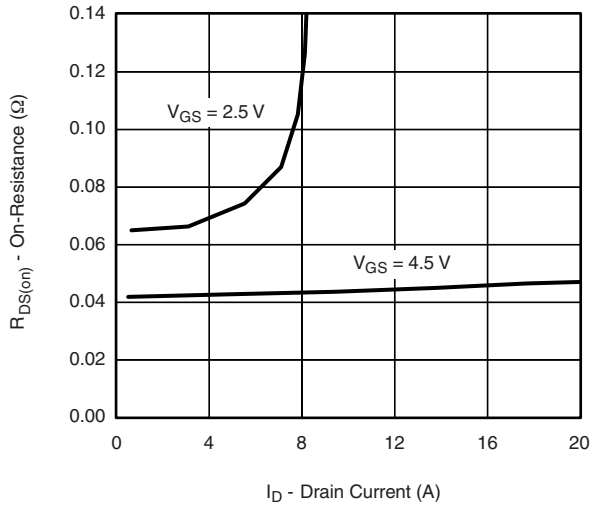


Output Characteristics

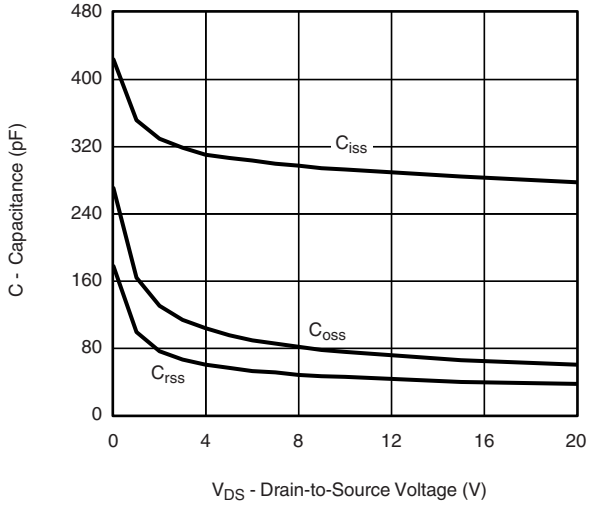


Transfer Characteristics

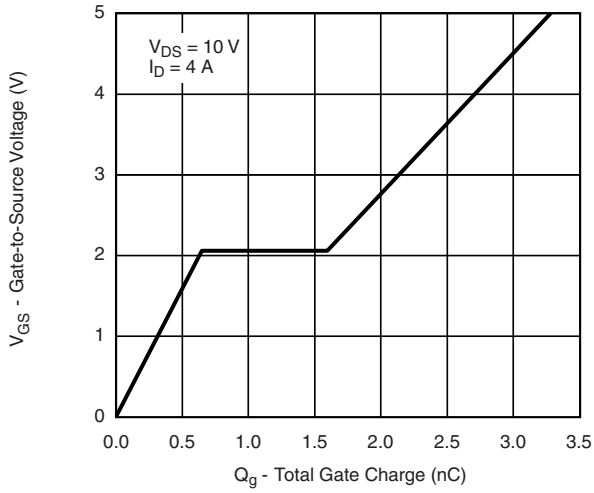
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



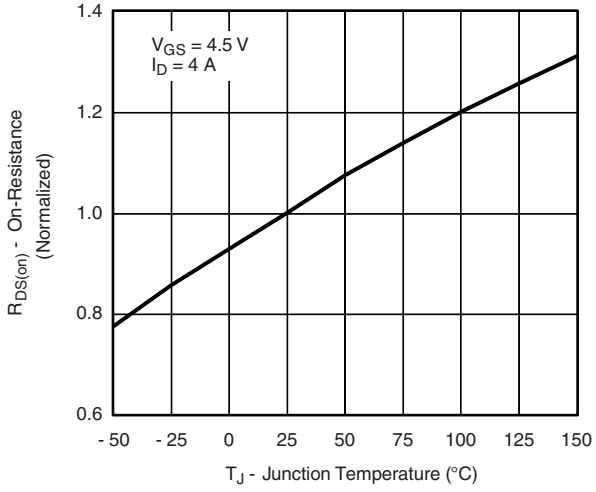
On-Resistance vs. Drain Current



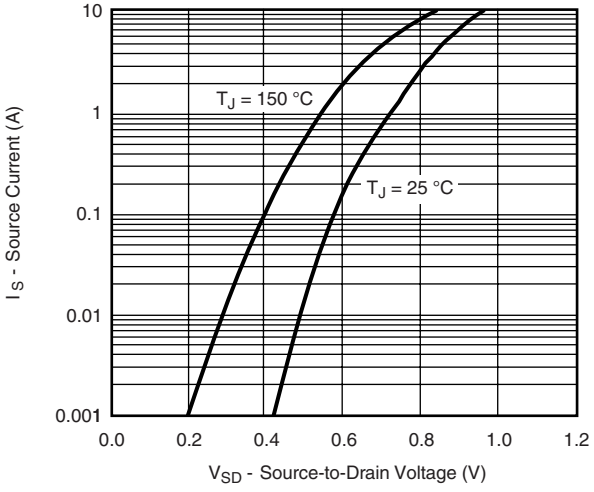
Capacitance



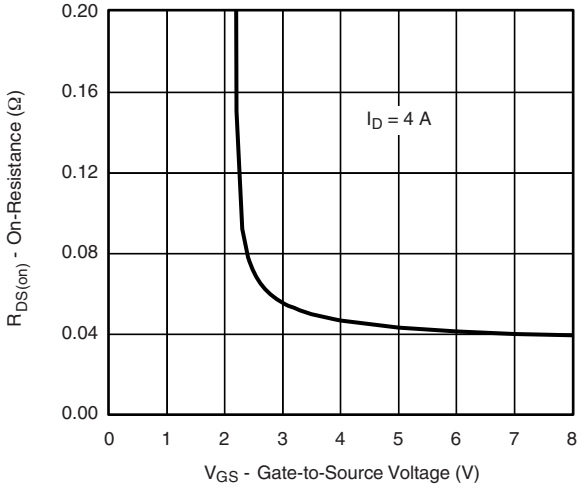
Gate Charge



On-Resistance vs. Junction Temperature

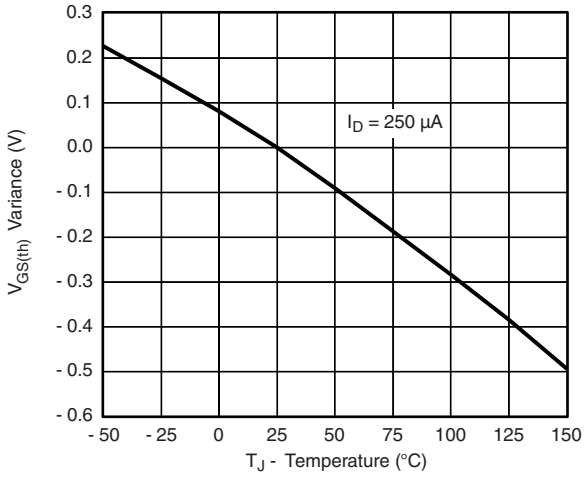


Source-Drain Diode Forward Voltage

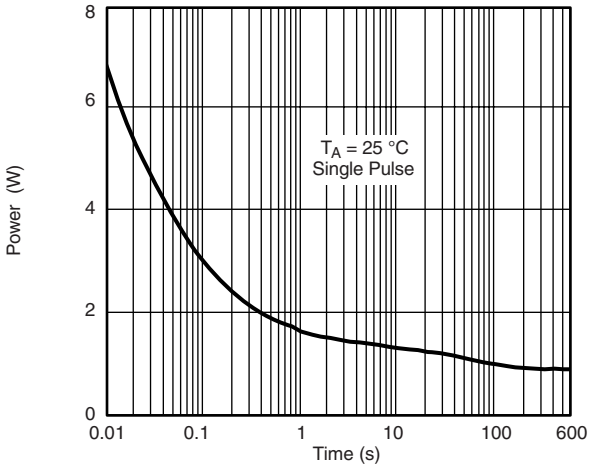


On-Resistance vs. Gate-to-Source Voltage

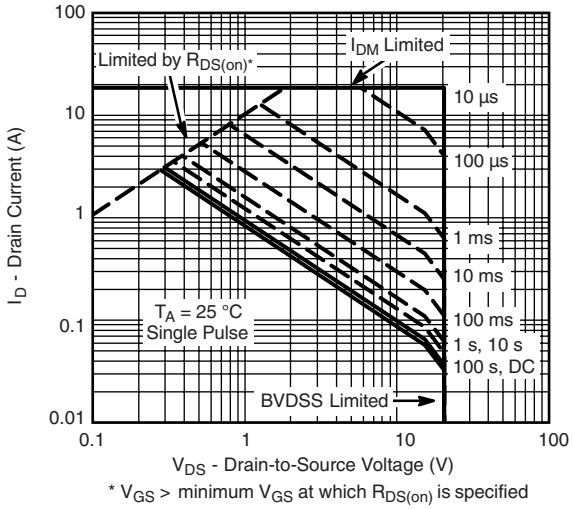
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Threshold Voltage

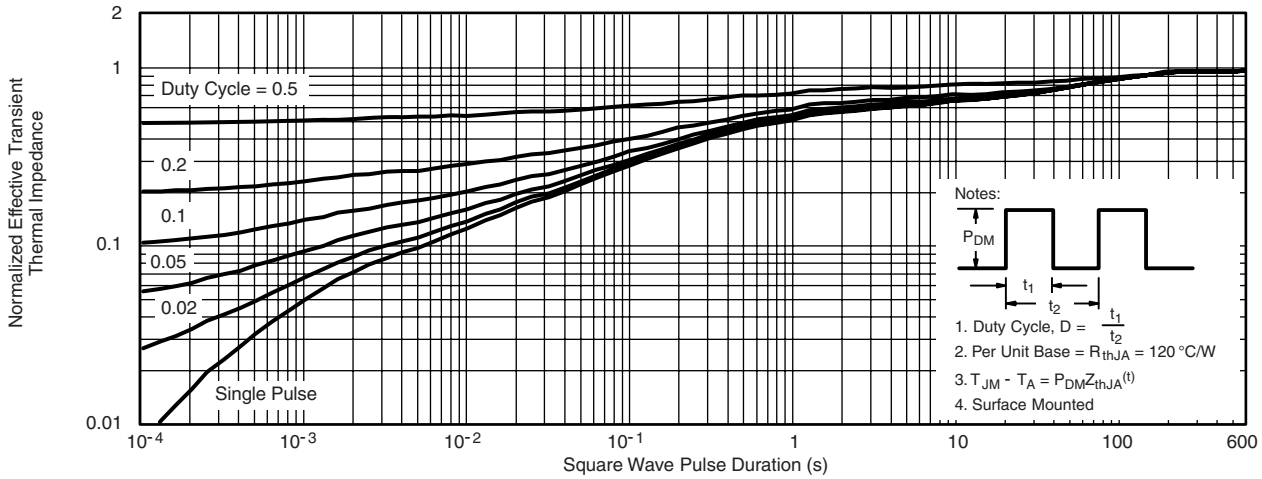


Single Pulse Power



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

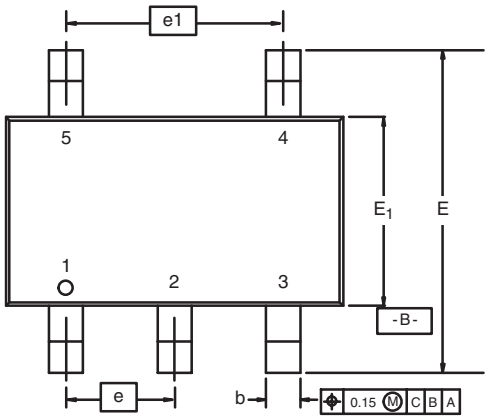
Safe Operating Area



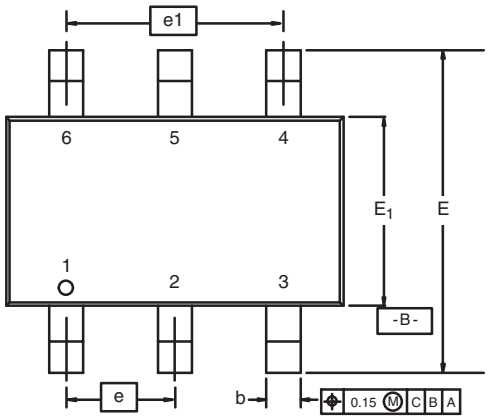
Normalized Thermal Transient Impedance, Junction-to-Ambient

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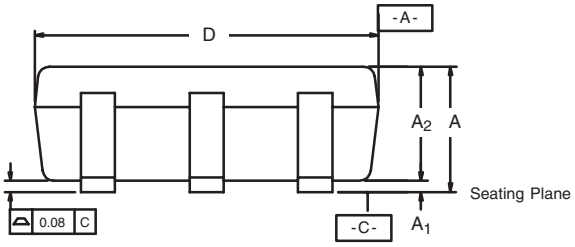
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

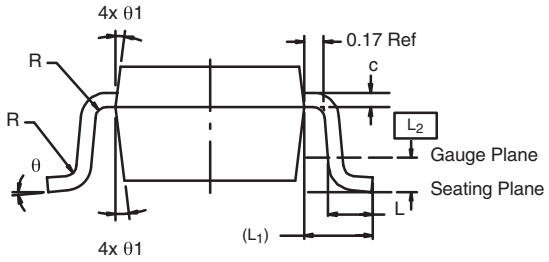


5-LEAD TSOP



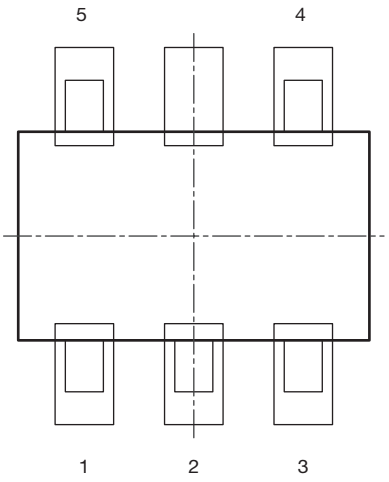
6-LEAD TSOP



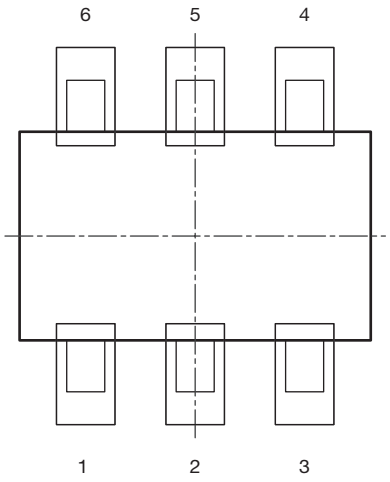


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

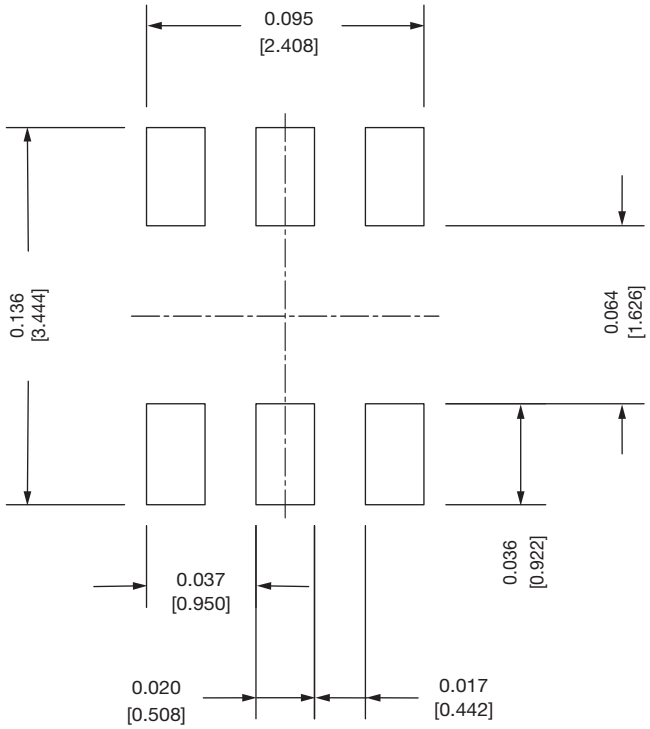
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010

For technical questions, contact: pmostechsupport@vishay.com

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