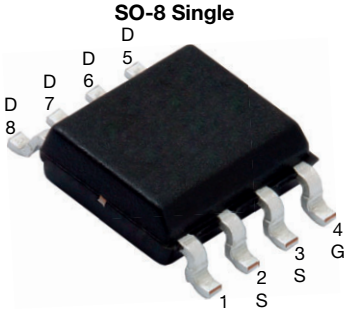
P-Channel 30 V (D-S) MOSFET

SO-8 Single



Top View

FEATURES

- Extended V_{GS} range (± 25 V) for adaptor switch applications
- Extremely low $R_{DS(on)}$
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Typical ESD performance: 4000 V (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

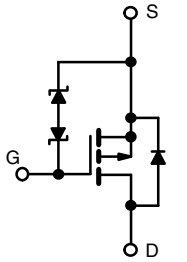
Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Adaptor switch, load switch
- Power management
- Notebook computers and portable battery packs



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0065
$R_{DS(on)}$ max. (Ω) at V_{GS} = -6 V	0.0082
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.0112
Q_g typ. (nC)	66
I_D (A) [a]	-29
Configuration	Single

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	Si4491EDY-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 25	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	-25.8	A
	T_C = 70 °C		-20.7	
	T_A = 25 °C		-17.3	
	T_A = 70 °C		-13.9 [b, c]	
Pulsed drain current (t = 300 µs)		I_{DM}	-60	
Continuous source-drain diode current	T_C = 25 °C	I_S	-5.8 [b, c]	
	T_A = 25 °C		-2.6 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	-40	
Single pulse avalanche energy		E_{AS}	80	mJ
Maximum power dissipation	T_C = 25 °C	P_D	6.9	W
	T_C = 70 °C		4.4	
	T_A = 25 °C		3.1 [b, c]	
	T_A = 70 °C		2 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, d]	t ≤ 10 s	R_{thJA}	33	40	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	15	17	

Notes

a. Based on T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. Maximum under steady state conditions is 90 °C/W

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-30	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-24	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	6	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = -250 µA	-1.2	-	-2.8	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 25 V	-	-	± 150	µA
		V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 15	
Zero gate voltage drain current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	-	-	-1	
		V_{DS} = -30 V, V_{GS} = 0 V, T_J = 55 °C	-	-	-10	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \leq$ -5 V, V_{GS} = -10 V	-20	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -13 A	-	0.0054	0.0065	Ω
		V_{GS} = -6 V, I_D = -10 A	-	0.0068	0.0082	
		V_{GS} = -4.5 V, I_D = -8 A	-	0.0093	0.0112	
Forward transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -13 A	-	44	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	-	4620	-	pF
Output capacitance	C_{oss}		-	880	-	
Reverse transfer capacitance	C_{rss}		-	820	-	
Total gate charge	Q_g	V_{DS} = -15 V, V_{GS} = -10 V, I_D = -17.3 A	-	102	153	nC
		V_{DS} = -15 V, V_{GS} = -5 V, I_D = -17.3 A	-	66	80	
Gate-source charge	Q_{gs}		-	16	-	
Gate-drain charge	Q_{gd}		-	28	-	
Gate resistance	R_g	f = 1 MHz	0.3	1.3	2.6	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 0 V, R_L = 1.5 Ω, $I_D \cong$ -10 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	70	105	ns
Rise time	t_r		-	70	105	
Turn-off delay time	$t_{d(off)}$		-	45	68	
Fall time	t_f		-	27	41	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -15 V, R_L = 1.5 Ω, $I_D \cong$ -10 A, V_{GEN} = -10 V, R_g = 1 Ω	-	18	30	
Rise time	t_r		-	15	25	
Turn-off delay time	$t_{d(off)}$		-	52	80	
Fall time	t_f		-	14	25	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	-5.8	A
Pulse diode forward current	I_{SM}		-	-	-60	
Body diode Voltage	V_{SD}	I_S = -10 A, V_{GS} = 0 V	-	-0.78	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -10 A, di/dt = 100 A/µs, T_J = 25 °C		35	53	ns
Body diode reverse recovery charge	Q_{rr}			25	38	nC
Reverse recovery fall time	t_a			19		ns
Reverse recovery rise time	t_b			16		

Notes

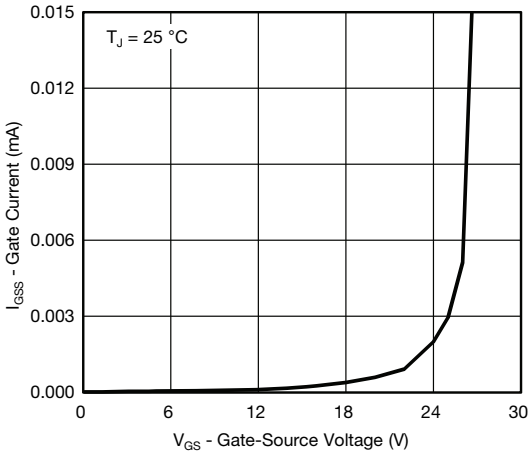
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

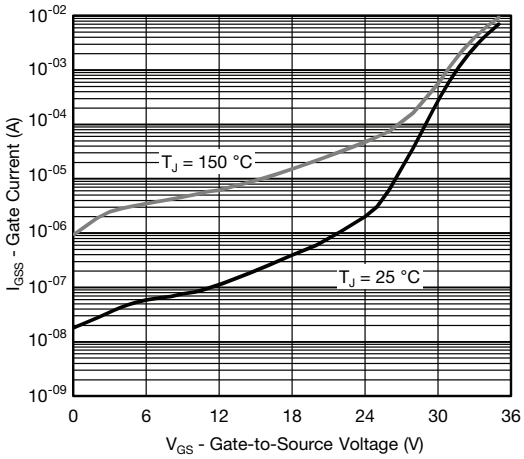
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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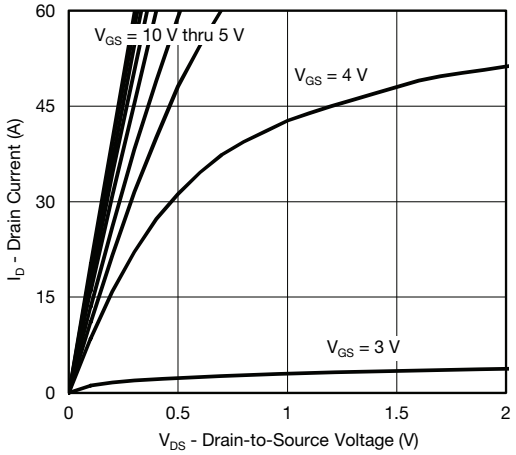
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



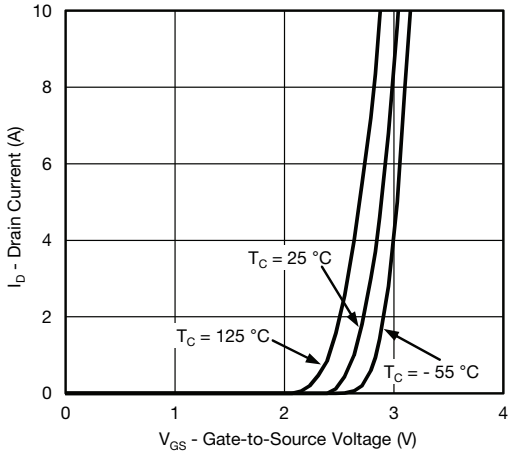
Gate Current vs. Gate-Source Voltage



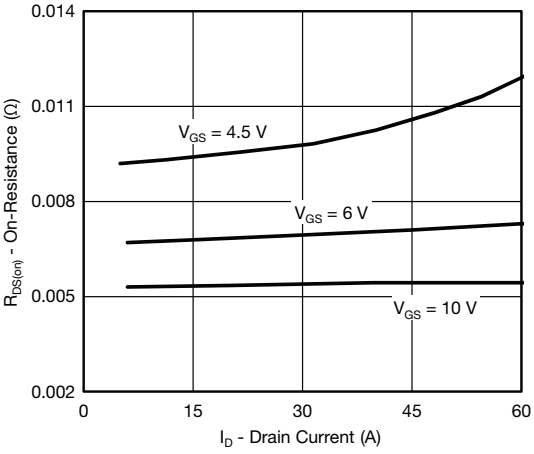
Gate Current vs. Gate-Source Voltage



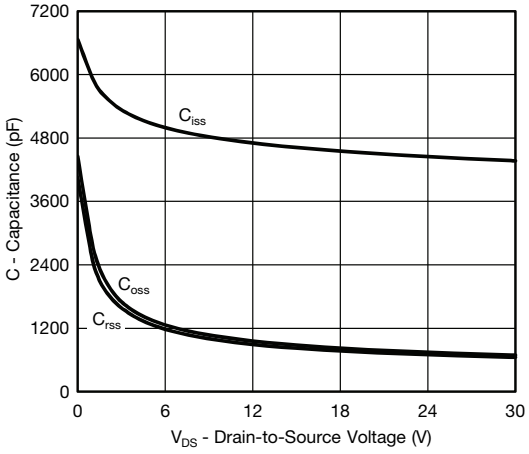
Output Characteristics



Transfer Characteristics



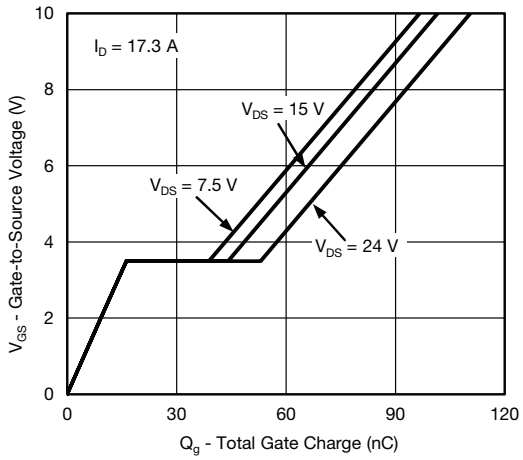
On-Resistance vs. Drain Current



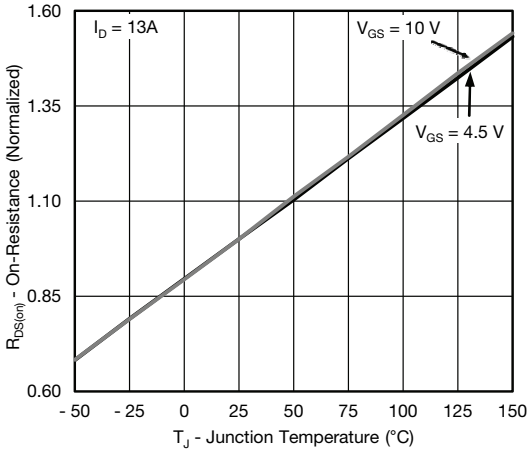
Capacitance

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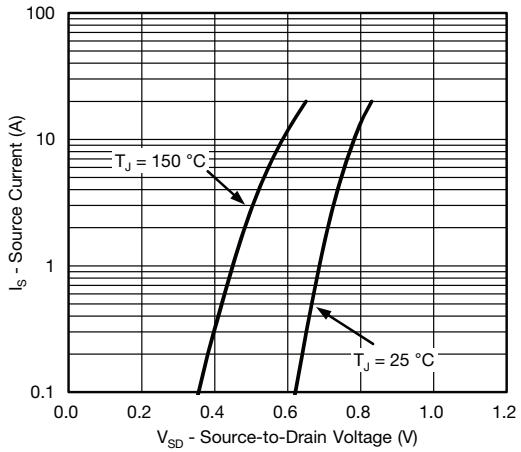
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



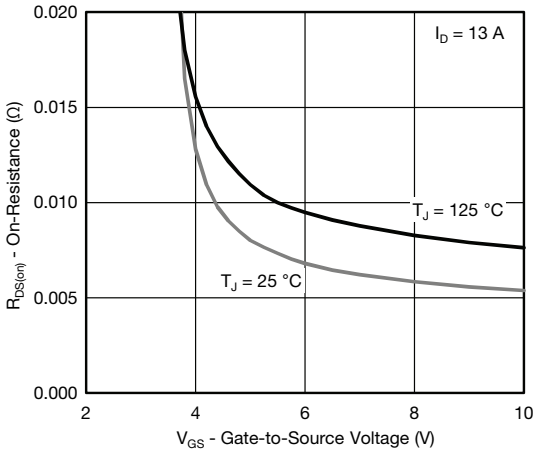
Gate Charge



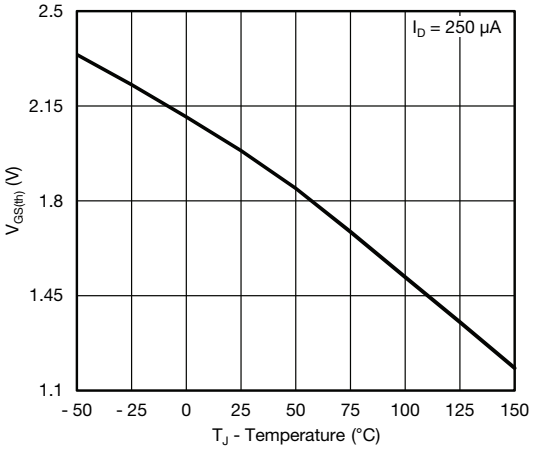
On-Resistance vs. Junction Temperature



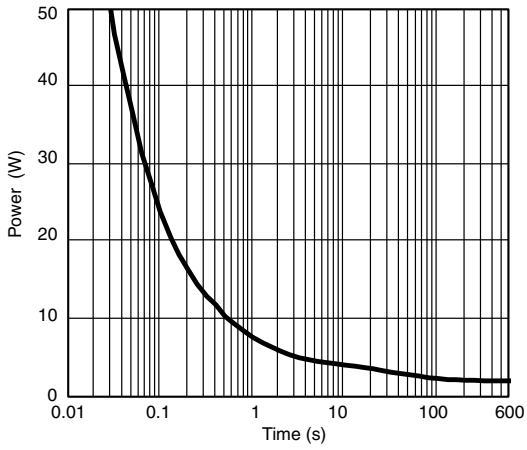
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



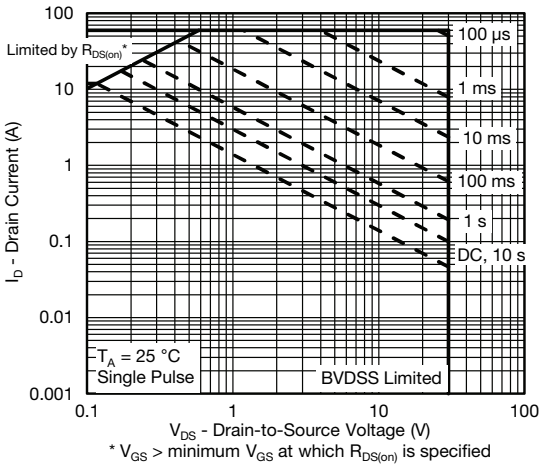
Threshold Voltage



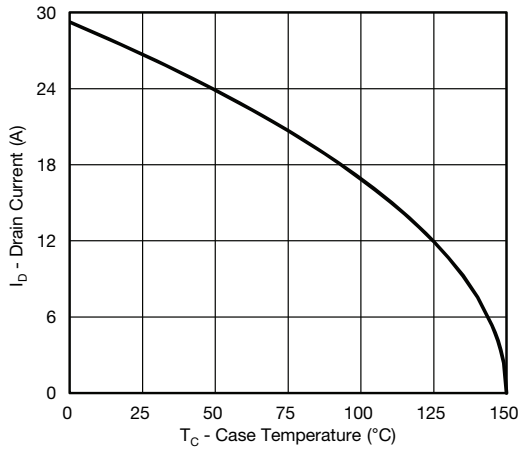
Single Pulse Power, Junction-to-Ambient

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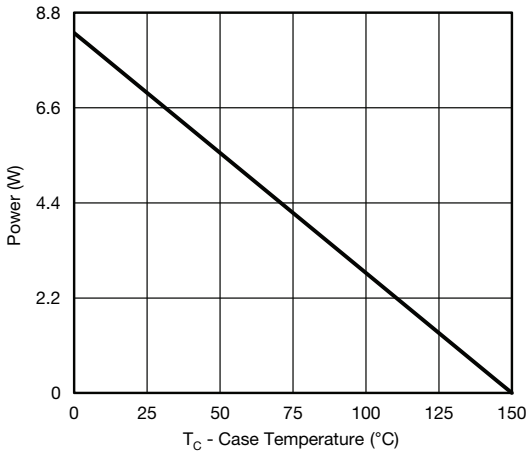
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



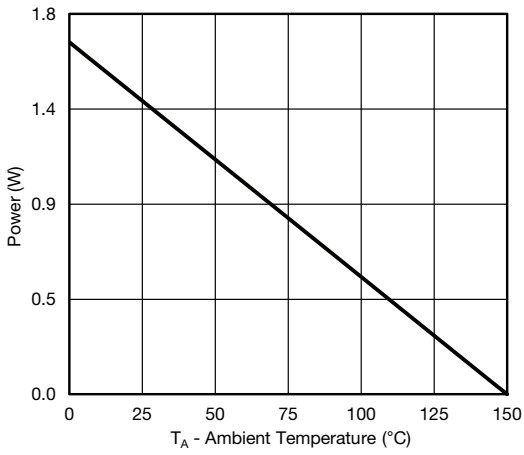
Safe Operating Area, Junction-to-Ambient



Current Derating [a]



Power Junction-to-Foot



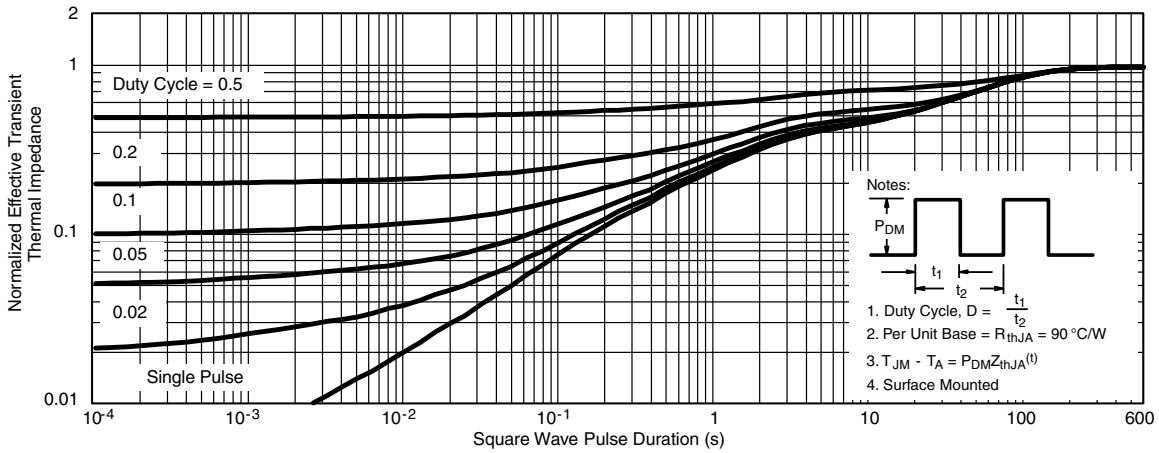
Power Junction-to-Ambient

Note

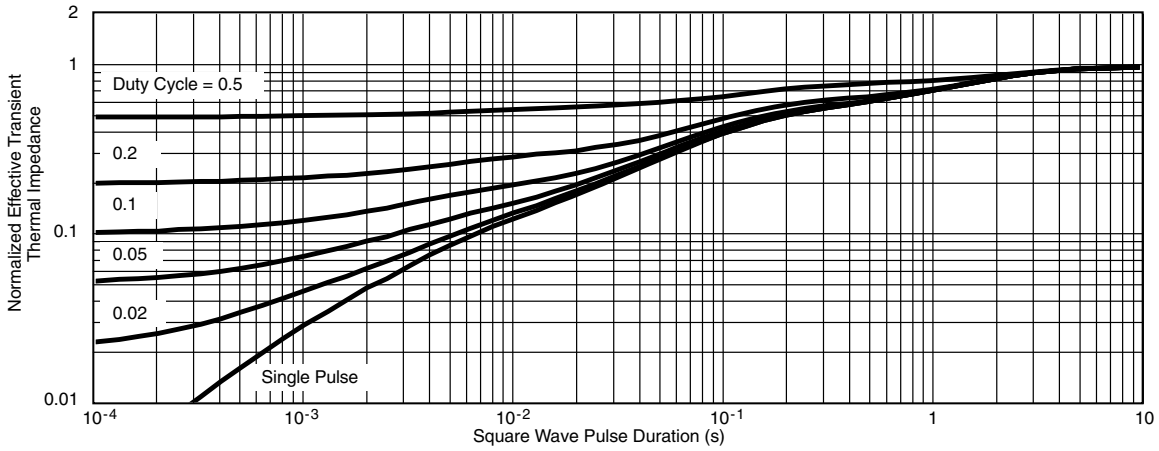
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



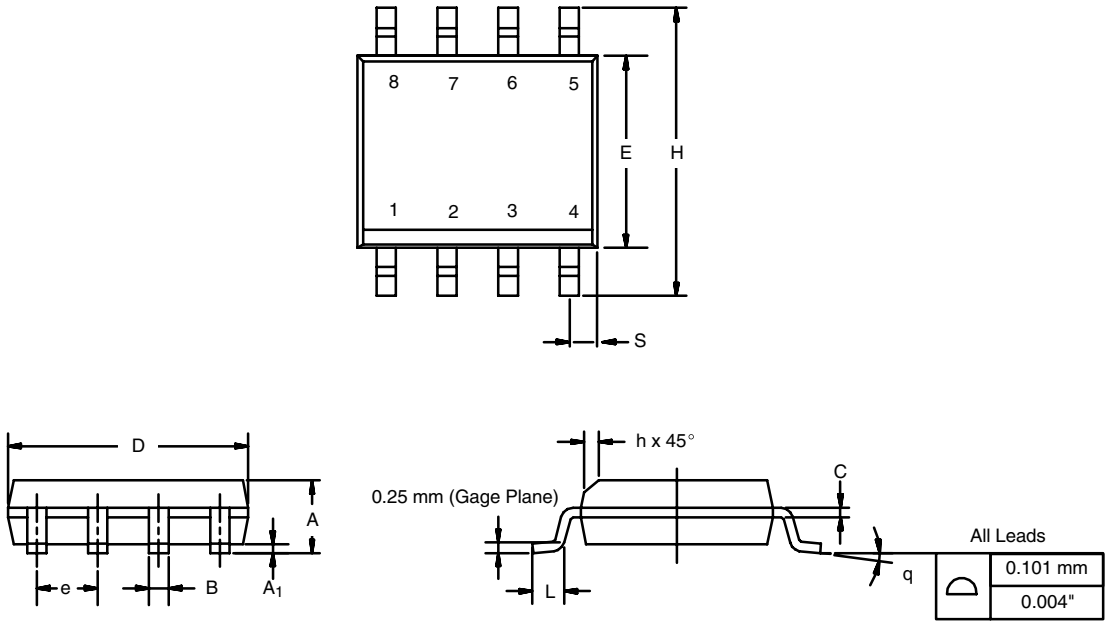
Normalized Thermal Transient Impedance, Junction-to-Foot

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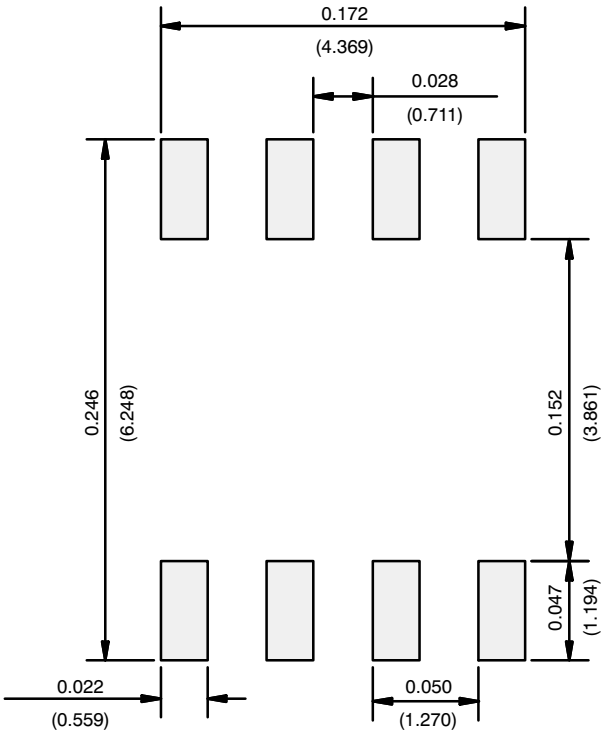
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SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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