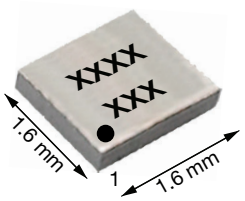
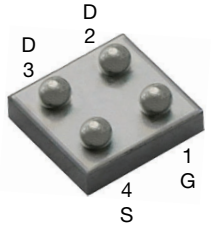
P-Channel 20 V (D-S) MOSFET

MICRO FOOT® 1.6 x 1.6



Backside View



Bump Side View

FEATURES

- TrenchFET® Gen III p-channel power MOSFET
- Low 0.6 mm maximum height
- Low on-resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

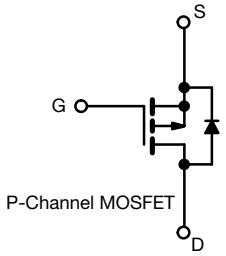
Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Load switch
  - With low voltage drop
- Power management in battery-operated, mobile, and wearable devices



PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.021
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	0.025
$R_{DS(on)}$ max. (Ω) at V_{GS} = -1.8 V	0.039
Q_g typ. (nC)	31.2
I_D (A)	-9.7 [a]
Configuration	Single

ORDERING INFORMATION	
Package	MICRO FOOT
Lead (Pb)-free and halogen-free	Si8481DB-T1-E1

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current (T_J = 150 °C)	T_A = 25 °C	I_D	-9.7 [a]	A
	T_A = 70 °C		-7.8 [a]	
	T_A = 25 °C		-6.2 [b]	
	T_A = 70 °C		-5 [b]	
Pulsed drain current (t = 100 µs)		I_{DM}	-30	
Continuous source-drain diode current	T_A = 25 °C	I_S	-2.3 [a]	
	T_A = 70 °C		-0.92 [b]	
Maximum power dissipation	T_A = 25 °C	P_D	2.8 [a]	W
	T_A = 70 °C		1.8 [a]	
	T_A = 25 °C		1.1 [b]	
	T_A = 70 °C		0.73 [b]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Package reflow conditions [c]		VPR	260	
		IR / convection		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a, f]	t = 5 s	R_{thJA}	35	45	°C/W
Maximum junction-to-ambient [b, g]			85	110	

Notes

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC / JEDEC® (J-STD-020), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on T_A = 25 °C.
f. Maximum under steady state conditions is 85 °C/W.
g. Maximum under steady state conditions is 175 °C/W.

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-13	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	2.5	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-	-0.9	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	-	-	-1	µA
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	-10	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \leq$ -5 V, V_{GS} = -4.5 V	-5	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D = -3 A	-	0.017	0.021	Ω
		V_{GS} = -2.5 V, I_D = -3 A	-	0.020	0.025	
		V_{GS} = -1.8 V, I_D = -1 A	-	0.026	0.039	
Forward transconductance[a]	g_{fs}	V_{DS} = -5 V, I_D = -3 A	-	22	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	-	2500	-	pF
Output capacitance	C_{oss}		-	320	-	
Reverse transfer capacitance	C_{rss}		-	260	-	
Total gate charge	Q_g	V_{DS} = -10 V, V_{GS} = -8 V, I_D = -3 A	-	54	81	nC
		V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -3 A	-	31.2	47	
Gate-source charge	Q_{gs}	V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -3 A	-	2.7	-	
Gate-drain charge	Q_{gd}		-	6.3	-	
Gate resistance	R_g	f = 1 MHz	-	17	-	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 3.3 Ω, $I_D \cong$ -3 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	16	30	ns
Rise time	t_r		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	300	600	
Fall time	t_f		-	110	220	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 3.3 Ω, $I_D \cong$ -3 A, V_{GEN} = -8 V, R_g = 1 Ω	-	7	15	
Rise time	t_r		-	20	40	
Turn-off delay time	$t_{d(off)}$		-	400	800	
Fall time	t_f		-	110	220	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_A = 25 °C	-	-	-2.3 [c]	A
Pulse diode forward current	I_{SM}		-	-	-15	
Body diode voltage	V_{SD}	I_S = -3 A, V_{GS} = 0 V	-	-0.8	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -3 A, dI/dt = 100 A/µs, T_J = 25 °C	-	150	300	ns
Body diode reverse recovery charge	Q_{rr}		-	235	470	nC
Reverse recovery fall time	t_a		-	47	-	ns
Reverse recovery rise time	t_b		-	103	-	

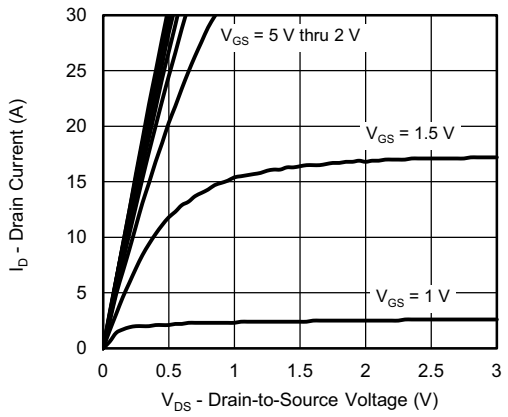
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.

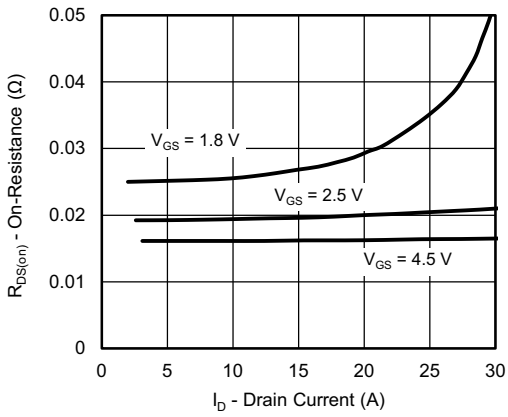
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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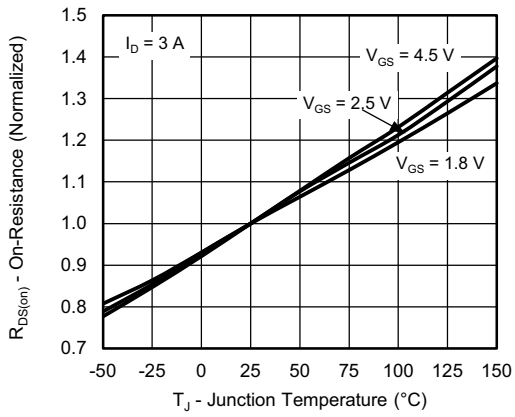
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



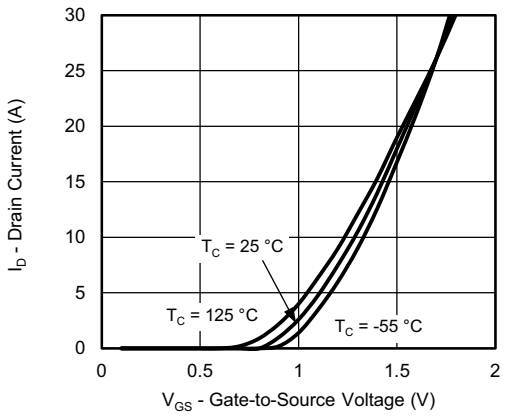
Output Characteristics



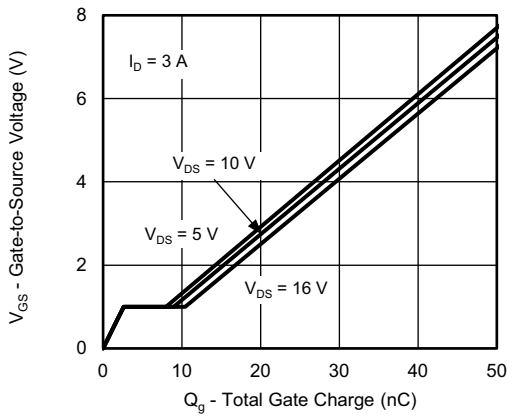
On-Resistance vs. Drain Current and Gate Voltage



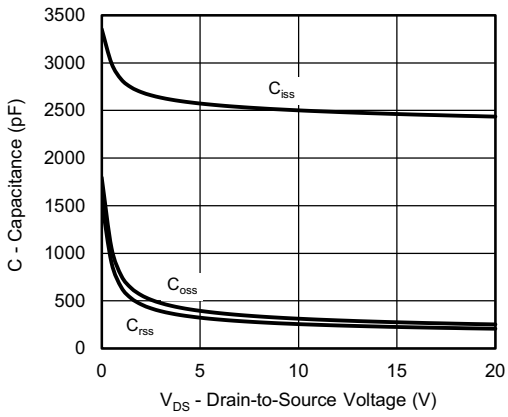
On-Resistance vs. Junction Temperature



Transfer Characteristics



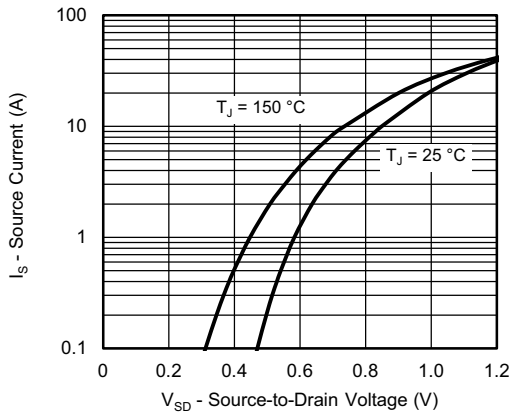
Gate Charge



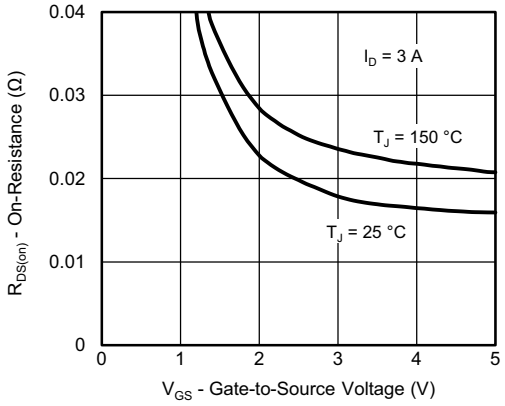
Capacitance

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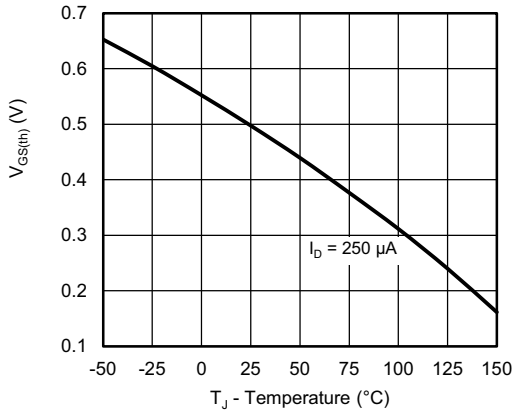
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



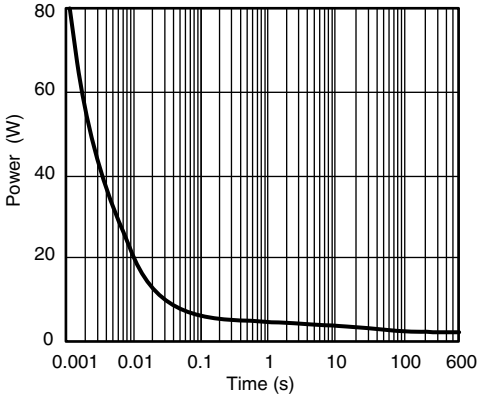
Source-Drain Diode Forward Voltage



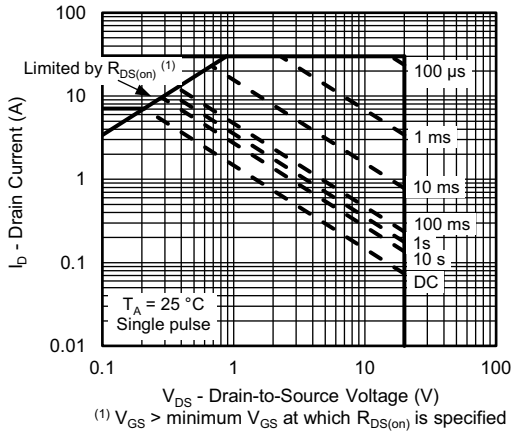
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



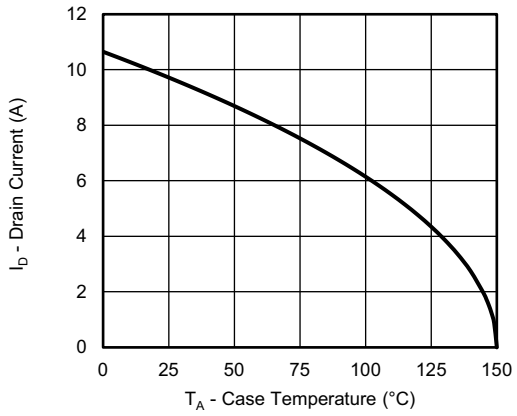
Single Pulse Power, Junction-to-Ambient



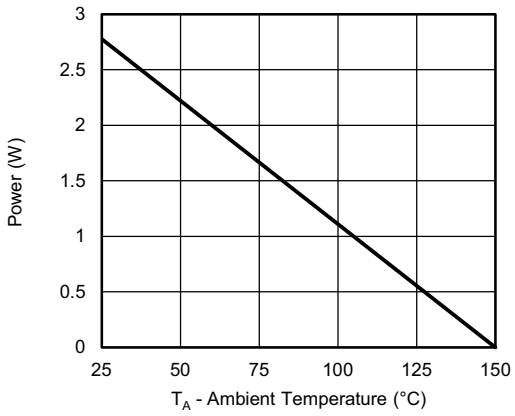
Safe Operating Area, Junction-to-Ambient

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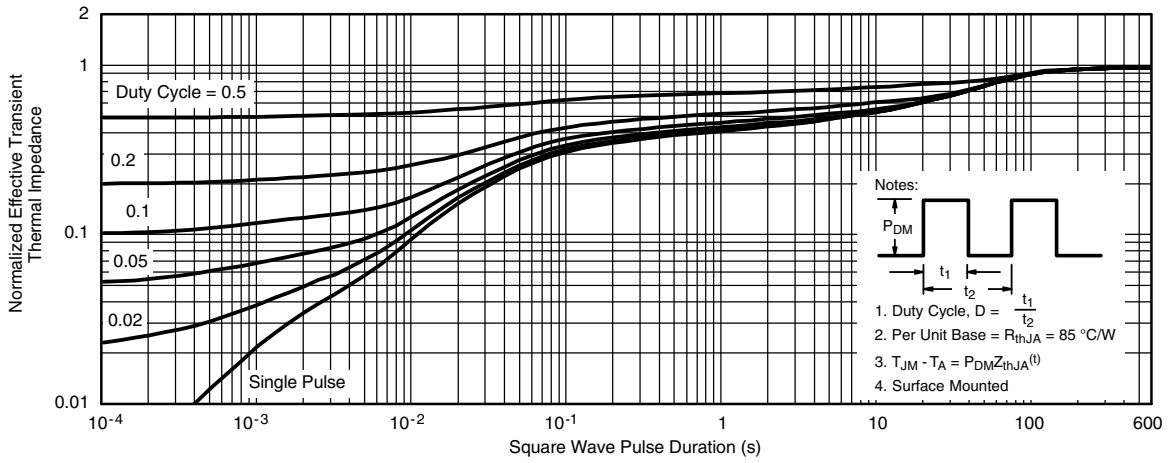
Current Derating [a]



Power, Junction-to-Ambient [a]

Note

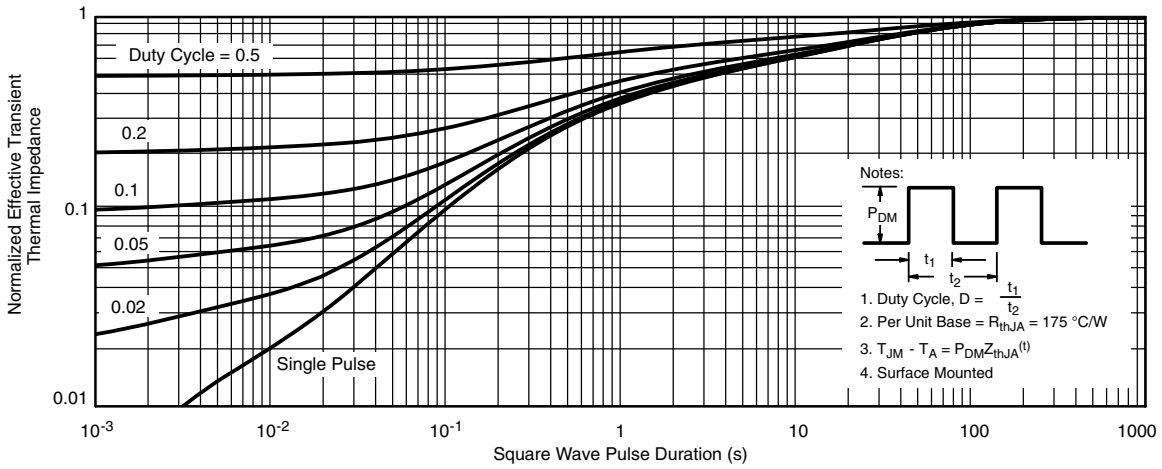
a. When surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)

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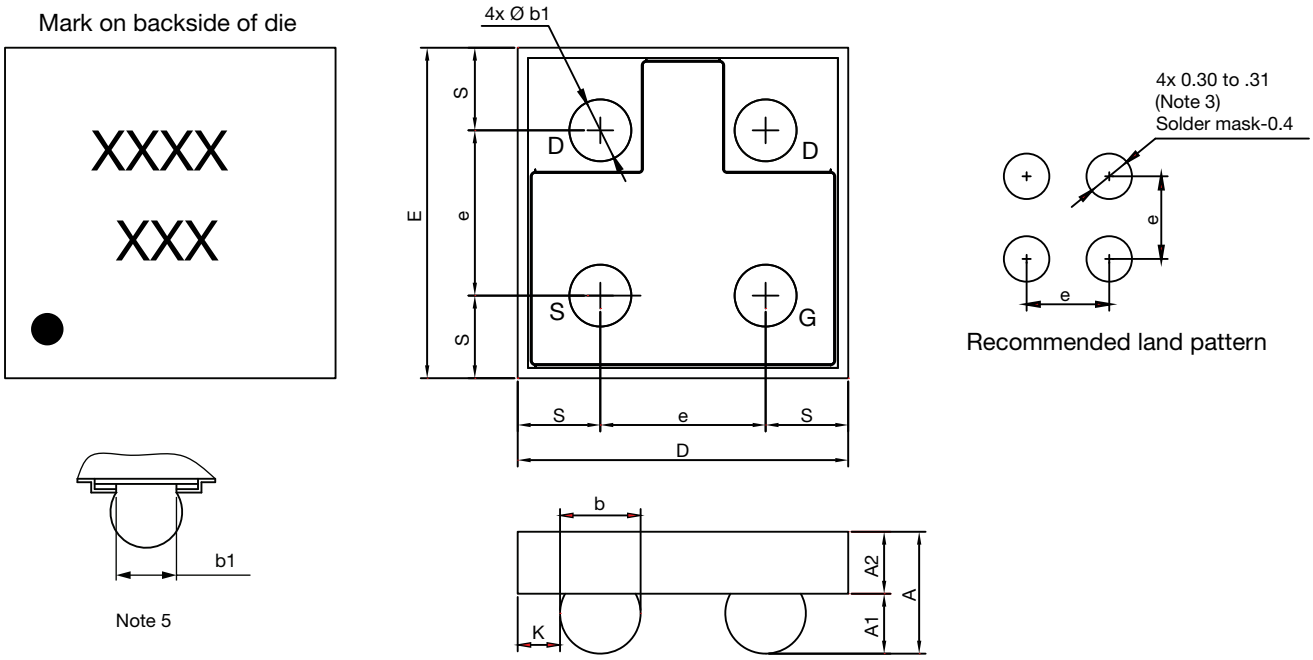


Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)

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MICRO FOOT®: 4-Bumps
(1.6 mm x 1.6 mm, 0.8 mm Pitch, 0.290 mm Bump Height)



Notes

1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. “b1” is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.550	0.575	0.600	0.0217	0.0226	0.0236
A1	0.260	0.275	0.290	0.0102	0.0108	0.0114
A2	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.370	0.390	0.410	0.0146	0.0153	0.0161
b1		0.300			0.0118	
e		0.800			0.0314	
s	0.360	0.380	0.400	0.0141	0.0150	0.0157
D	1.520	1.560	1.600	0.0598	0.0614	0.0630
E	1.520	1.560	1.600	0.0598	0.0614	0.0630
K	0.155	0.185	0.215	0.0061	0.0073	0.0085

Note

- Use millimeters as the primary measurement.

ECN: T15-0175-Rev. A, 27-Apr-15
DWG: 6038

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