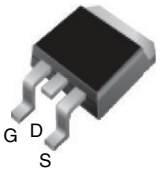
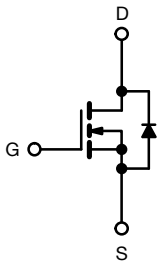
Power MOSFET

D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor forward

PRODUCT SUMMARY		
V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1.2
Q_g max. (nC)	42	
Q_{gs} (nC)	10	
Q_{gd} (nC)	20	
Configuration	Single	

ORDERING INFORMATION			
Package	D²PAK (TO-263)	D²PAK (TO-263)	D²PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHFBC40AS-GE3	SiHFBC40ASTRL-GE3 [a]	SiHFBC40ASTRR-GE3 [a]
Lead (Pb)-free	IRFBC40ASPbF	IRFBC40ASTRLPbF [a]	IRFBC40ASTRRPbF [a]

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage			V_{DS}	600	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current [e]	V_{GS} at 10 V	T_C = 25 °C	I_D	6.2	A
		T_C = 100 °C		3.9	
Pulsed drain current [a, e]			I_{DM}	25	
Linear derating factor				1.0	W/°C
Single pulse avalanche energy [b]			E_{AS}	570	mJ
Repetitive avalanche current [a]			I_{AR}	6.2	A
Repetitive avalanche energy [a]			E_{AR}	13	mJ
Maximum power dissipation	T_C = 25 °C		P_D	125	W
Peak diode recovery dV/dt [c, e]			dV/dt	6.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	for 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Starting T_J = 25 °C, L = 29.6 mH, R_g = 25 Ω, I_{AS} = 6.2 A (see fig. 12)
c. $I_{SD} \leq$ 6.2 A, dI/dt ≤ 88 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C
d. 1.6 mm from case
e. Uses IRFBC40A, SiHFBC40A data and test conditions

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THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA [d]		-	0.66	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 3.7 A [b]	-	-	1.2	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.7 A		3.4	-	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1036	-	pF
Output capacitance	C_{oss}			-	136	-	
Reverse transfer capacitance	C_{rss}			-	7.0	-	
Output capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 1.0 V, f = 1.0 MHz	-	1487	-	
			V_{DS} = 480 V, f = 1.0 MHz	-	36	-	
Output capacitance effective	C_{oss} eff.		V_{DS} = 0 V to 480 V [c]	-	48	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 6.2 A, V_{DS} = 480 V, see fig. 6 and 13 [b]	-	-	42	nC
Gate-source charge	Q_{gs}			-	-	10	
Gate-drain charge	Q_{gd}			-	-	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 300 V, I_D = 6.2 A, R_g = 9.1 Ω, R_D = 47 Ω, see fig. 10 [b]		-	13	-	ns
Rise time	t_r			-	23	-	
Turn-off delay time	$t_{d(off)}$			-	31	-	
Fall time	t_f			-	18	-	
Gate input resistance	R_g	f = 1 MHz, open drain		0.6	-	3.9	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	6.2	A
Pulsed diode forward current [a]	I_{SM}			-	-	25	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 6.2 A, V_{GS} = 0 V [b]		-	-	1.5	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 6.2 A, dI/dt = 100 A/µs [b]		-	431	647	ns
Body diode reverse recovery charge	Q_{rr}			-	1.8	2.8	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %
c. C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
d. Uses IRHFBC40A, SiHFBC40A data and test conditions

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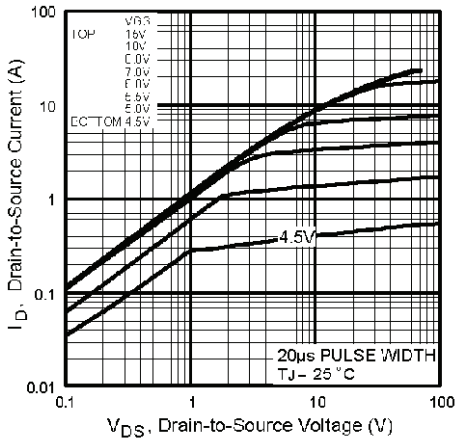


Fig. 1 - Typical Output Characteristics

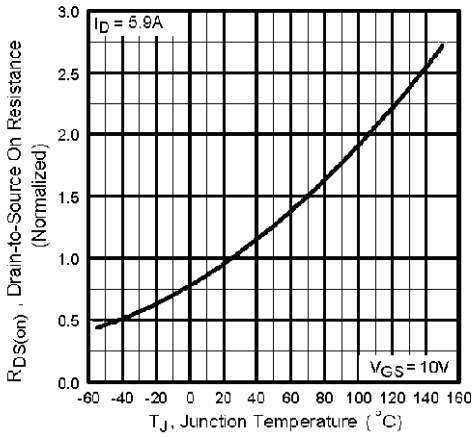


Fig. 4 - Normalized On-Resistance vs. Temperature

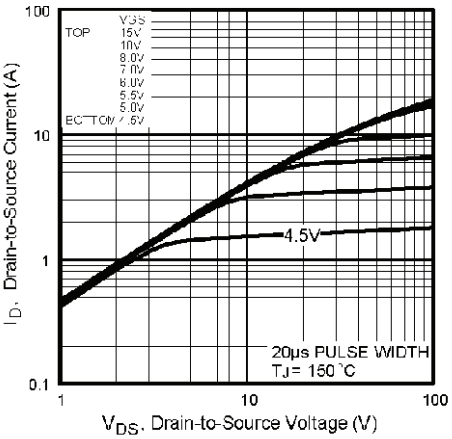


Fig. 2 - Typical Output Characteristics

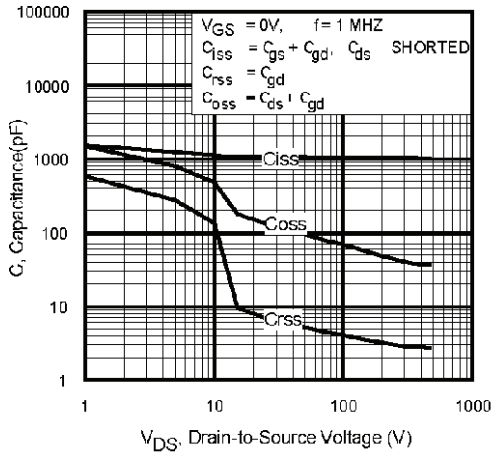


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

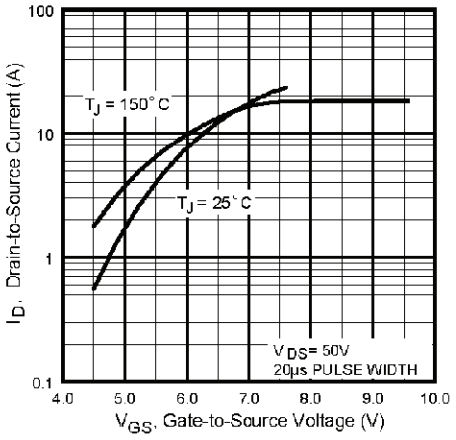


Fig. 3 - Typical Transfer Characteristics

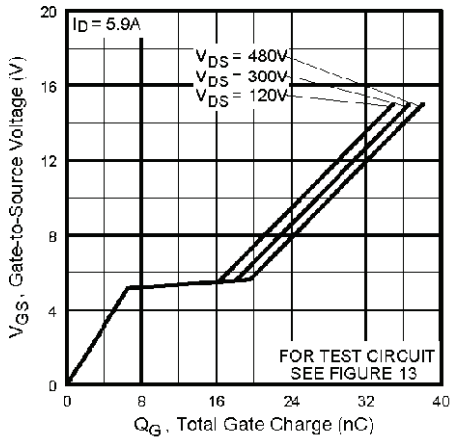


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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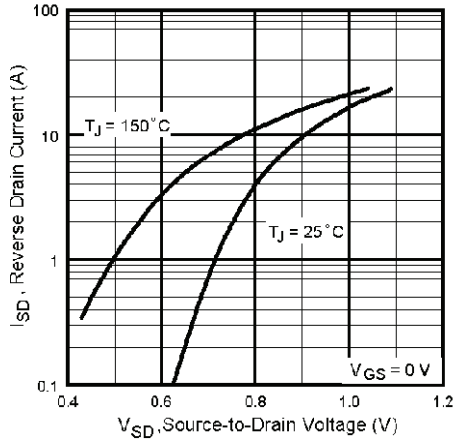


Fig. 7 - Typical Source-Drain Diode Forward Voltage

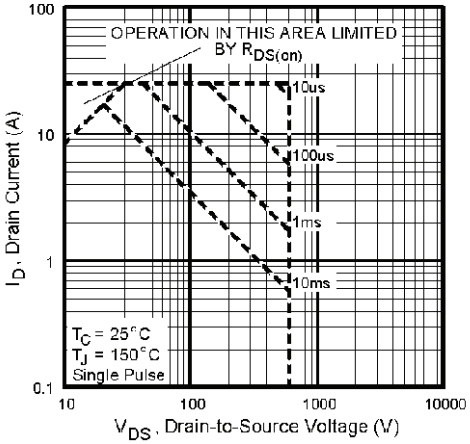


Fig. 8 - Maximum Safe Operating Area

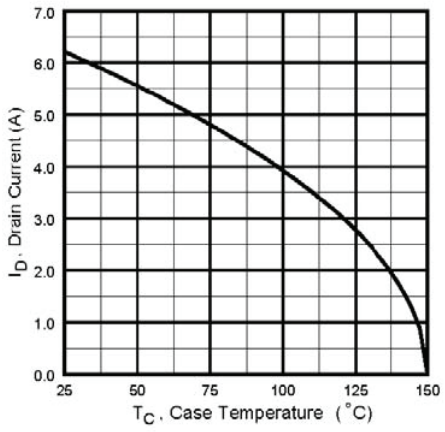


Fig. 9 - Maximum Drain Current vs. Case Temperature

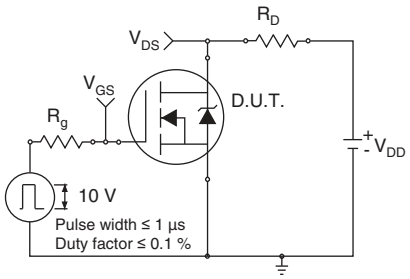


Fig. 10a - Switching Time Test Circuit

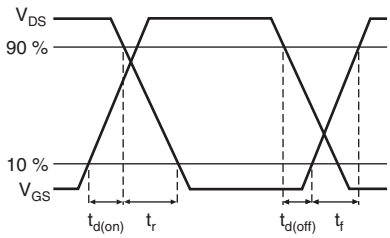


Fig. 10b - Switching Time Waveforms

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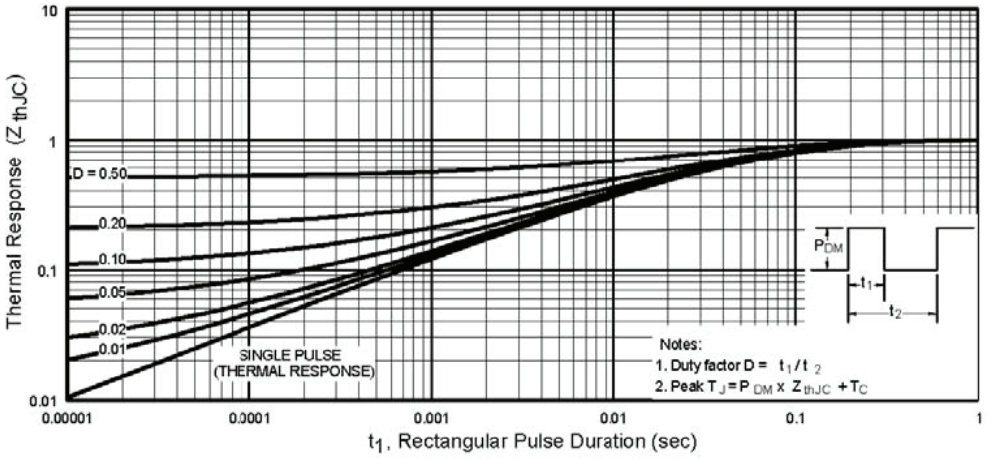


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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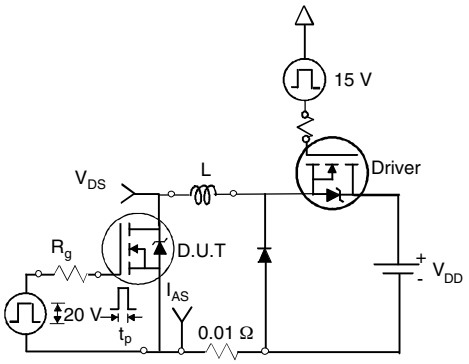


Fig. 12a - Unclamped Inductive Test Circuit

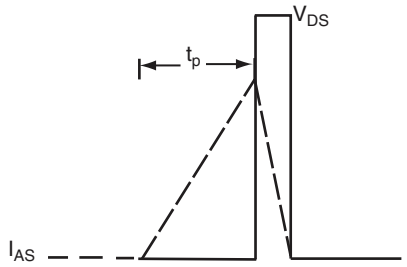


Fig. 12b - Unclamped Inductive Waveforms

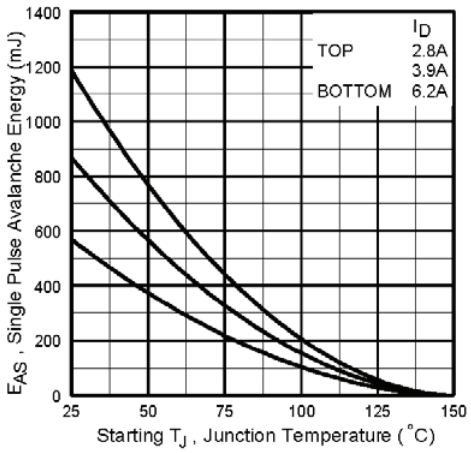


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

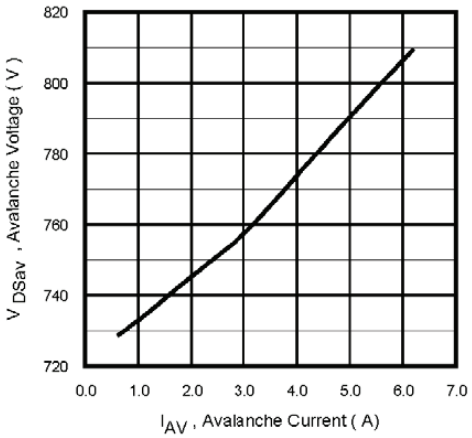


Fig. 12d - Maximum Avalanche Energy vs. Drain Current

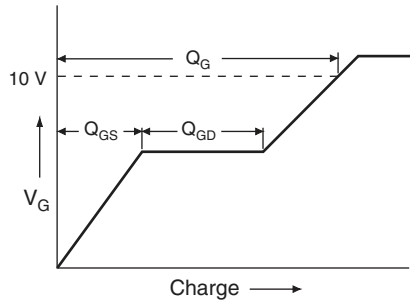


Fig. 13a - Basic Gate Charge Waveform

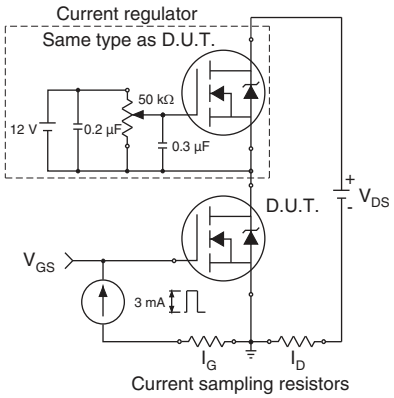
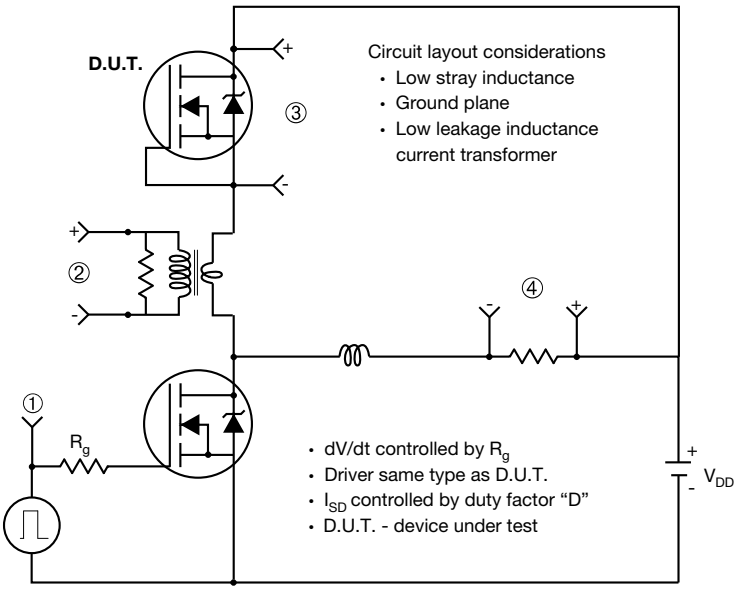
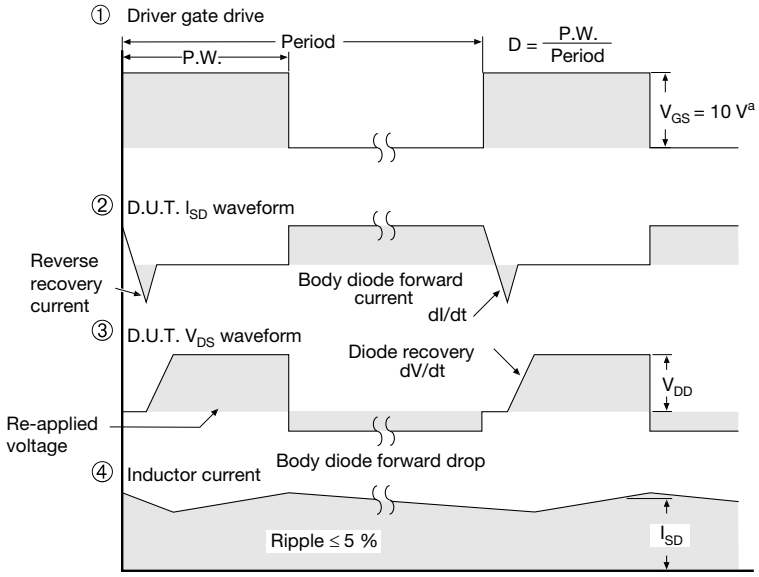


Fig. 13b - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit





Note

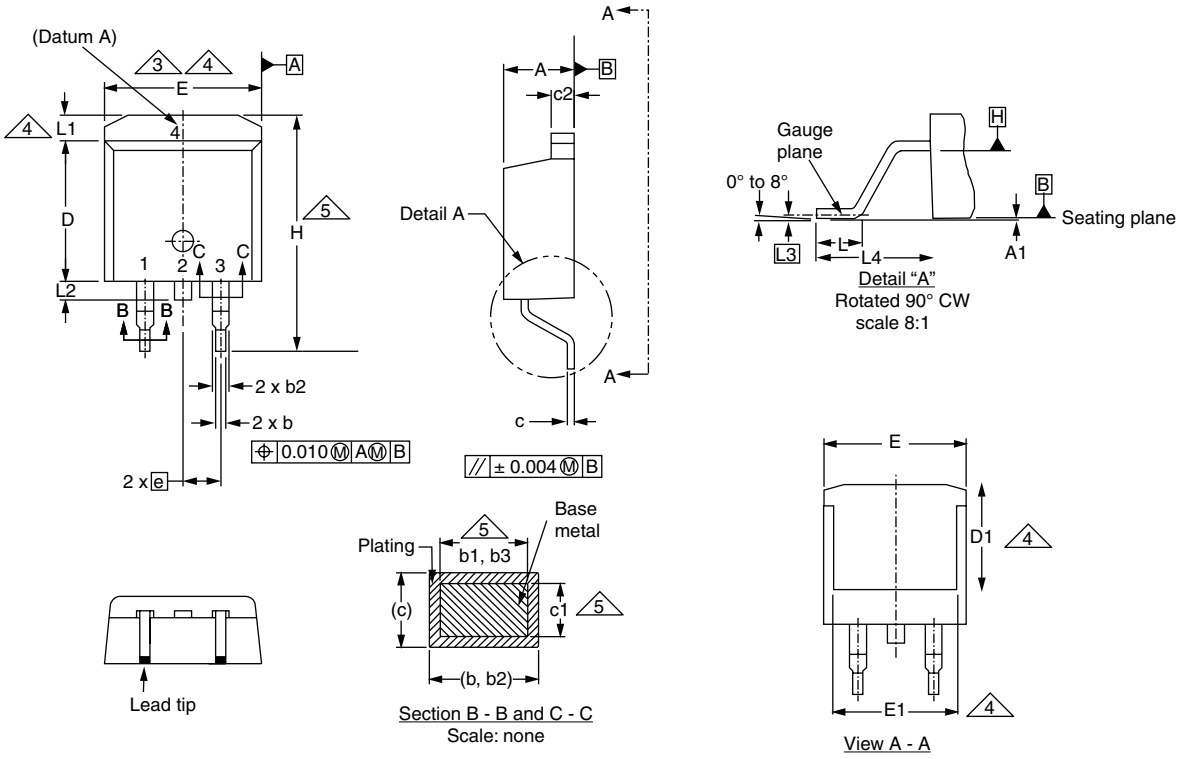
a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

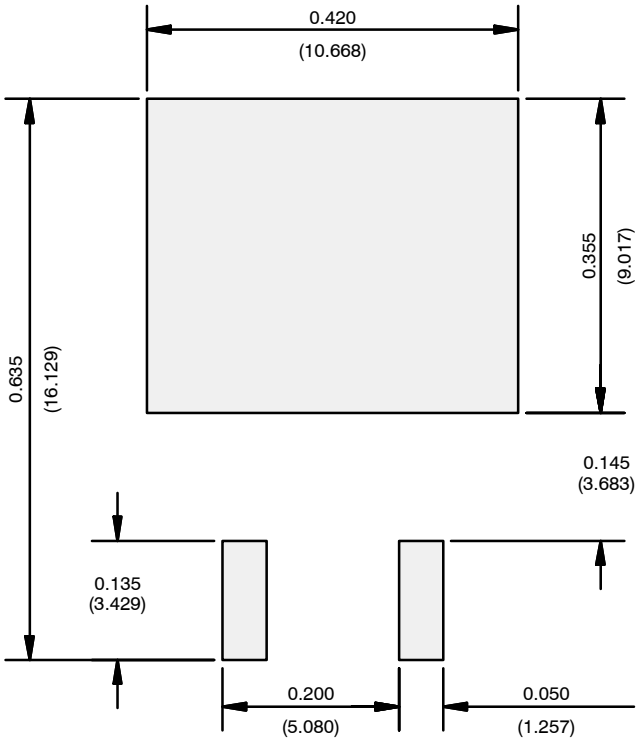
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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Teklif isteyin

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