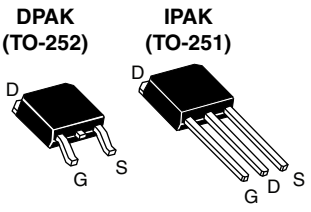
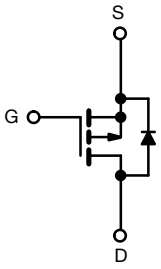
Power MOSFET





P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Surface-mount (IRFR9210, SiHFR9210)
- Straight lead (IRFU9210, SiHFU9210)
- Available in tape and reel
- P-channel
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

PRODUCT SUMMARY		
V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	V_{GS} = -10 V	3.0
Q_g (Max.) (nC)	8.9	
Q_{gs} (nC)	2.1	
Q_{gd} (nC)	3.9	
Configuration	Single	

DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface-mount applications.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR9210-GE3	SiHFR9210TR-GE3 [a]	-	SiHFU9210-GE3
	IRFR9210PbF-BE3 [b]	-	-	-
Lead (Pb)-free	IRFR9210PbF	IRFR9210TRPbF [a]	IRFR9210TRLPbF [a]	IRFU9210PbF

Notes

a. See device orientation
b. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	-200	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at -10 V	T_C = 25 °C	I_D	-1.9	A
		T_C = 100 °C		-1.2	
Pulsed drain current [a]			I_{DM}	-7.6	
Linear derating factor				0.20	W/°C
Linear derating factor (PCB mount) [e]				0.020	
Single pulse avalanche energy [b]			E_{AS}	300	mJ
Repetitive avalanche current [a]			I_{AR}	-1.9	A
Repetitive avalanche energy [a]			E_{AR}	2.5	mJ
Maximum power dissipation	T_C = 25 °C		P_D	25	W
Maximum power dissipation (PCB mount) [e]	T_A = 25 °C			2.5	
Peak diode recovery dV/dt [c]			dV/dt	-5.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			260	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = -50 V, starting T_J = 25 °C, L = 124 mH, R_g = 25 Ω, I_{AS} = -1.9 A (see fig. 12)
c. I_{SD} ≤ -1.9 A, dI/dt ≤ 70 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
d. 1.6 mm from case
e. When mounted on 1" square PCB (FR-4 or G-10 material)

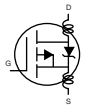
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THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	-	110	°C/W
Maximum junction-to-ambient (PCB mount) [a]	R_{thJA}	-	-	50	
Maximum junction-to-case (drain)	R_{thJC}	-	-	5.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA	-	- 0.23	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2.0	-	- 4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = - 200 V, V_{GS} = 0 V	-	-	- 100	µA
		V_{DS} = - 160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	- 500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = - 10 V; I_D = - 1.1 A[b]	-	-	3.0	Ω
Forward transconductance	g_{fs}	V_{DS} = - 50 V, I_D = - 1.1 A	0.98	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 5	-	170	-	pF
Output capacitance	C_{oss}		-	54	-	
Reverse transfer capacitance	C_{rss}		-	16	-	
Total gate charge	Q_g	V_{GS} = - 10 V; I_D = - 1.3 A, V_{DS} = - 160 V, see fig. 6 and 13[b]	-	-	8.9	nC
Gate-source charge	Q_{gs}		-	-	2.1	
Gate-drain charge	Q_{gd}		-	-	3.9	
Turn-on delay time	$t_{d(on)}$	V_{DD} = - 100 V, I_D = - 2.3 A, R_g = 24 Ω, R_D = 41 Ω, see fig. 10[b]	-	8.0	-	ns
Rise time	t_r		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	11	-	
Fall time	t_f		-	13	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 1.9	A
Pulsed diode forward current [a]	I_{SM}		-	-	- 7.6	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = - 1.9 A, V_{GS} = 0 V[b]	-	-	- 5.8	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = - 2.3 A, dI/dt = 100 A/µs[b]	-	110	220	ns
Body diode reverse recovery charge	Q_{rr}		-	0.56	1.1	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

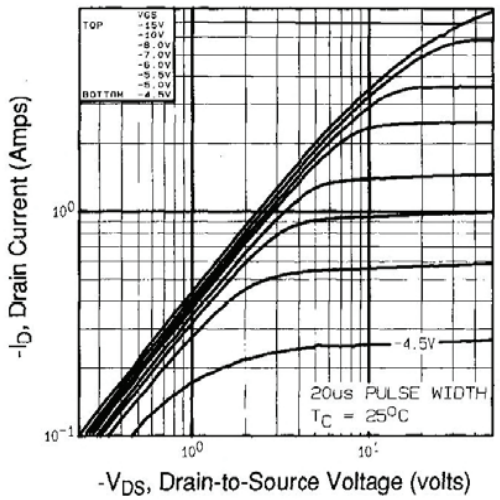


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

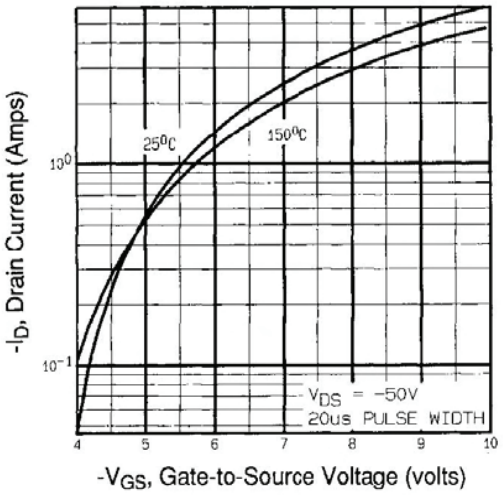


Fig. 2 - Typical Transfer Characteristics

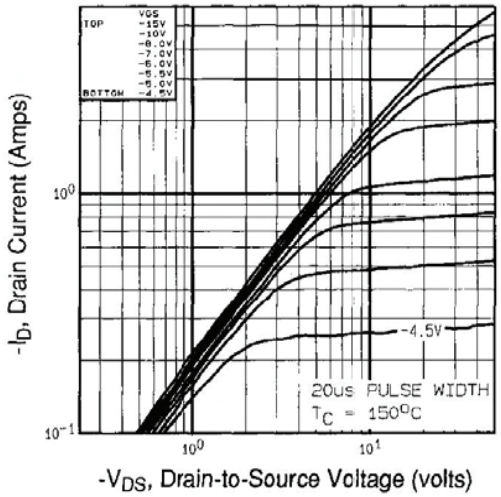


Fig. 1 - Typical Output Characteristics, T_C = 150 °C

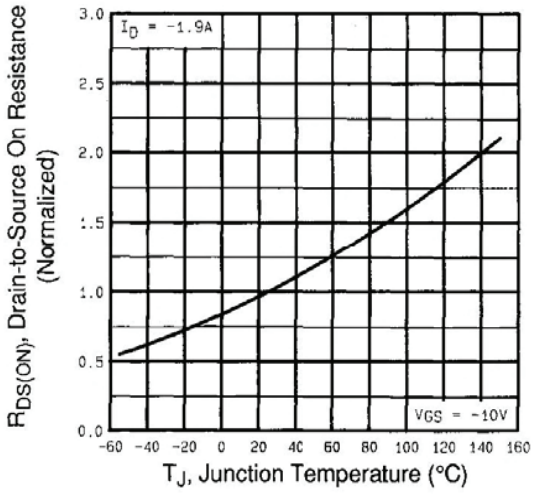


Fig. 3 - Normalized On-Resistance vs. Temperature

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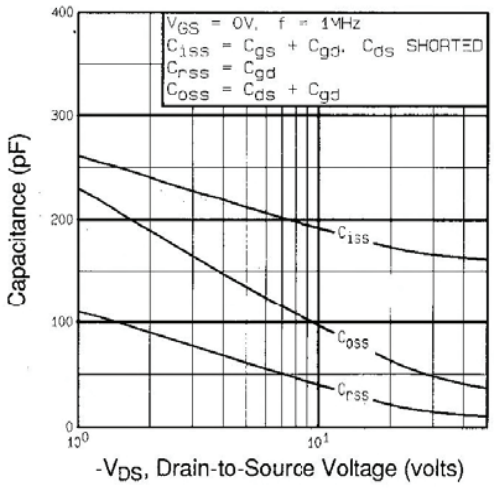


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

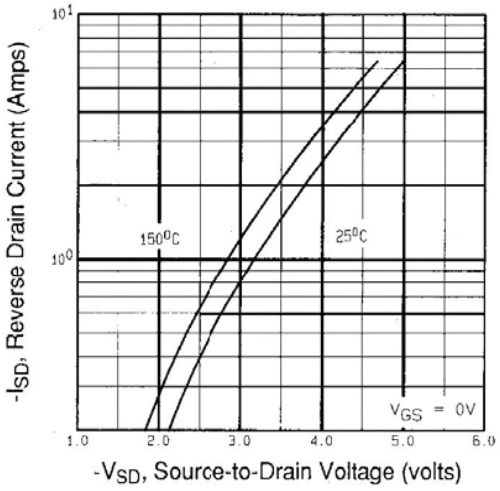


Fig. 6 - Typical Source-Drain Diode Forward Voltage

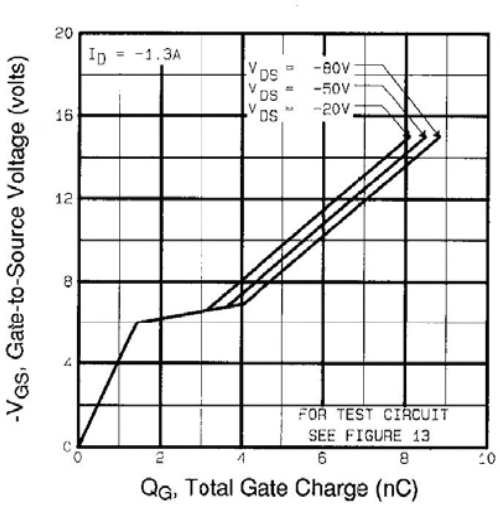


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

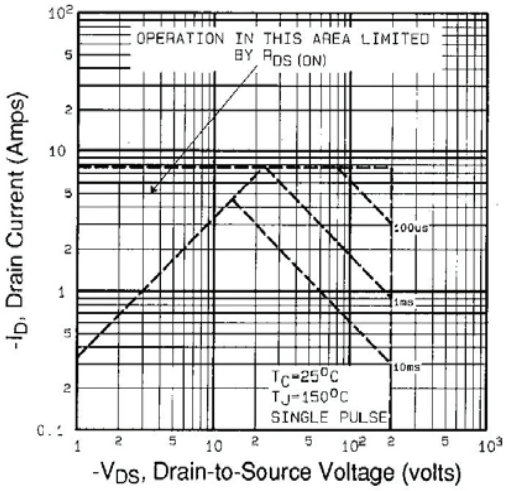


Fig. 7 - Maximum Safe Operating Area

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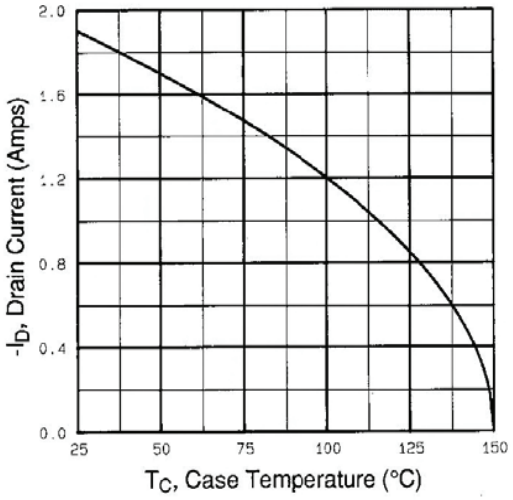


Fig. 8 - Maximum Drain Current vs. Case Temperature

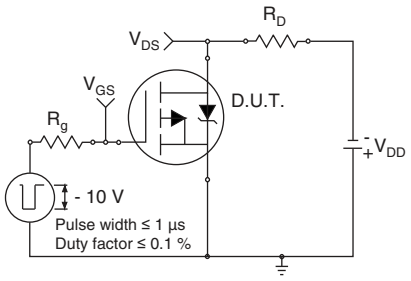


Fig. 10a - Switching Time Test Circuit

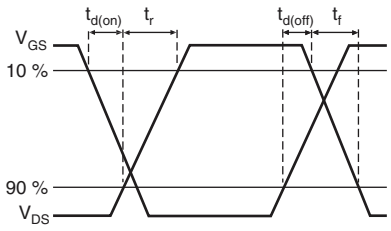


Fig. 10b - Switching Time Waveforms

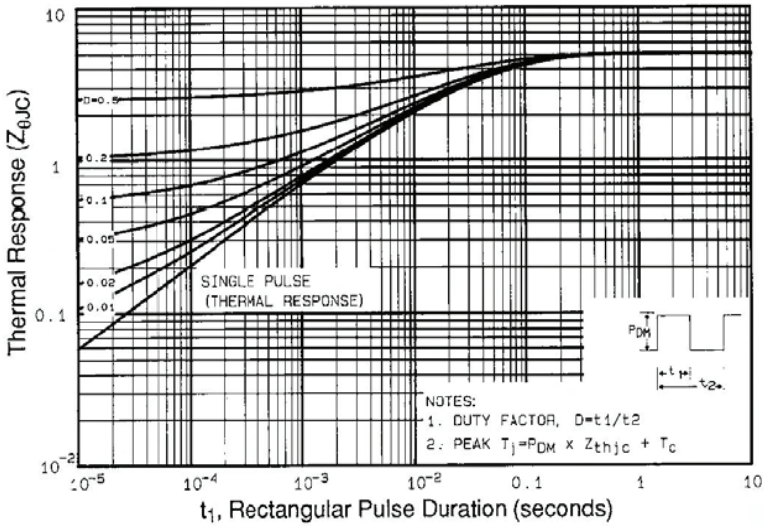


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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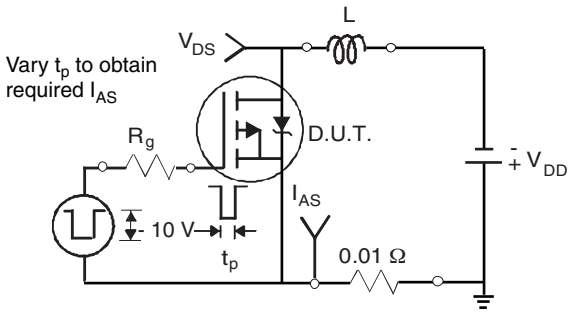


Fig. 12a - Unclamped Inductive Test Circuit

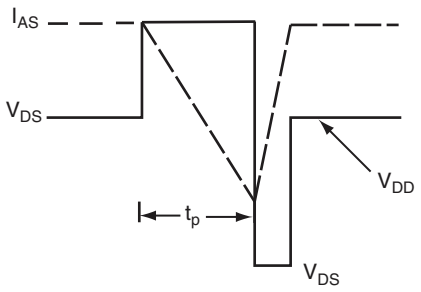


Fig. 12b - Unclamped Inductive Waveforms

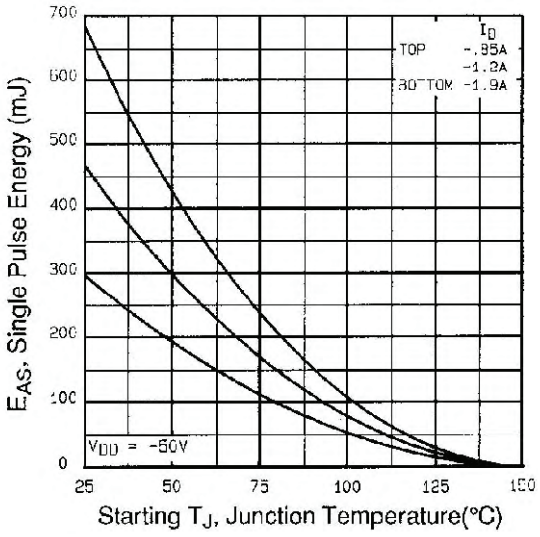


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

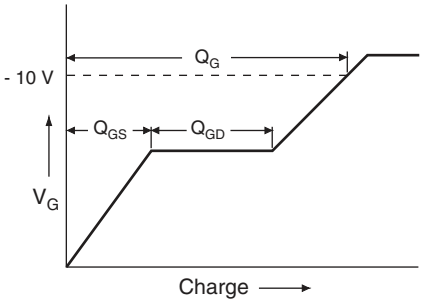


Fig. 13a - Basic Gate Charge Waveform

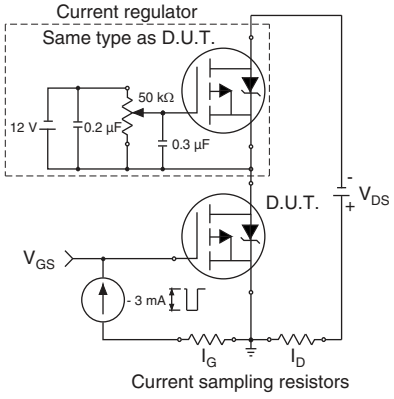
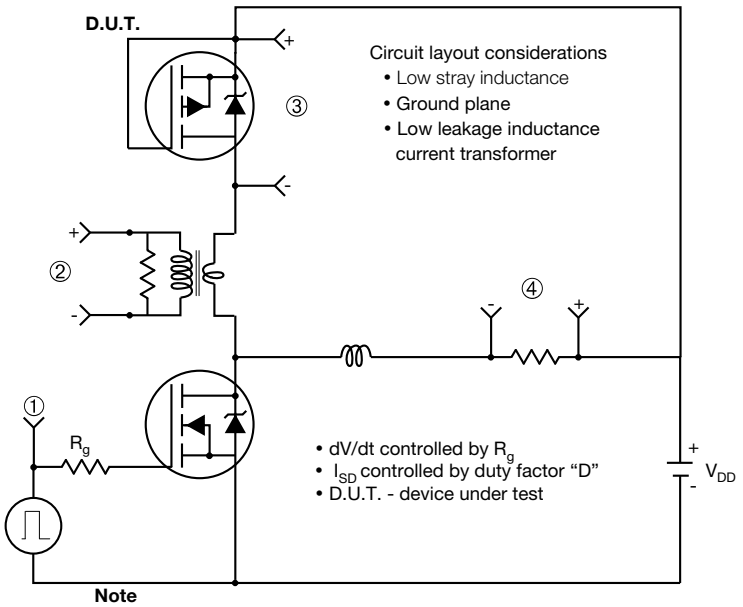


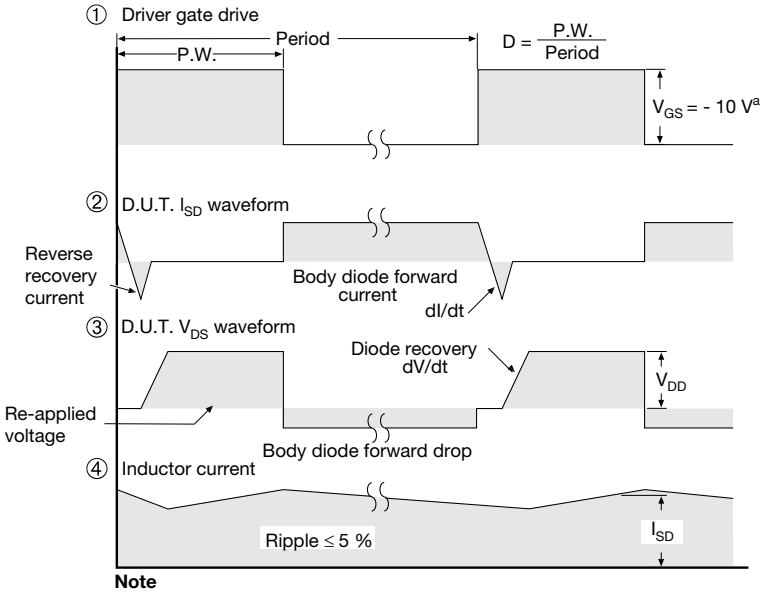
Fig. 13b - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. V_{GS} = - 5 V for logic level and - 3 V drive devices

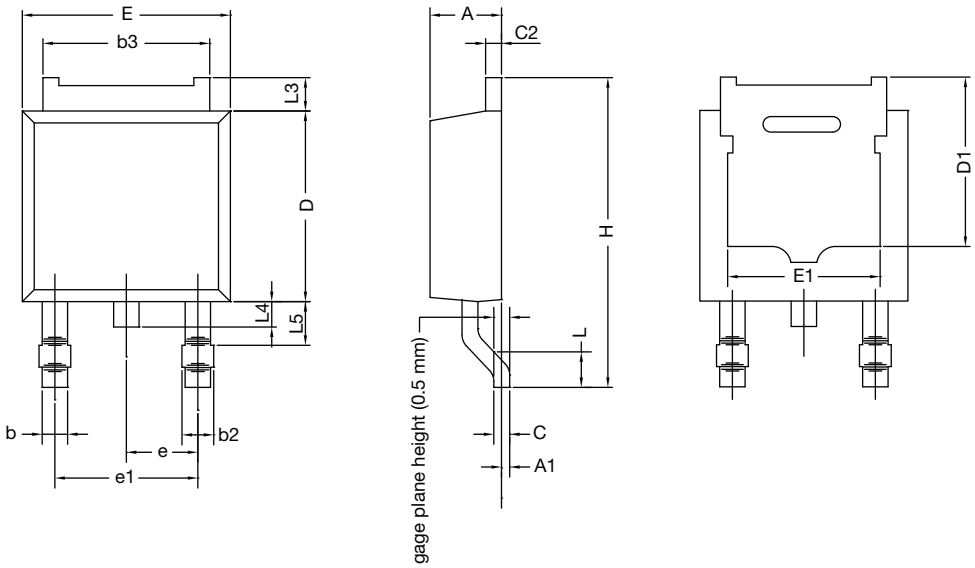
Fig. 10 - For P-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

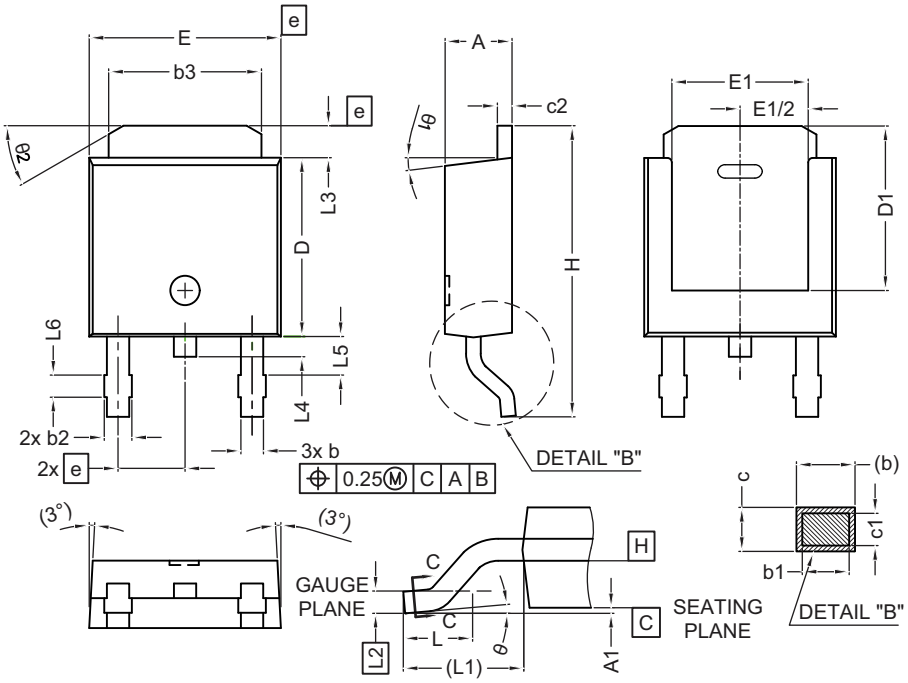
Note

- Dimension L3 is for reference only

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VERSION 2: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

	MILLIMETERS	
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

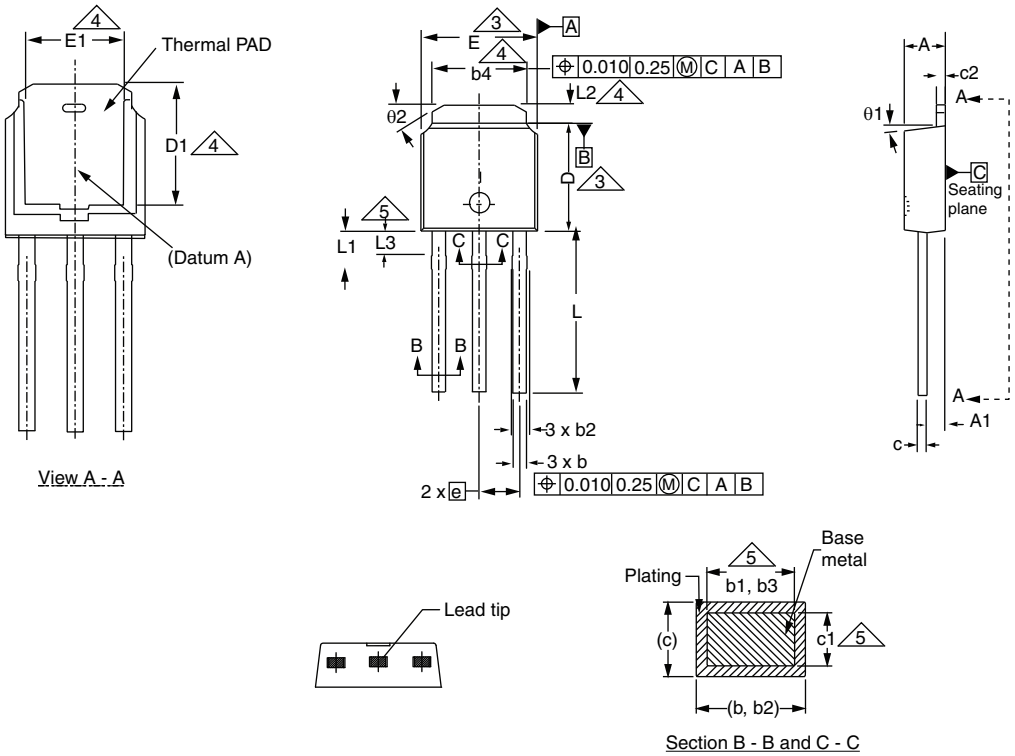
ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

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Case Outline for TO-251AA (High Voltage)

OPTION 1:



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0'	15'	0'	15'
θ2	25'	35'	25'	35'

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

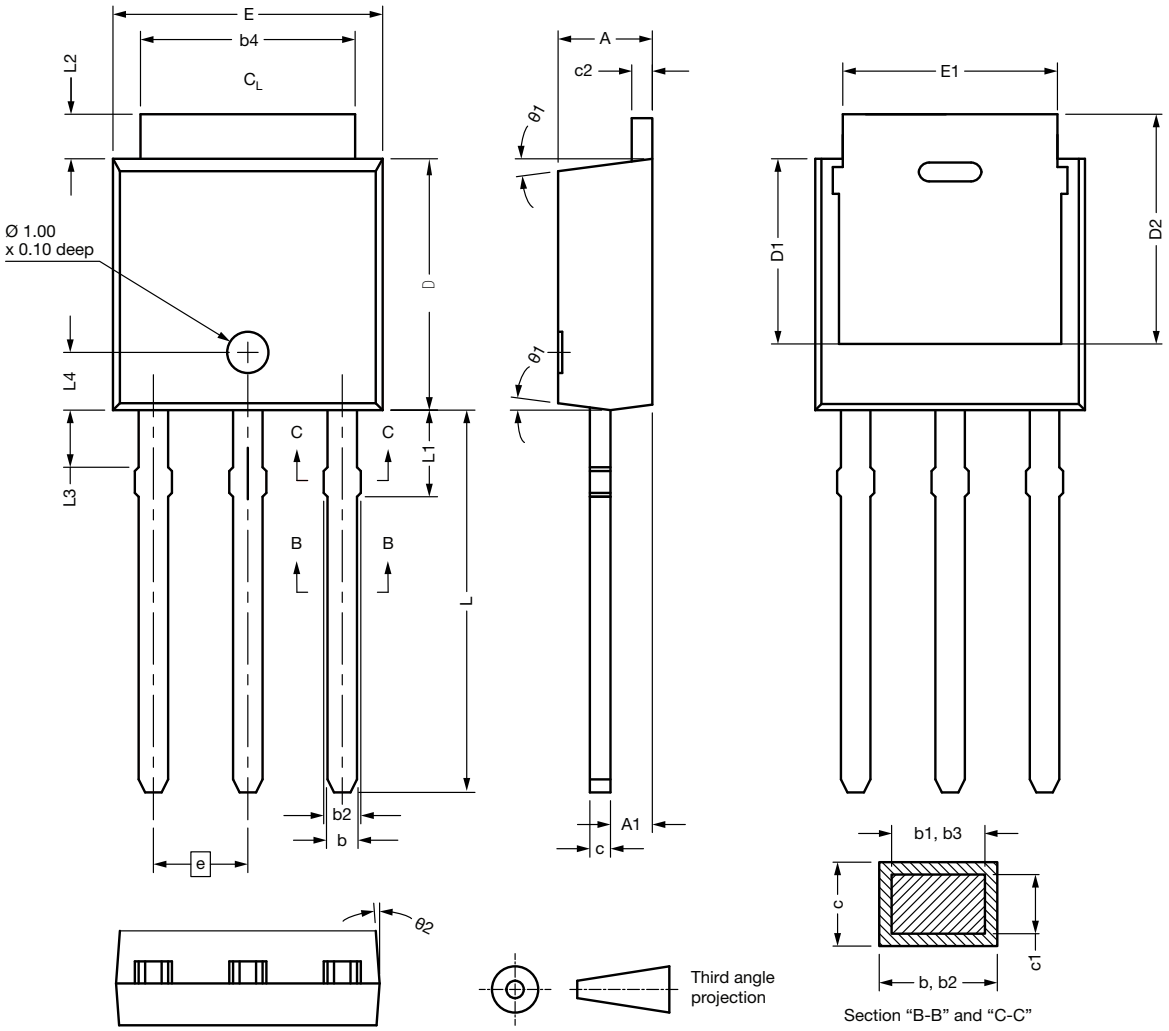
Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA

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OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
θ1	0°	7.5°	15°
θ2	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

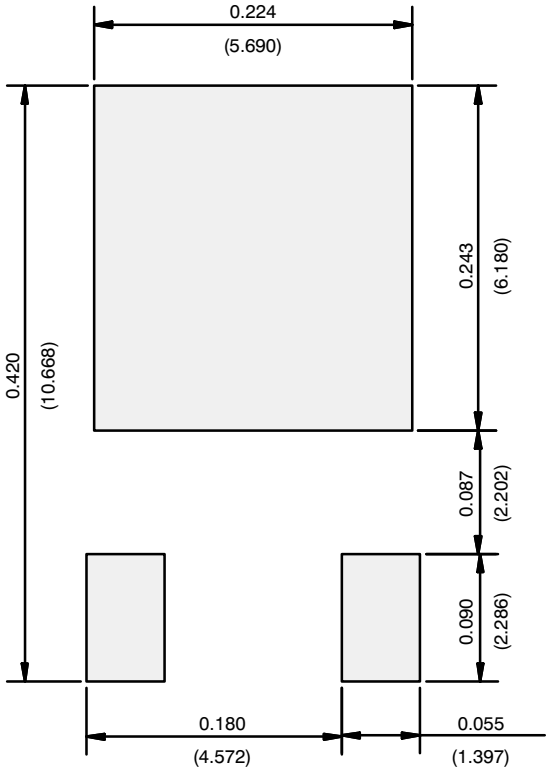
Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm

For technical questions, contact: hvmos.techsupport@vishay.com

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RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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