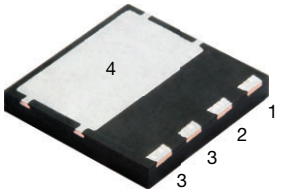
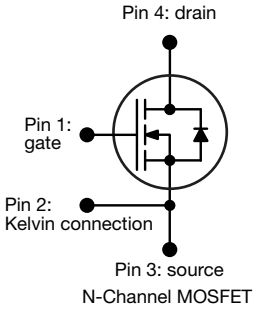
E Series Power MOSFET

PowerPAK® 8 x 8





N-Channel MOSFET

FEATURES

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.085
Q_g max. (nC)	129	
Q_{gs} (nC)	20	
Q_{gd} (nC)	44	
Configuration	Single	

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and halogen-free	SiHH28N60E-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	600	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	29	A
		T_C = 100 °C		19	
Pulsed drain current [a]			I_{DM}	76	
Linear derating factor				1.6	W/°C
Single pulse avalanche energy [b]			E_{AS}	353	mJ
Maximum power dissipation			P_D	202	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	70	V/ns
Reverse diode dV/dt [c]				13	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 5 A

c. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting T_J = 25 °C

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THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	38	50	°C/W
Maximum junction-to-case (Drain)	R_{thJC}	0.48	0.62	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 10 mA		-	0.58	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
		V_{GS} = ± 30 V		-	-	± 1	µA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V		-	-	1	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 14 A	-	0.085	0.098	Ω
Forward transconductance	g_{fs}	V_{DS} = 30 V, I_D = 14 A		-	7.6	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	2614	-	pF
Output capacitance	C_{oss}			-	125	-	
Reverse transfer capacitance	C_{rss}			-	5	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V		-	86	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$			-	444	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 10 A, V_{DS} = 480 V	-	86	129	nC
Gate-source charge	Q_{gs}			-	20	-	
Gate-drain charge	Q_{gd}			-	44	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 480 V, I_D = 14 A, V_{GS} = 10 V, R_g = 9.1 Ω		-	29	58	ns
Rise time	t_r			-	75	113	
Turn-off delay time	$t_{d(off)}$			-	84	126	
Fall time	t_f			-	54	81	
Gate input resistance	R_g	f = 1 MHz		0.2	0.5	1.0	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	29	A
Pulsed diode forward current	I_{SM}			-	-	76	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 14 A, V_{GS} = 0 V		-	0.9	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 14 A, dI/dt = 100 A/µs, V_R = 25 V		-	386	772	ns
Reverse recovery charge	Q_{rr}			-	6	12	µC
Reverse recovery current	I_{RRM}			-	25	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

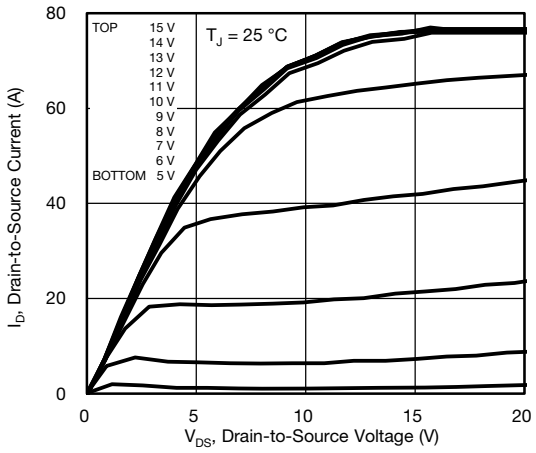


Fig. 1 - Typical Output Characteristics

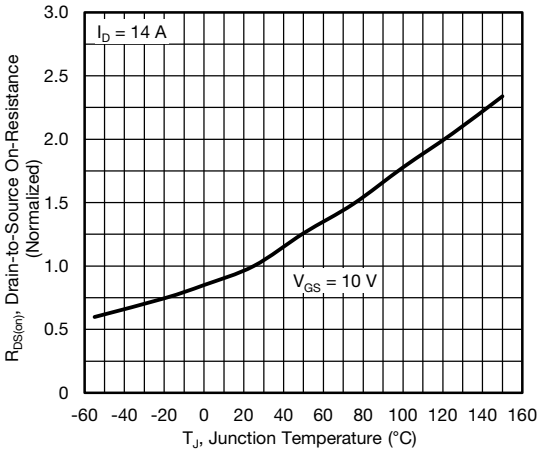


Fig. 4 - Normalized On-Resistance vs. Temperature

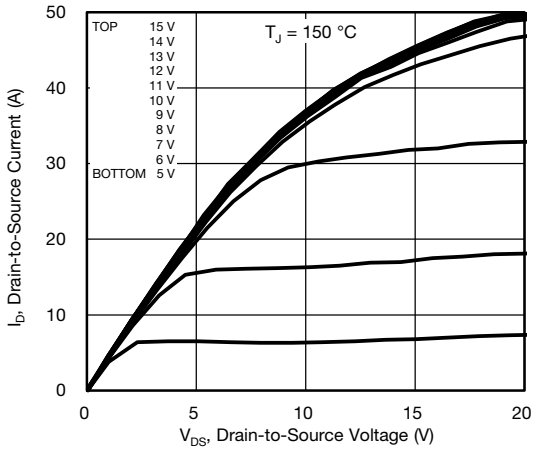


Fig. 2 - Typical Output Characteristics

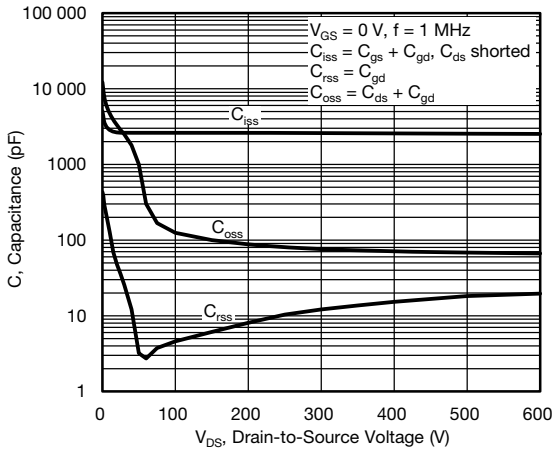


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

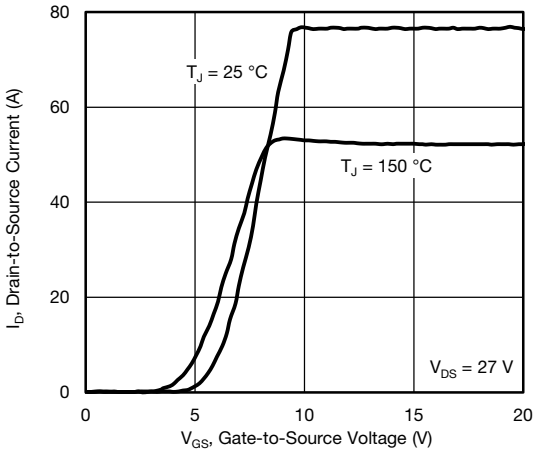


Fig. 3 - Typical Transfer Characteristics

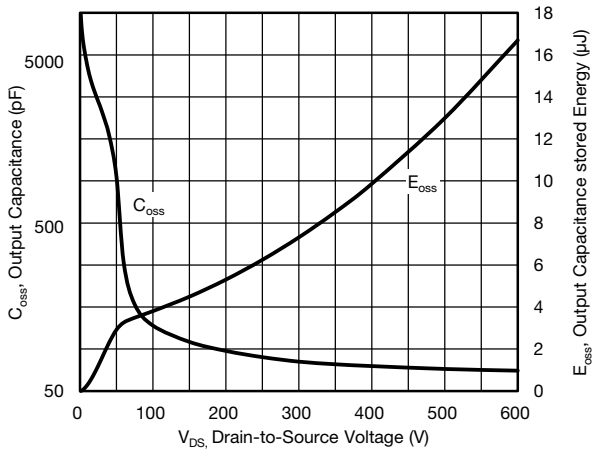


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

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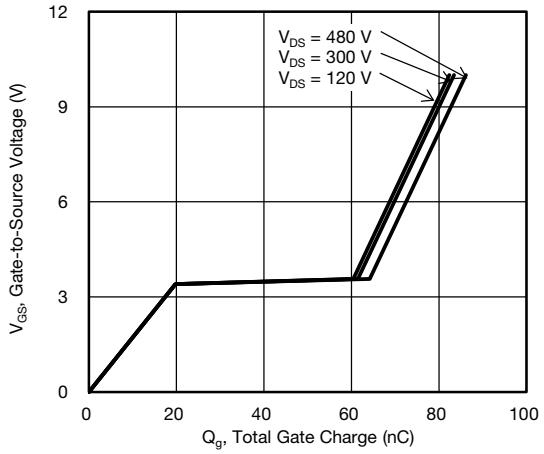


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

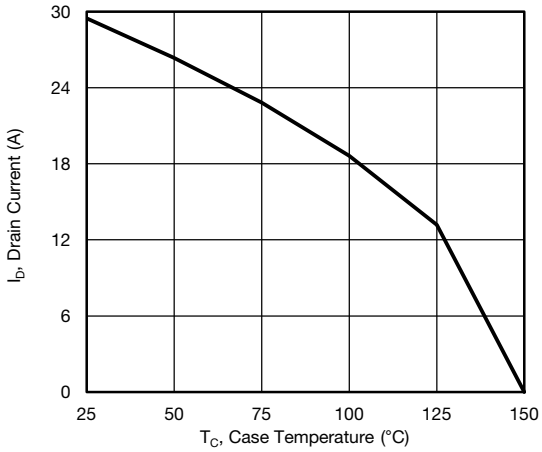


Fig. 10 - Maximum Drain Current vs. Case Temperature

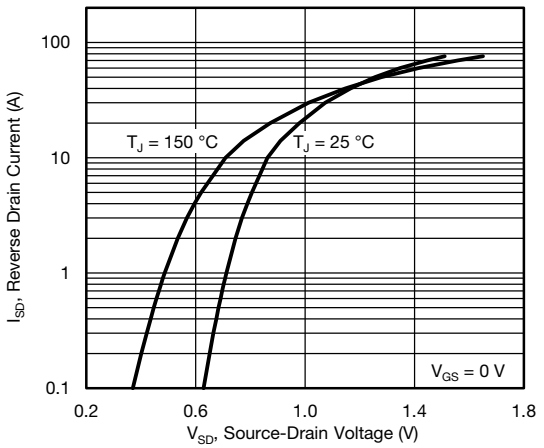


Fig. 8 - Typical Source-Drain Diode Forward Voltage

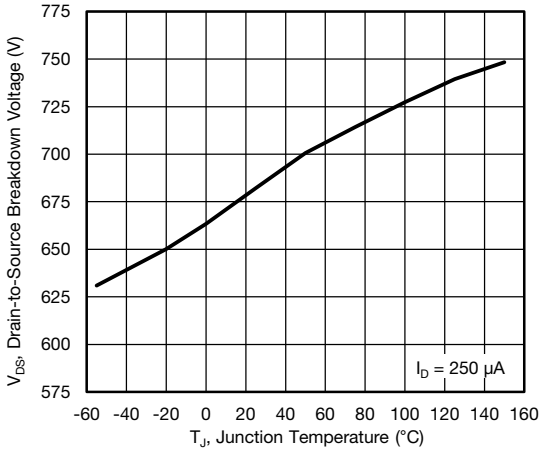


Fig. 11 - Temperature vs. Drain-to-Source Voltage

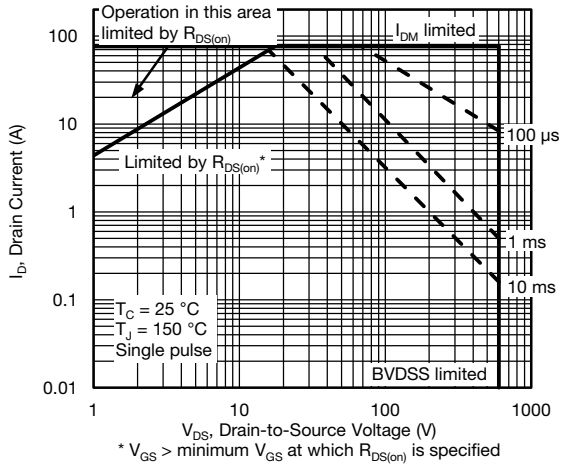


Fig. 9 - Maximum Safe Operating Area

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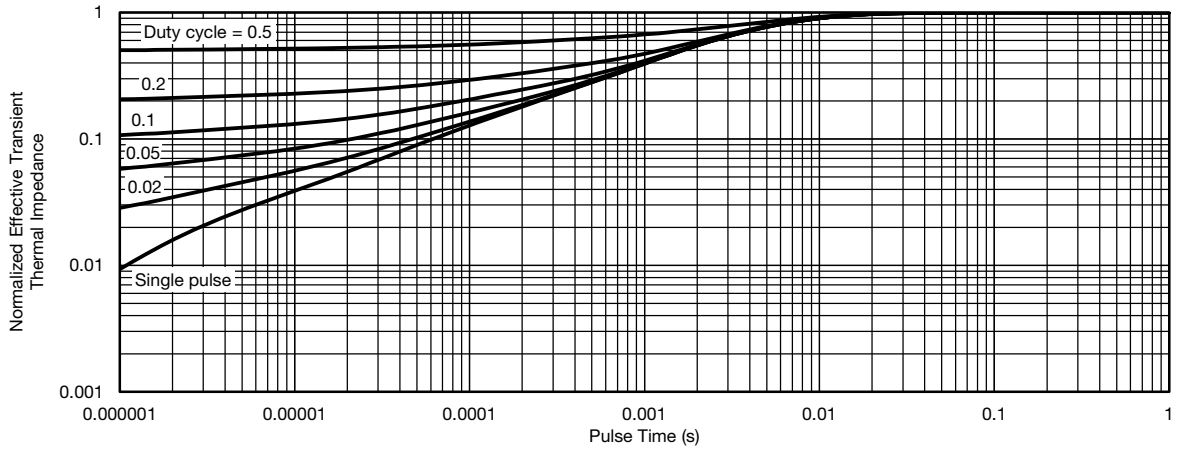


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

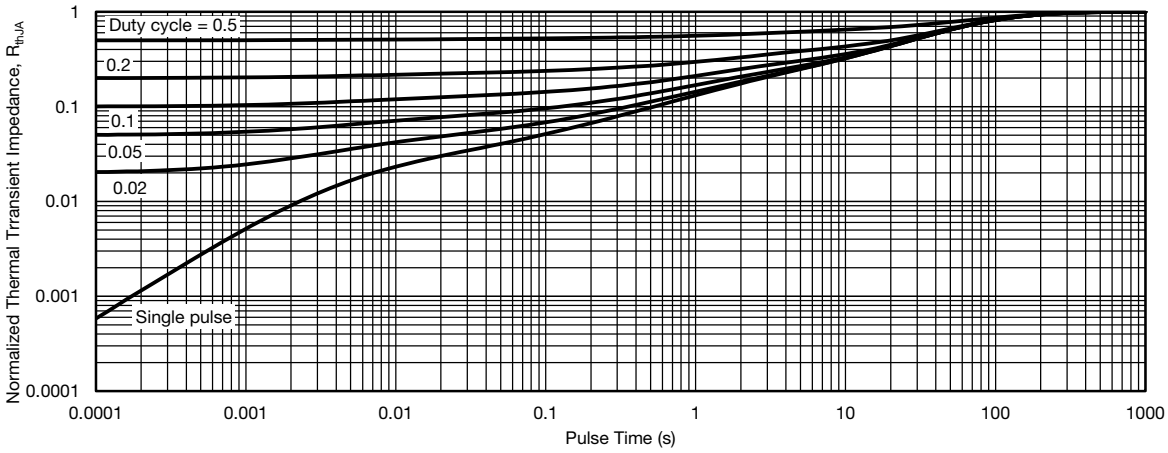


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

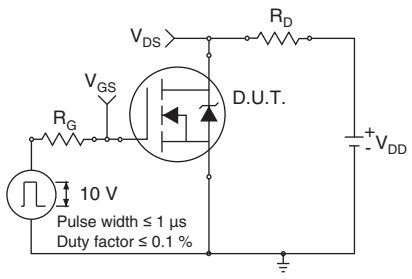


Fig. 14 - Switching Time Test Circuit

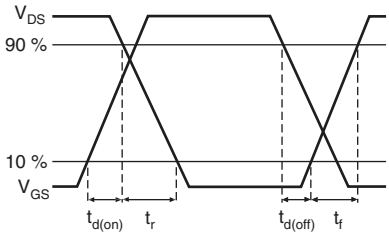


Fig. 15 - Switching Time Waveforms

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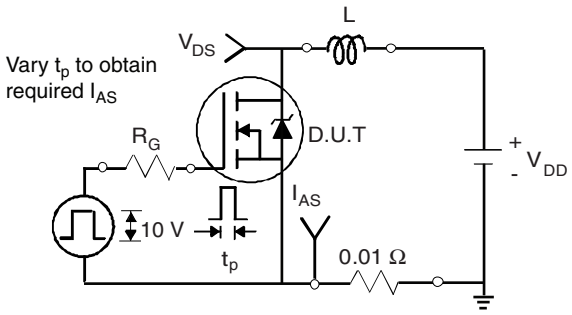


Fig. 16 - Unclamped Inductive Test Circuit

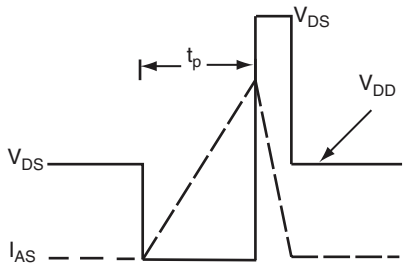


Fig. 17 - Unclamped Inductive Waveforms

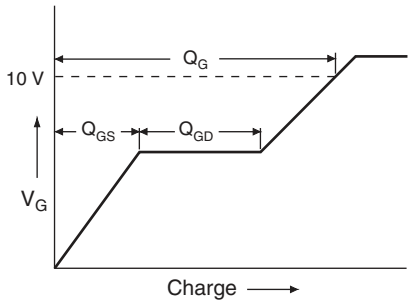


Fig. 18 - Basic Gate Charge Waveform

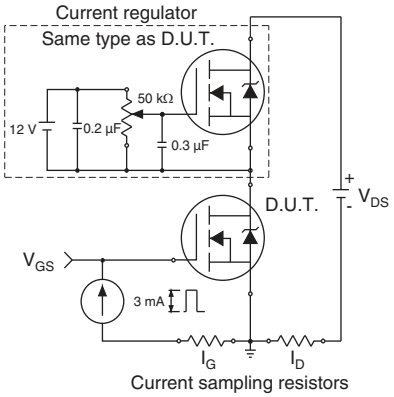
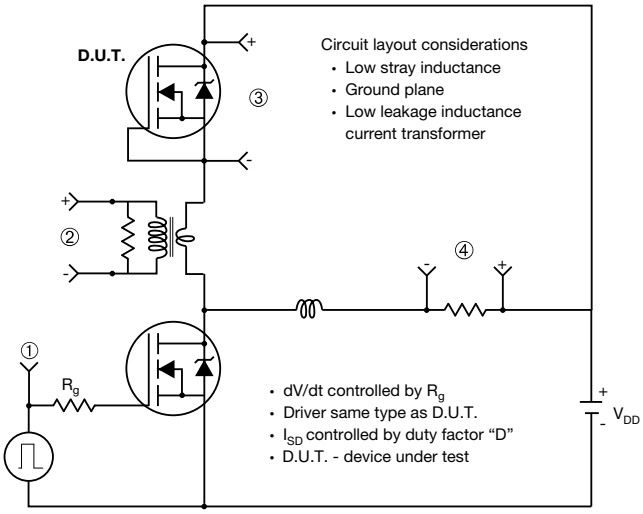
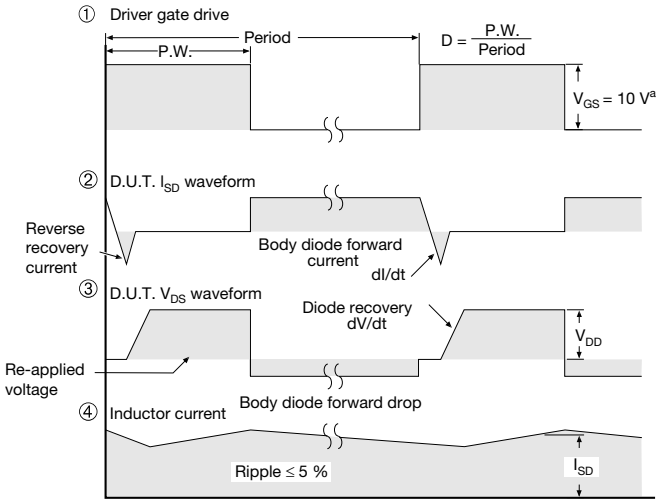


Fig. 19 - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit





Note

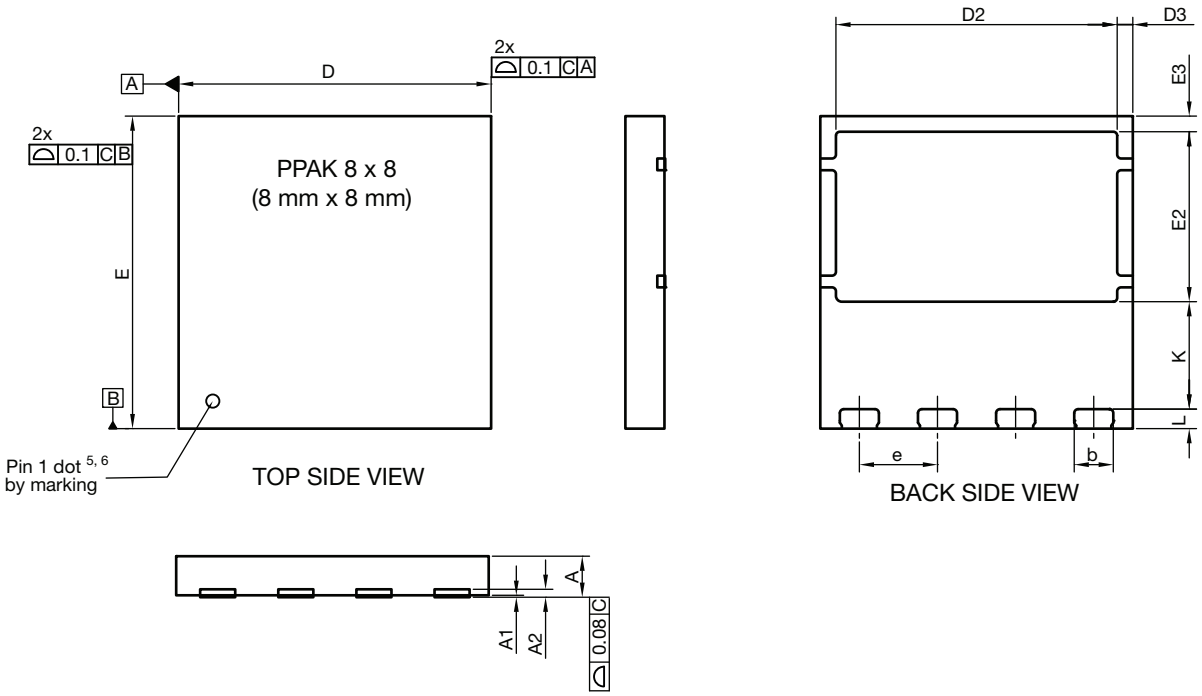
a. V_{GS} = 5 V for logic level devices

Fig. 20 - For N-Channel

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PowerPAK® 8 x 8 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	8			8		

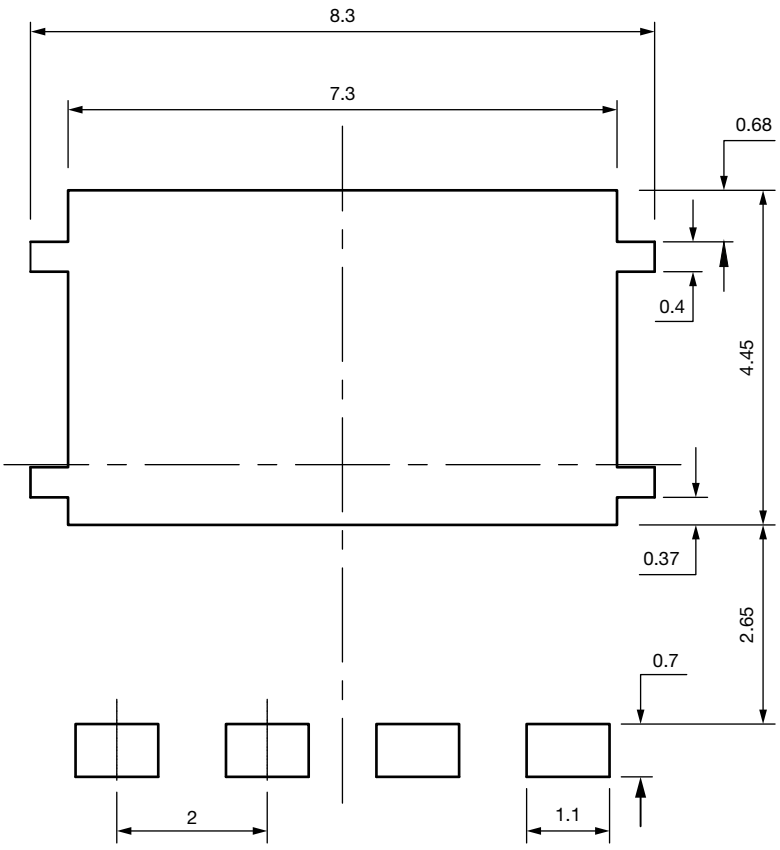
Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5 M - 1994
(3) N is the number of terminals
(4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(5) Exact shape and size of this feature is optional

ECN: E20-0518-Rev. B, 28-Sep-2020
DWG: 6041

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Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters

For technical questions, contact: pmostechsupport@vishay.com

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Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

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Toplu alım ve teklif

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Teklif isteyin

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