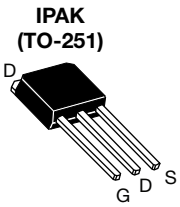
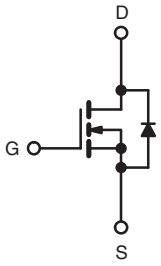
# D Series Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 550 | |
| $R_{DS(on)}$ max. at 25 °C (Ω) | $V_{GS}$ = 10 V | 3.2 |
| $Q_g$ (max.) (nC) | 12 | |
| $Q_{gs}$ (nC) | 2 | |
| $Q_{gd}$ (nC) | 3 | |
| Configuration | Single | |




N-Channel MOSFET

## FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance ($C_{iss}$)
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): $R_{on}$ x $Q_g$
  - Fast switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding, induction heating, motor drives
- Battery chargers

| ORDERING INFORMATION | |
|---|---|
| Package | IPAK (TO-251) |
| Lead (Pb)-free and Halogen-free | SiHU3N50DA-GE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 500 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Gate-Source Voltage AC (f > 1 Hz) | | | | 30 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 3.0 | A |
| | | $T_C$ = 100 °C | | 1.9 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 5.5 | |
| Linear Derating Factor | | | | 0.56 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 9 | mJ |
| Maximum Power Dissipation | | | $P_D$ | 69 | W |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Drain-Source Voltage Slope | $T_J$ = 125 °C | | dV/dt | 24 | V/ns |
| Reverse Diode dV/dt[d] | | | | 0.22 | |
| Soldering Recommendations (Peak Temperature)[c] | for 10 s | | | 300 | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 2.3 mH, $R_g$ = 25 Ω, $I_{AS}$ = 2.8 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting $T_J$ = 25 °C.



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| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 1.8 | |

| SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 500 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.59 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | - | 4.5 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 1.5 A | - | 2.6 | 3.2 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 8 V, $I_D$ = 1.5 A | - | 1 | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 177 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 26 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 7 | - | |
| Effective Output Capacitance, Energy Related[b] | $C_{o(er)}$ | $V_{DS}$ = 0 V to 400 V, $V_{GS}$ = 0 V | - | 21 | - | |
| Effective Output Capacitance, Time Related[c] | $C_{o(tr)}$ | | - | 28 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V, $I_D$ = 1.5 A, $V_{DS}$ = 400 V | - | 6 | 12 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 2 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 3 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 400 V, $I_D$ = 1.5 A, $R_g$ = 9.1 Ω, $V_{GS}$ = 10 V | - | 12 | 24 | ns |
| Rise Time | $t_r$ | | - | 9 | 18 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 11 | 22 | |
| Fall Time | $t_f$ | | - | 13 | 26 | |
| Gate Input Resistance | $R_g$ | f = 1 MHz, open drain | - | 2.6 | - | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse P - N junction diode  | - | - | 3 | A |
| Pulsed Diode Forward Current | $I_{SM}$ | | - | - | 5.5 | |
| Diode Forward Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 1.5 A, $V_{GS}$ = 0 V | - | - | 1.2 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 1.5 A, dI/dt = 100 A/µs, $V_R$ = 25 V | - | 285 | 570 | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 0.68 | 1.36 | µC |
| Reverse Recovery Current | $I_{RRM}$ | | - | 5 | - | A |

**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.



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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

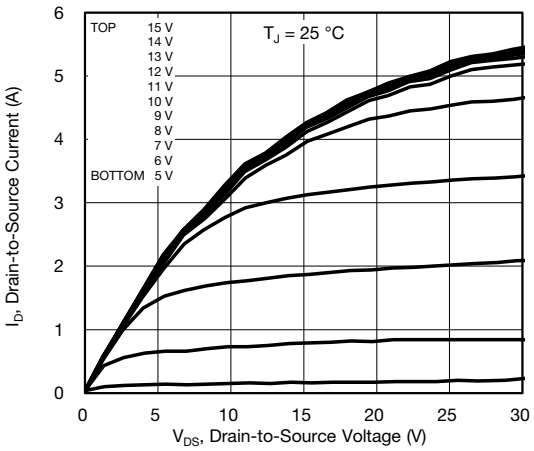



**Fig. 1 - Typical Output Characteristics**

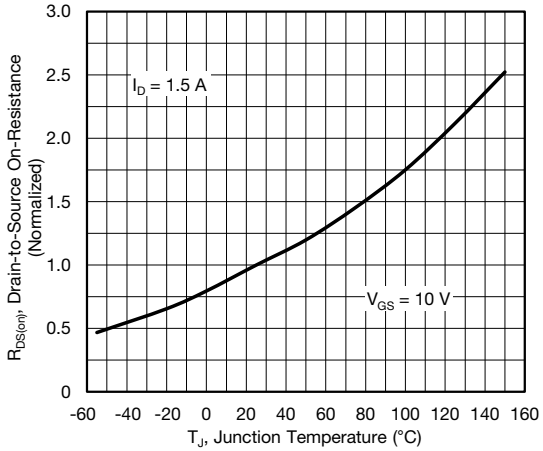



**Fig. 4 - Normalized On-Resistance vs. Temperature**

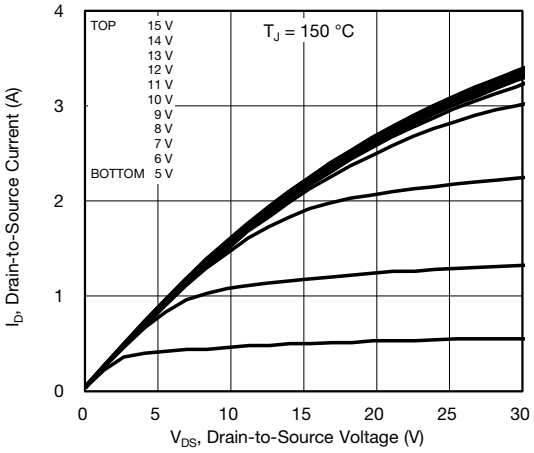



**Fig. 2 - Typical Output Characteristics**

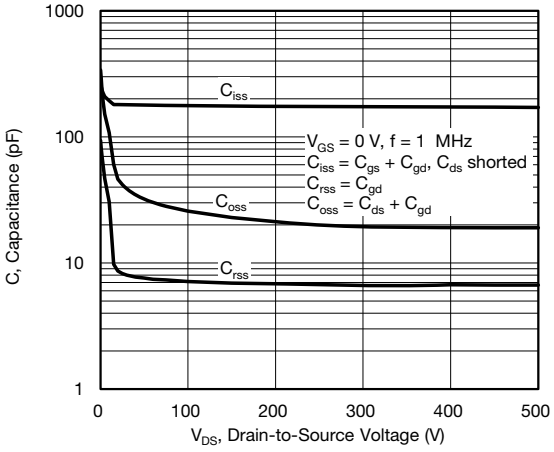



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

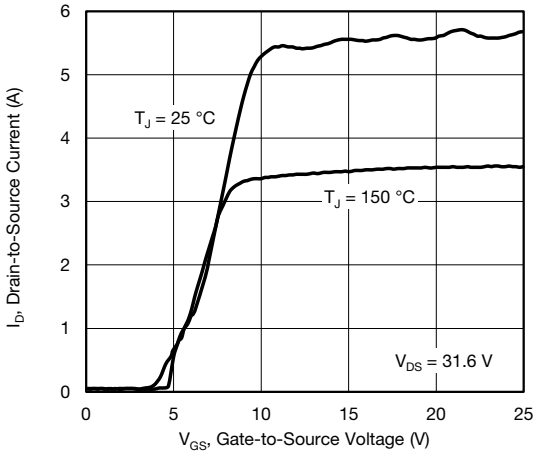



**Fig. 3 - Typical Transfer Characteristics**

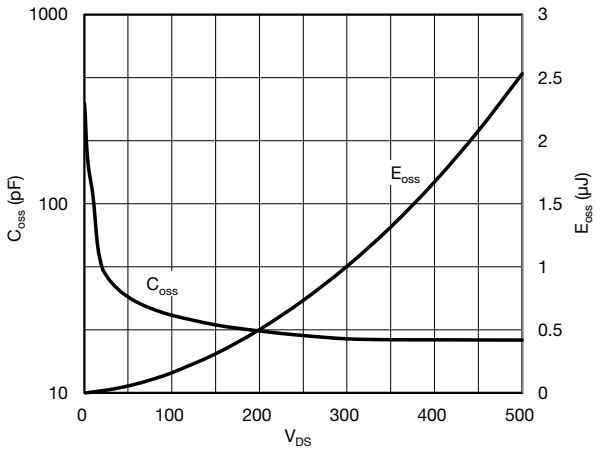



**Fig. 6 - $C_{oss}$ and $E_{oss}$ vs. $V_{DS}$**


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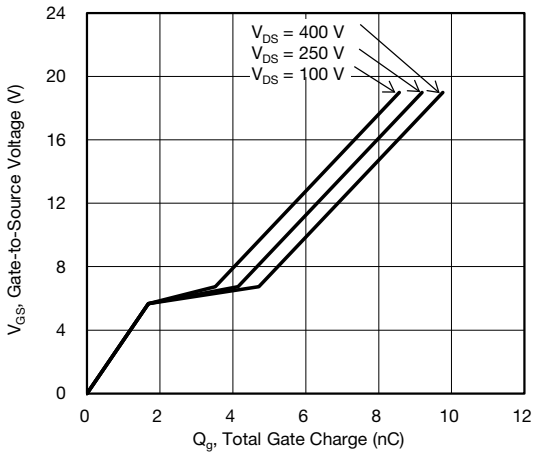



**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

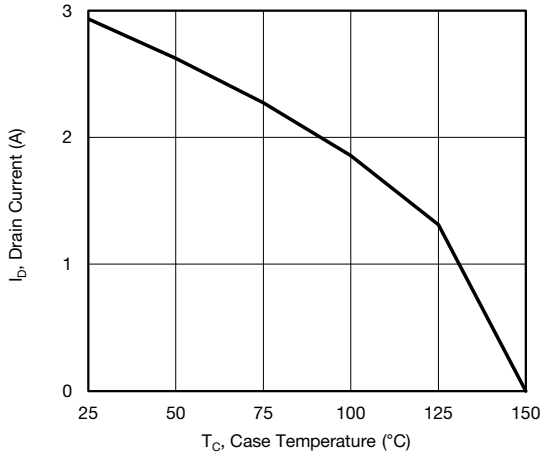



**Fig. 10 - Maximum Drain Current vs. Case Temperature**

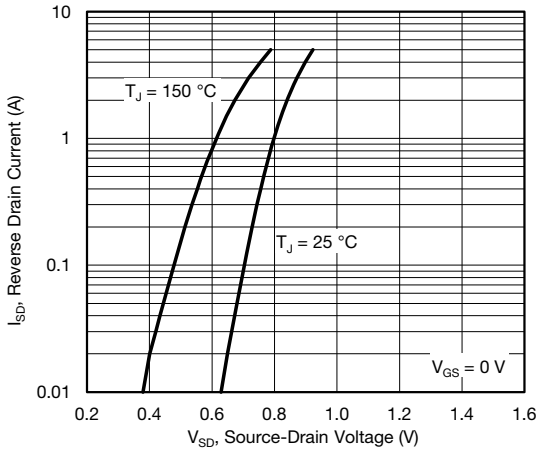



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

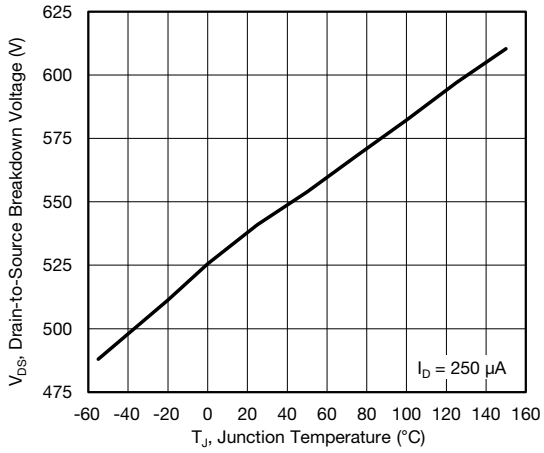



**Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature**

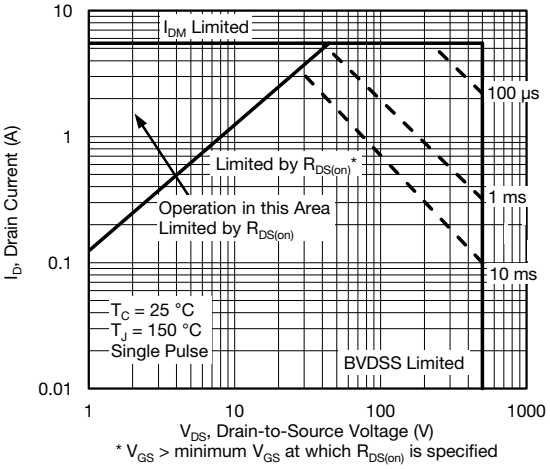



**Fig. 9 - Maximum Safe Operating Area**


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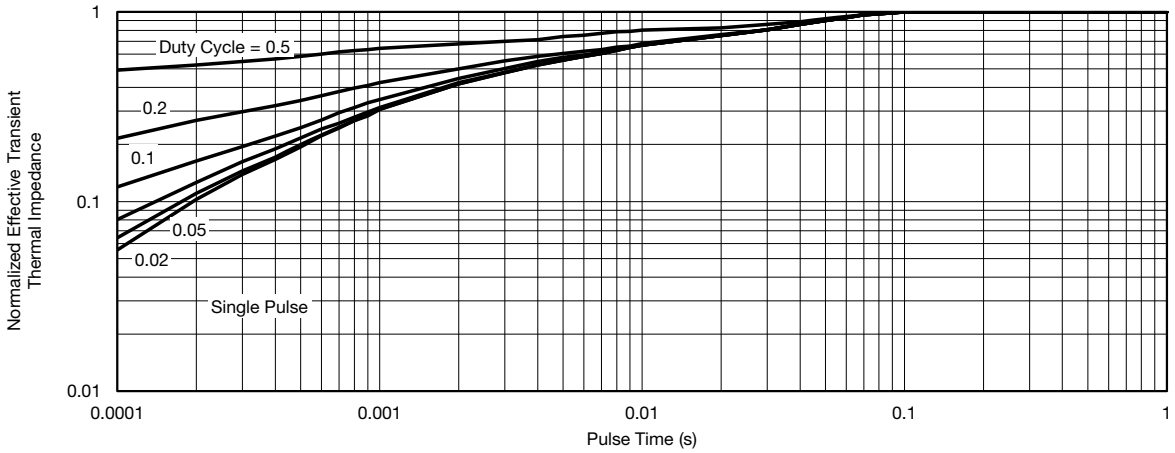



**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**

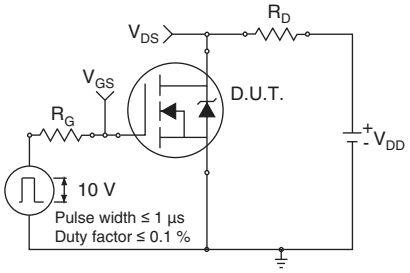



**Fig. 13 - Switching Time Test Circuit**

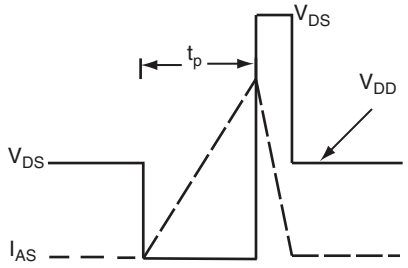



**Fig. 16 - Unclamped Inductive Waveforms**

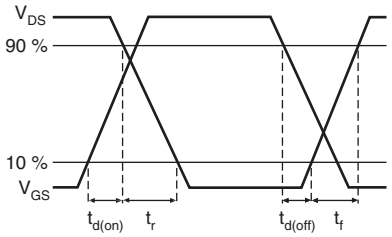



**Fig. 14 - Switching Time Waveforms**

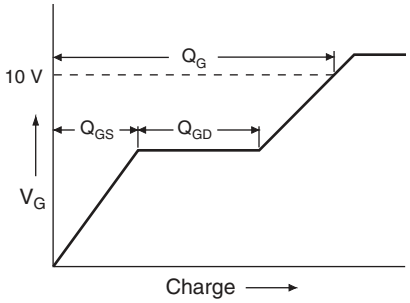



**Fig. 17 - Basic Gate Charge Waveform**

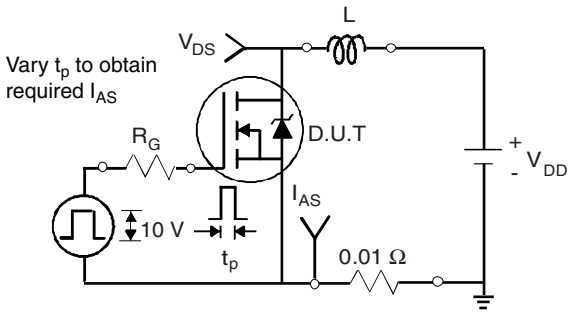



**Fig. 15 - Unclamped Inductive Test Circuit**

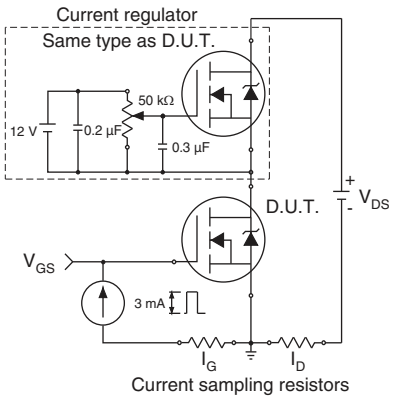
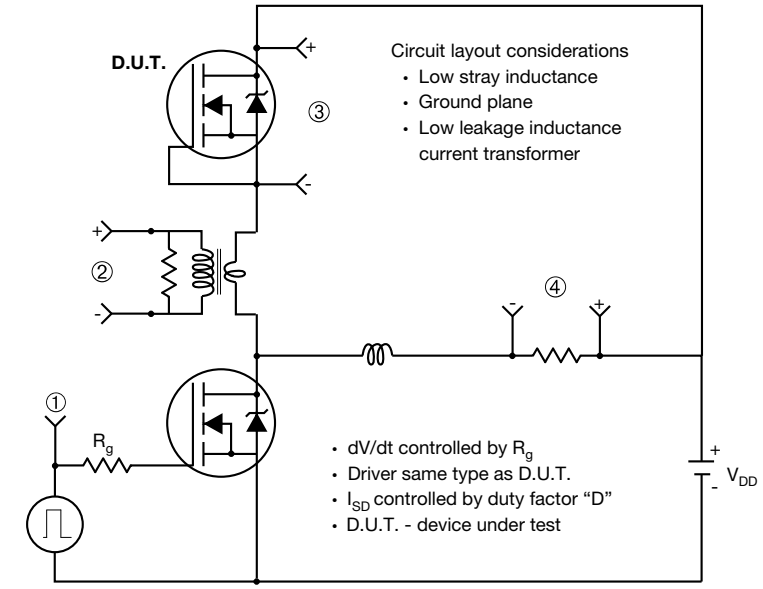
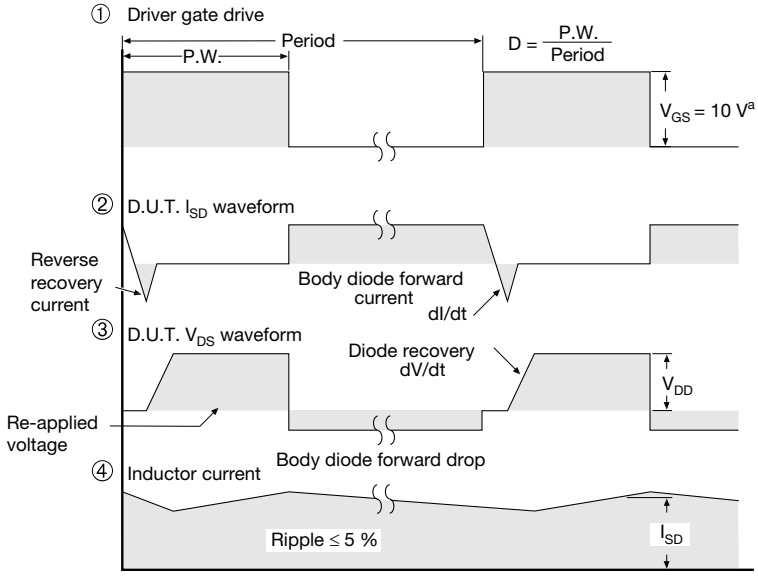



**Fig. 18 - Gate Charge Test Circuit**


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**Peak Diode Recovery dV/dt Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 19 - For N-Channel**

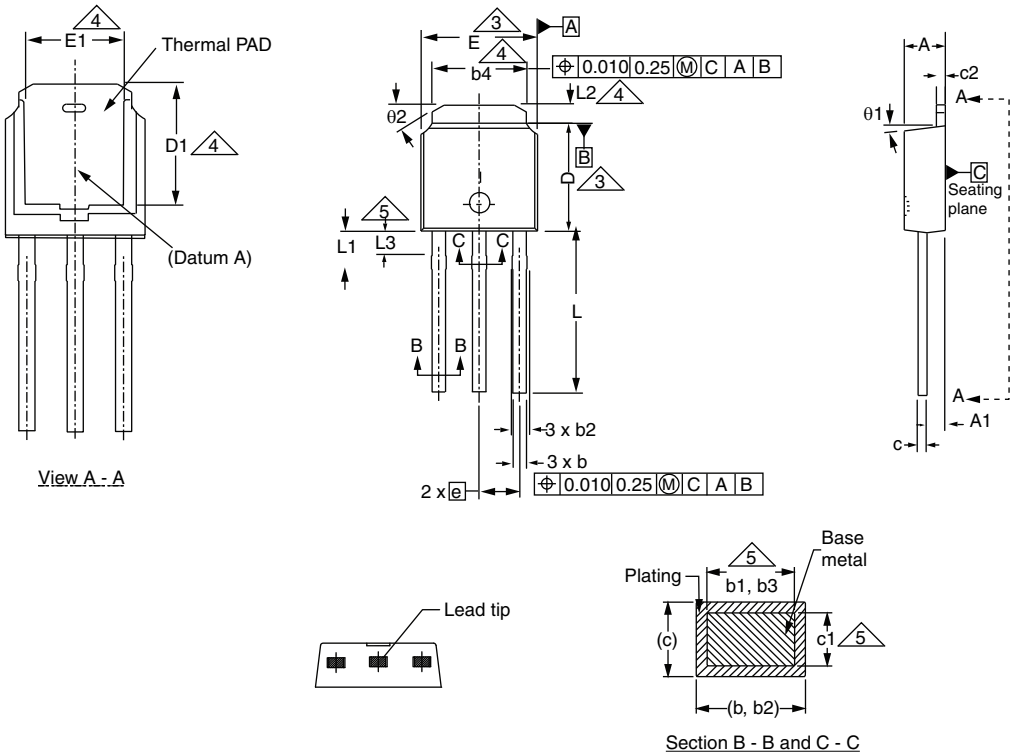
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# Case Outline for TO-251AA (High Voltage)

## OPTION 1:




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.39 | 0.086 | 0.094 |
| A1 | 0.89 | 1.14 | 0.035 | 0.045 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b1 | 0.65 | 0.79 | 0.026 | 0.031 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 0.76 | 1.04 | 0.030 | 0.041 |
| b4 | 4.95 | 5.46 | 0.195 | 0.215 |
| c | 0.46 | 0.61 | 0.018 | 0.024 |
| c1 | 0.41 | 0.56 | 0.016 | 0.022 |
| c2 | 0.46 | 0.86 | 0.018 | 0.034 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 5.21 | - | 0.205 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| e | 2.29 BSC | | 2.29 BSC | |
| L | 8.89 | 9.65 | 0.350 | 0.380 |
| L1 | 1.91 | 2.29 | 0.075 | 0.090 |
| L2 | 0.89 | 1.27 | 0.035 | 0.050 |
| L3 | 1.14 | 1.52 | 0.045 | 0.060 |
| θ1 | 0' | 15' | 0' | 15' |
| θ2 | 25' | 35' | 25' | 35' |

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

**Notes**

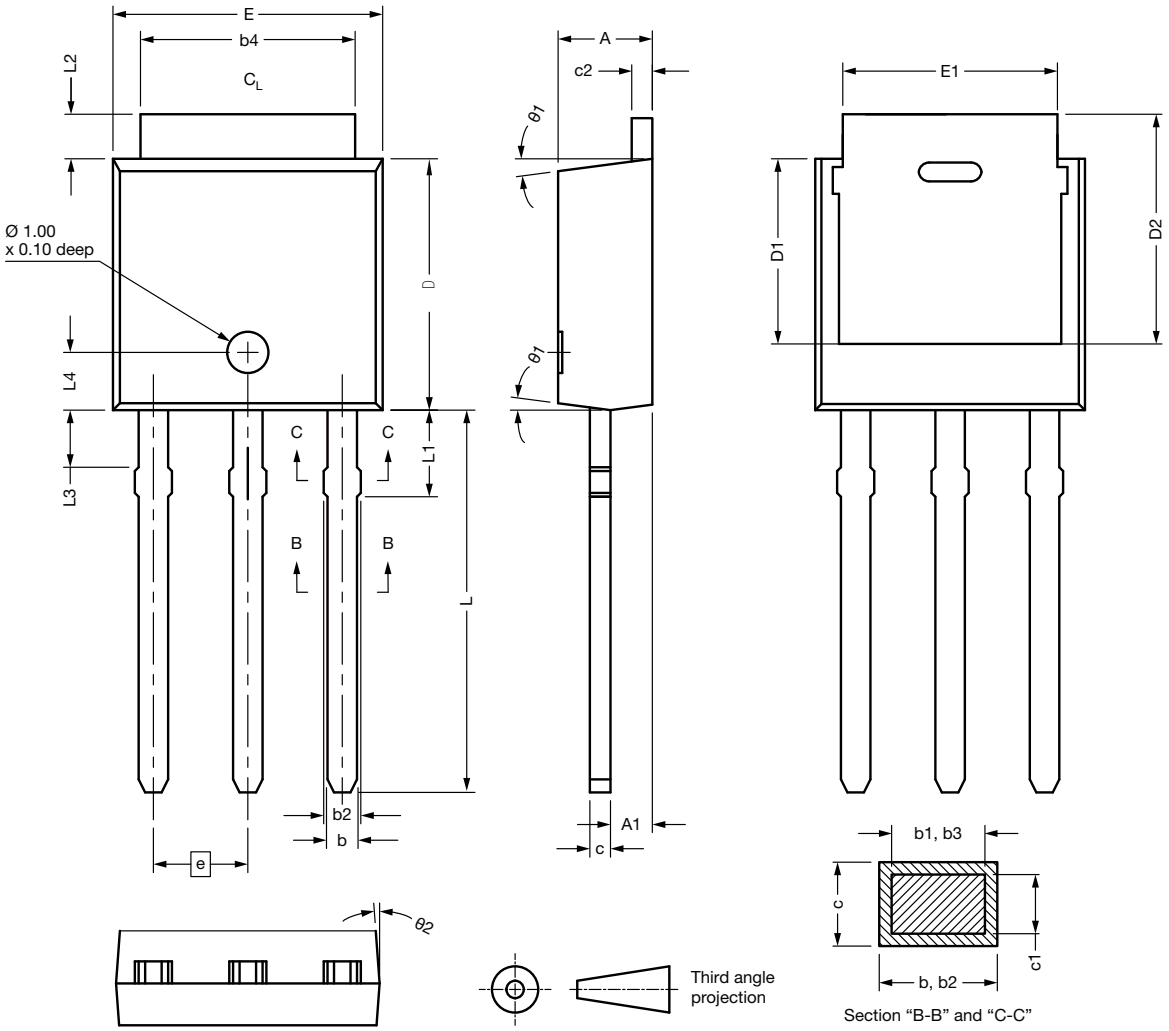
- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



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## OPTION 2: FACILITY CODE = N




| DIM. | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 2.180 | 2.285 | 2.390 |
| A1 | 0.890 | 1.015 | 1.140 |
| b | 0.640 | 0.765 | 0.890 |
| b1 | 0.640 | 0.715 | 0.790 |
| b2 | 0.760 | 0.950 | 1.140 |
| b3 | 0.760 | 0.900 | 1.040 |
| b4 | 4.950 | 5.205 | 5.460 |
| c | 0.460 | - | 0.610 |
| c1 | 0.410 | - | 0.560 |
| c2 | 0.460 | - | 0.610 |
| D | 5.970 | 6.095 | 6.220 |
| D1 | 4.300 | - | - |

| DIM. | MIN. | NOM. | MAX. |
|---|---|---|---|
| D2 | 5.380 | - | - |
| E | 6.350 | 6.540 | 6.730 |
| E1 | 4.32 | - | - |
| e | 2.29 BSC | | |
| L | 8.890 | 9.270 | 9.650 |
| L1 | 1.910 | 2.100 | 2.290 |
| L2 | 0.890 | 1.080 | 1.270 |
| L3 | 1.140 | 1.330 | 1.520 |
| L4 | 1.300 | 1.400 | 1.500 |
| θ1 | 0° | 7.5° | 15° |
| θ2 | 4° | - | - |

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

**Notes**

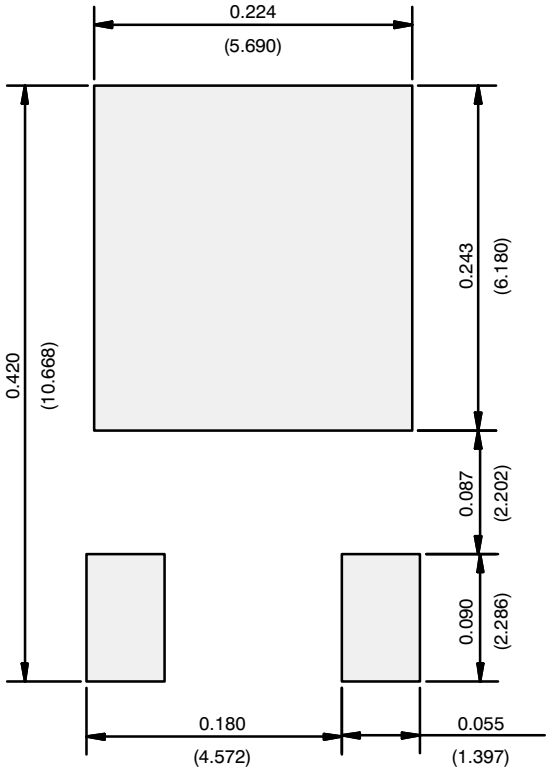
- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm



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## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)




Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE

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