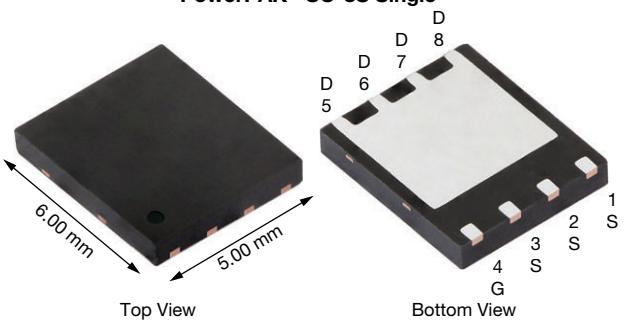
N-Channel 30 V (D-S) MOSFET

PowerPAK® SO-8S Single



Top View Bottom View

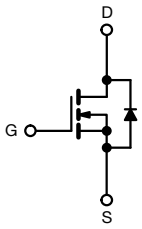
FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} x Q_g figure-of-merit (FOM)
- 100 % R_g and UIS tested
- Enhance power dissipation and lower R_{thJC}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Battery management



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00057
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00083
Q_g typ. (nC)	73
I_D (A) [a]	518
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8S
Lead (Pb)-free and halogen-free	SiRS4302DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage a		V_{GS}	+20, -16	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	518	A
	T_C = 70 °C		414	
	T_A = 25 °C		90 [b, c]	
	T_A = 70 °C		72 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	600	
Continuous source-drain diode current	T_C = 25 °C	I_S	223	
	T_A = 25 °C		6.7 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	65	
Single pulse avalanche energy		E_{AS}	211	mJ
Maximum power dissipation	T_C = 25 °C	P_D	245	W
	T_C = 70 °C		157	
	T_A = 25 °C		7.4 [b, c]	
	T_A = 70 °C		4.7 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b]	t ≤ 10 s	R_{thJA}	11	17	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.34	0.51	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 50 °C/W

For technical questions, contact: pmostechsupport@vishay.com

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 10 mA	-	18.1	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	-	-5.2	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.2	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	-	0.00047	0.00057	Ω
		V_{GS} = 4.5 V, I_D = 20 A	-	0.00065	0.00083	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	-	140	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	-	10150	-	pF
Output capacitance	C_{oss}		-	4325	-	
Reverse transfer capacitance	C_{rss}		-	300	-	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	-	153	230	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	-	73	110	
Gate-source charge	Q_{gs}		-	30	-	
Gate-drain charge	Q_{gd}		-	17	-	
Output charge	Q_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	-	118	-	
Gate resistance	R_g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω, $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	-	16	30	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	65	130	
Fall time	t_f		-	15	30	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω, $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	55	110	
Rise time	t_r		-	110	220	
Turn-off delay time	$t_{d(off)}$		-	60	120	
Fall time	t_f		-	30	60	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	189	A
Pulse diode forward current	I_{SM}		-	-	600	
Body diode voltage	V_{SD}	I_S = 10 A, V_{GS} = 0 V	-	0.70	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 10 A, di/dt = 100 A/µs, T_J = 25 °C	-	75	150	ns
Body diode reverse recovery charge	Q_{rr}		-	80	160	nC
Reverse recovery fall time	t_a		-	45	-	ns
Reverse recovery rise time	t_b		-	30	-	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

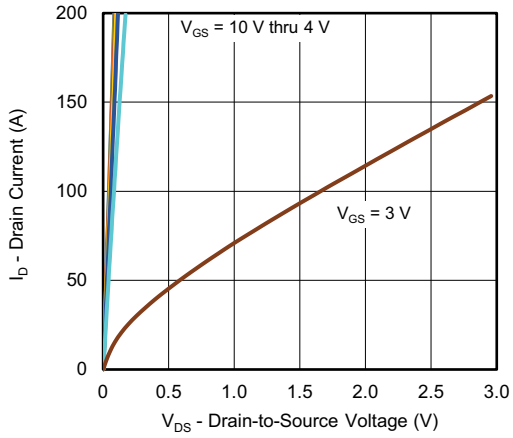
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

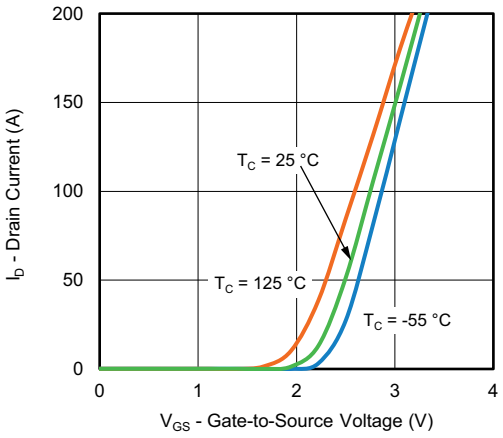
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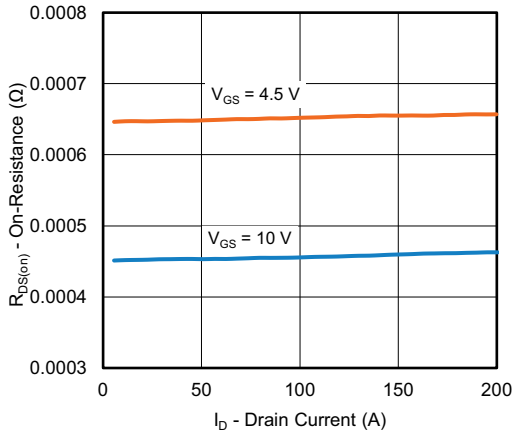
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



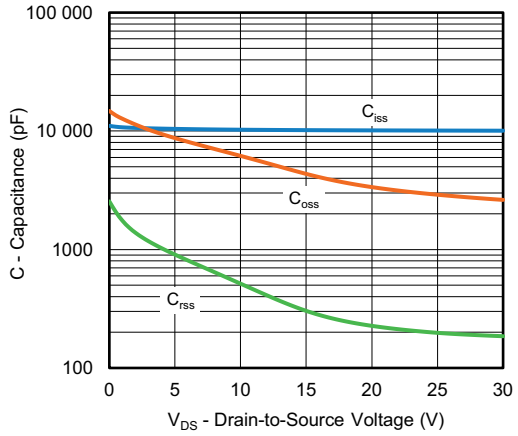
Output Characteristics



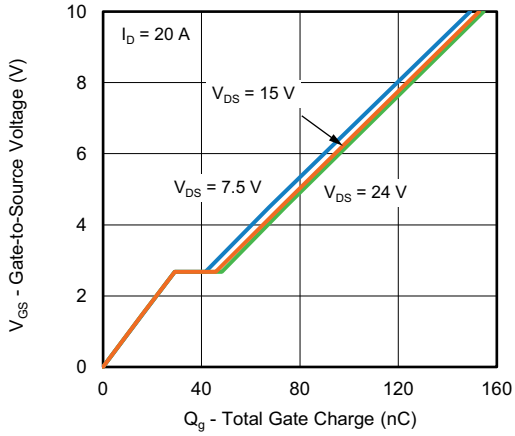
Transfer Characteristics



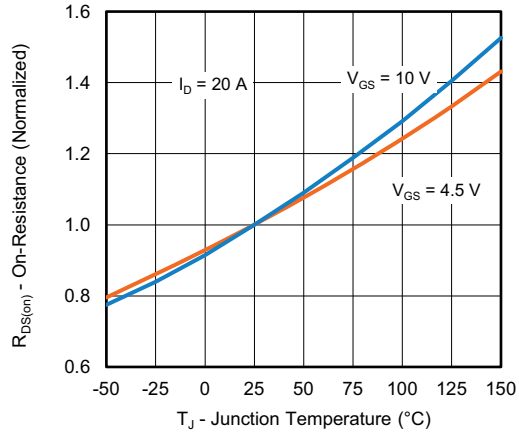
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



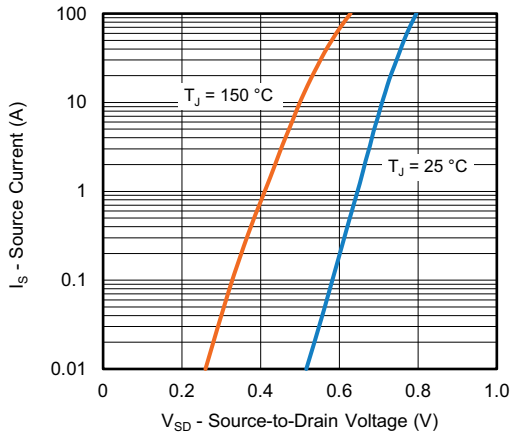
Gate Charge



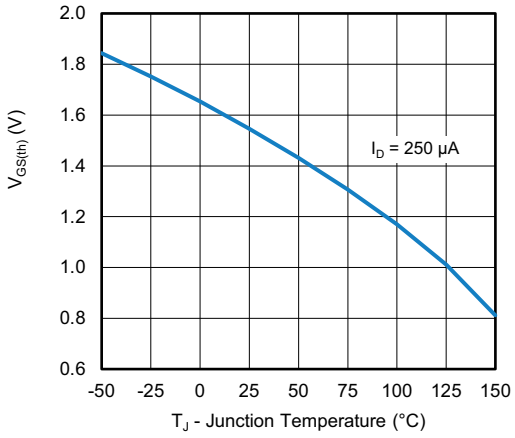
On-Resistance vs. Junction Temperature

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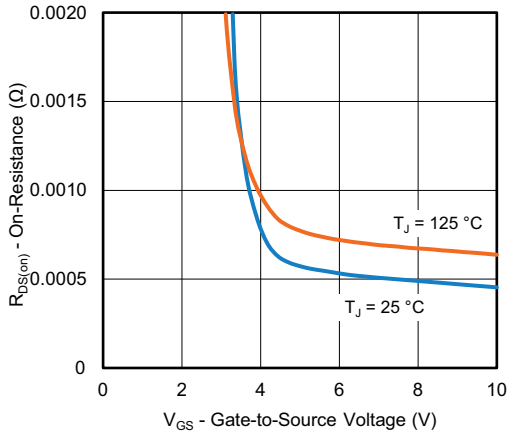
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



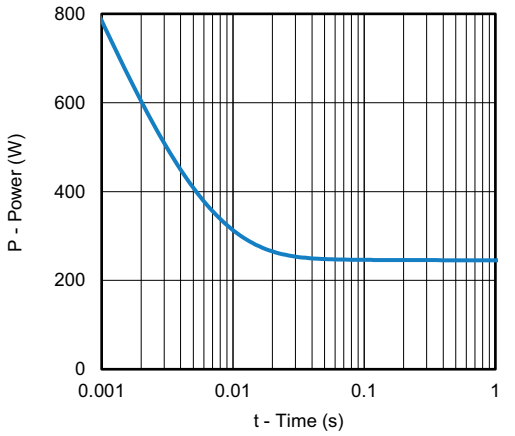
Source-Drain Diode Forward Voltage



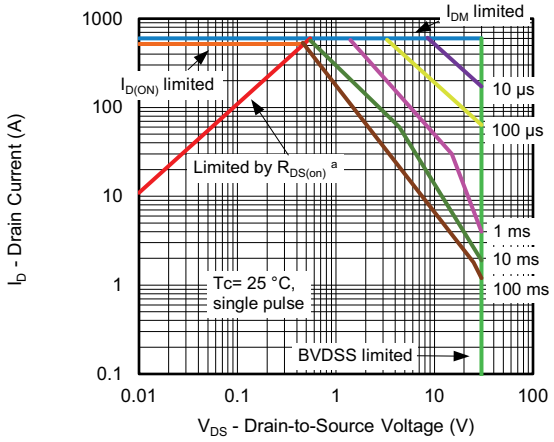
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



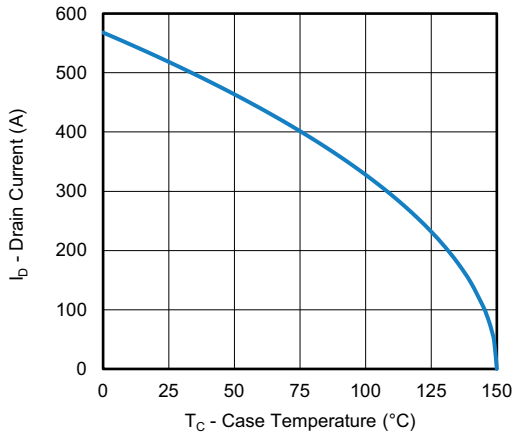
Safe Operating Area, Junction-to-Case

Note

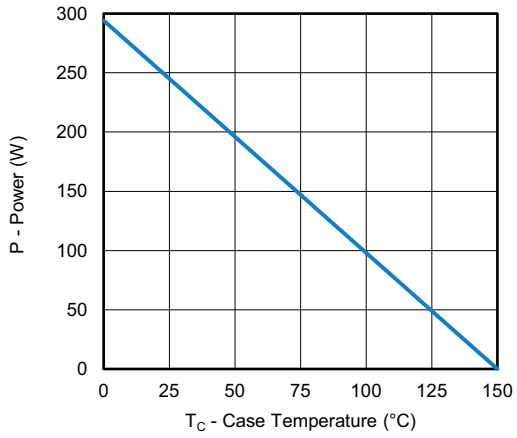
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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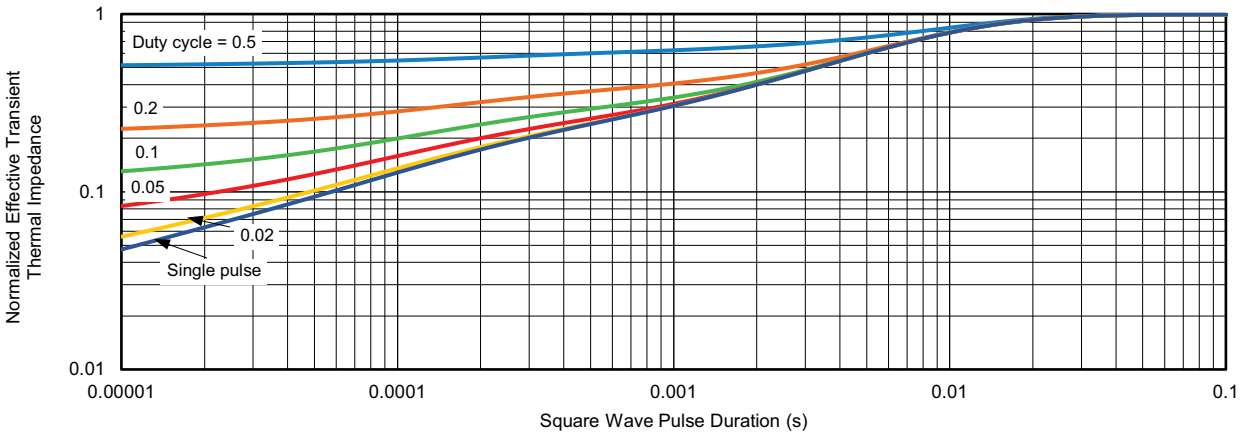
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

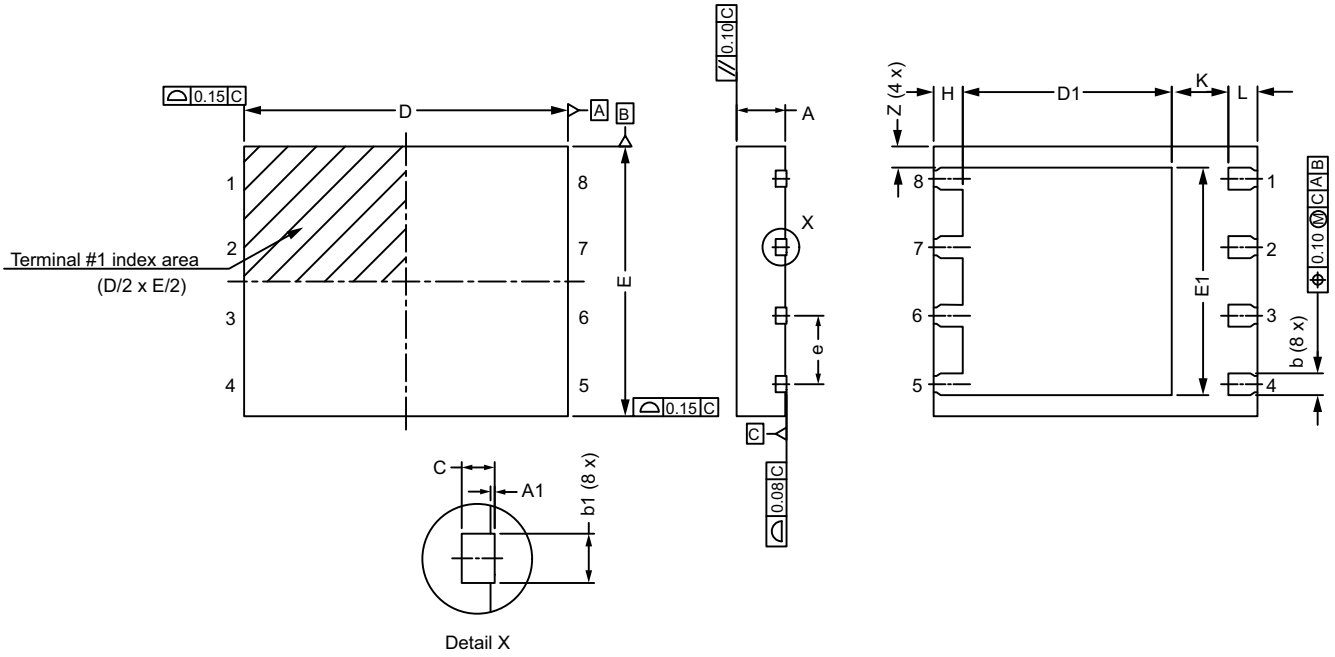
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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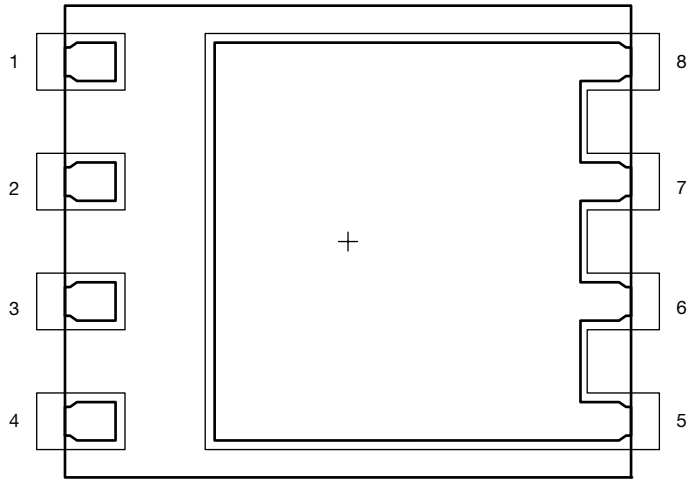
PowerPAK® SO-8S BWL

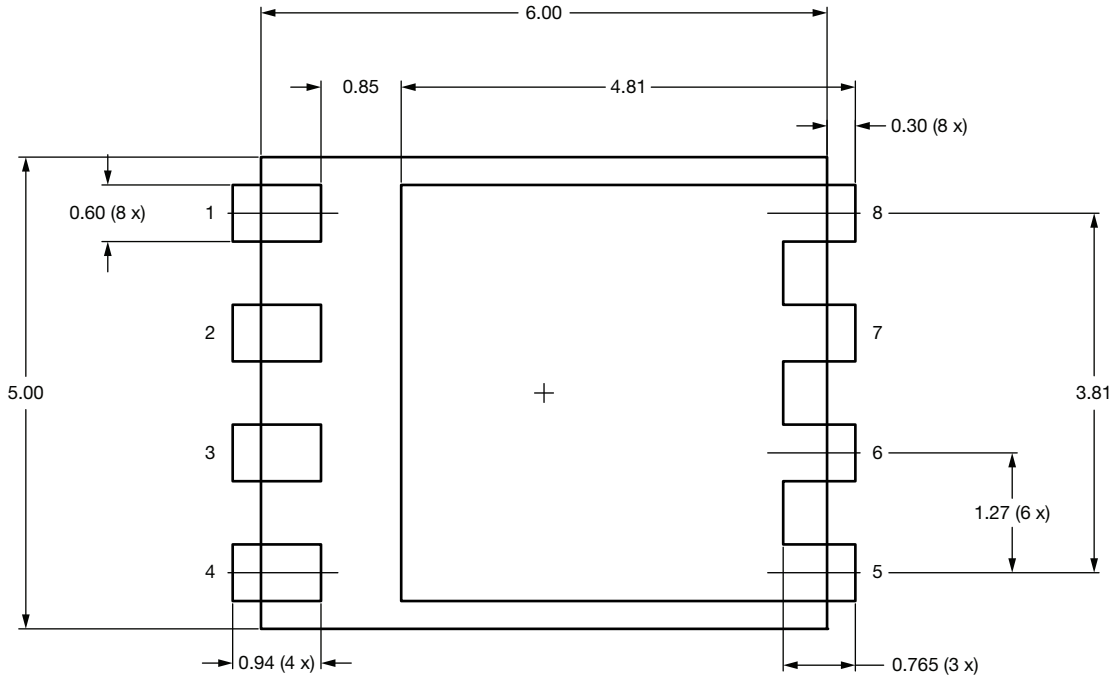


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	-	-	0.05	-	-	0.002
b	0.31	0.41	0.51	0.012	0.016	0.020
b1	0.20	0.30	0.40	0.008	0.012	0.016
c	0.20 ref.			0.008 ref.		
D	5.90	6.00	6.10	0.232	0.236	0.240
D1	3.78	3.88	3.98	0.149	0.153	0.157
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.12	4.22	4.32	0.162	0.166	0.170
e	1.27 BSC			0.050 BSC		
H	0.44	0.54	0.64	0.017	0.021	0.025
K	1.05 ref.			0.041 ref.		
L	0.44	0.54	0.64	0.017	0.021	0.025
Z	0.39 ref.			0.015 ref.		
ECN: C20-0936-Rev. A, 03-Aug-2020 DWG: 6082						

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Recommended Land Pattern PowerPAK® SO-8S BWL





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