Application Report
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TPS7A63xx-Q1 Configuration to Achieve Long-Reset Pulse Width When the Watchdog Detects a Fault

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ABSTRACT

The normal logic for the TPS7A63xx-Q1 window-watchdog LDO is that when detecting a fault from the input of watchdog, the watchdog output (WDO) will pull down for a duration equal to 1/5000-times the watchdog period. For some microcontrollers, the required minimum pulse-width to reset the microcontrollers correctly is several milliseconds, if the WDO is used to reset the microcontrollers at this moment, the watchdog period is too long (longer than 10 s) which is not applicable for automotive applications. This application note introduces a configuration that can achieve a long pulse width at the RESET pin when the watchdog detects a fault. This pulse width equals the power-on reset delay time which is adjustable through the capacitor connect at the DELAY pin.

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1 Watchdog Linear Regulator Application

Internal watchdogs are built into the central processing unit (CPU) of most embedded processor devices that include high-integration peripherals. However, these watchdog timers are not reliable because uncontrolled, or *runaway*, software can reprogram the internal watchdog-timer controller. A reliable watchdog must be independent of the CPU that is protected by the watchdog.

To achieve a better application-specific integrated circuit (ASIC) for automotive systems, an external window watchdog is required to monitor the operating status of the microcontroller. The TPS7A63xx-Q1 device is a linear regulator with an integrated window watchdog. This device is suitable for as an automotive microcontroller power-supply.

Figure 1 shows a typical application diagram of the TPS7A63xx-Q1 device powering an MCU with an edge-detection reset function. The microcontroller sends a clock signal with stable frequency to the WD pin during normal operation status. If a fault occurs with the microcontroller, the output clock signal frequency will be abnormal which causes the WD_FLT pin to pull down for a short period, $t_{(WD_OUT)}$. The microcontroller is either interrupted or reset after detecting the drop edge from the WD_FLT or RESET pin (the RESET pin pulls down when the output voltage of the TPS7A63xx-Q1 device drops below 90% of the normal value).

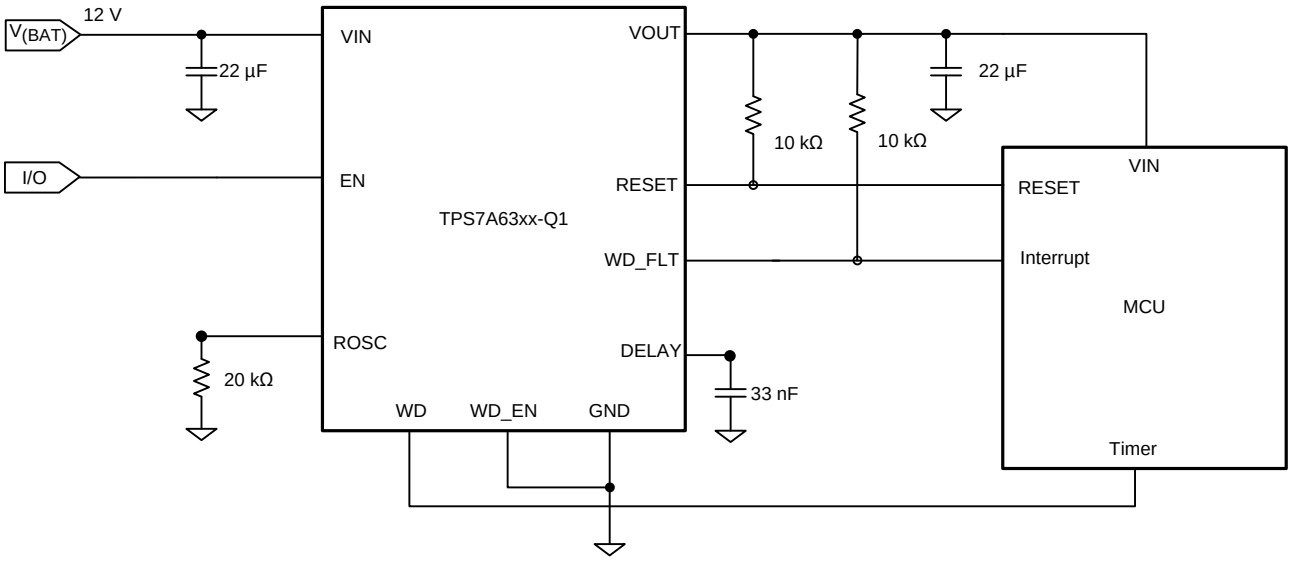

Figure 1. MCU With Edge-Detection Reset

Use Equation 1 to calculate the WD_FLT pulldown period, $t_{(WD_OUT)}$, when the watchdog detects a fault.

$$t_{(WD_OUT)} = t_{(WD)} / 5000 \quad (1)$$

The window watchdog period, $t_{(WD)}$, is programmed through the resistor connected at the ROSC pin and ranges from several milliseconds to dozens of milliseconds in most automotive applications. In this case, the $t_{(WD_OUT)}$ is at microsecond level.

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2 TPS7A63xx-Q1 Configuration to Achieve Long Reset Pulse Width When the Watchdog Detects a Fault

2.1 Configuration Graph

For some microcontrollers, 10 ms is the minimum pulse width required to correctly reset the microcontroller. If the microcontroller is not reset within this time, it might regard the short low-level pulse from the WD_FLT pin as noise and ignore the pulse. At this moment, if the WD_FLT signal is used to reset the microcontroller, $t_{(WD_OUT)}$ must be longer than 10 ms which means the window watchdog period $t_{(WD)}$ must be longer than $t_{(WD_OUT)}$ × 5000 = 50 s. A 50-s watchdog period is not acceptable for any application.

Figure 2 shows the TPS7A63xx-Q1 configuration to achieve a long fault-signal output to microcontroller without increasing the window watchdog period when the watchdog detects a fault. In such configuration, when the watchdog detects a fault, the RESET voltage pulls down for a duration equal to the power-on reset delay-time which is programmable through the capacitor connected at the DELAY pin. At the same time, the watchdog period is adjustable through the resistor connected at the ROSC pin.

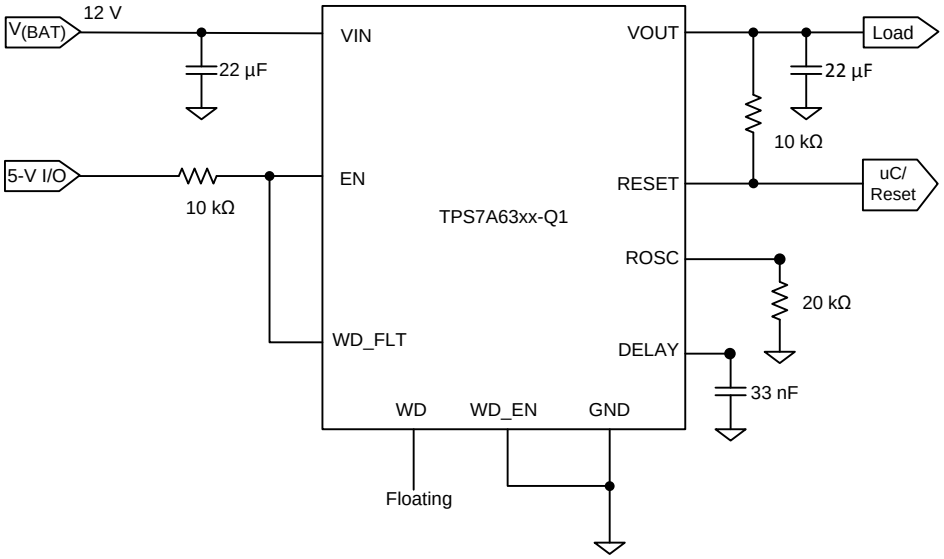

Figure 2. TPS7A63xx-Q1 Configuration to Achieve a Long Reset Pulse-Width When the Watchdog Detects a Fault

2.2 Configuration Details

The following lists the details of the configuration:

- The EN pin is connect to the WD_FLT pin and the watchdog function is enabled with the WD_EN pin connected to ground.
- The WD pin is floating without any input signal which causes the watchdog to report faults periodically.
- 12 V is applied at the VIN pin and 5 V is connected to the EN pin through a 10-kΩ resistor.
- A 20-kΩ resistor is connected at the ROSC pin. The window watchdog width is equal to: $t_{(wd)} = 10^{-6} \times 20000 = 20$ ms
- A 33-nF capacitor is connected at the DELAY pin. The power-on reset delay-time is equal to: $t_{d(RESET)} = 100$ ms

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2.3 Test Results

2.3.1 No Load Applied at VOUT

Figure 3 shows the response of the EN, WD_FLT, RESET, and DELAY pins when the WD pin is floating. After the window watchdog initializes, which is equal to eight-times $t_{(WD)}$ 160 ms, the RESET voltage is pulled down to the ground because no rising edge is detected from the WD pin during the initialization of the watchdog. As soon as the RESET pin pulls down, the voltage at the DELAY pin begins to increase which means the capacitor at the DELAY pin is charging through the TPS7A63xx-Q1 device. The charging occurs because the device is reenabled as shown in Figure 4. After approximately 100 ms (which is equal to the power-on reset delay-time) the voltage at the DELAY pin increase to 3 V which leads to the RESET voltage pulling high again.

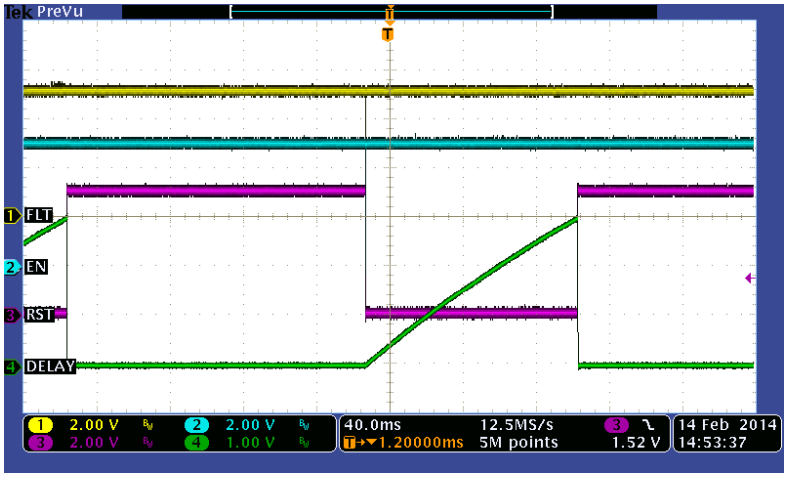

Figure 3. TPS7A63xx-Q1 Response When the WD Fault Mode is Triggered, I_O = 0 mA

Figure 4 is the amplified waveform in Figure 3 with 400-ns time units. When the watchdog detects a fault, the WD_FLT pin drops to 0 V which causes the EN pin voltage to drop as well because the pins are shorted and the TPS7A63xx-Q1 device is disabled. The reset logic circuit is also disabled which causes the voltage at the RESET pin to immediately drop to 0 V.

The EN and WD_FLT pins both go to the high impedance state in disable mode and the 5-V I/O begins to charge the EN and WD_FLT pin voltages through the 10-kΩ resistor as soon as the TPS7A63xx-Q1 device is disabled. The charging speed is relatively fast because no capacitor is connected at the EN and WD_FLT pins. When the EN voltage is higher than the high active threshold and the output voltage is higher than 93% of the nominal value, the device begins to charge the capacitor connected at the DELAY pin. The RESET voltage is pulled high to $V_{(OUT)}$ when $V_{(DELAY)}$ reaches the 3-V threshold.

NOTE: The output voltage does not drop below the 93% threshold when a fault occurs at light loads because the capacitor does not have enough time to discharge.

In this case, a 100-ms low pulse-width at the RESET pin is achieved which is equal to the power-on reset delay-time of the TPS7A63xx-Q1 device. The reset pulse width can be adjusted through the capacitor value connected at the DELAY pin according to the requirement of the application.

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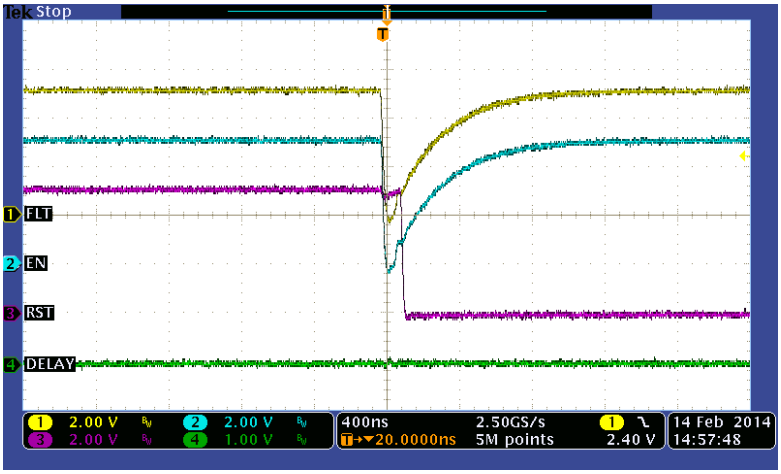

Figure 4. TPS7A63xx Response Waveform With 400-ns Time Units

Figure 5 includes the VOUT waveform because no load applies at VOUT and therefore almost no voltage spike occurs at VOUT.

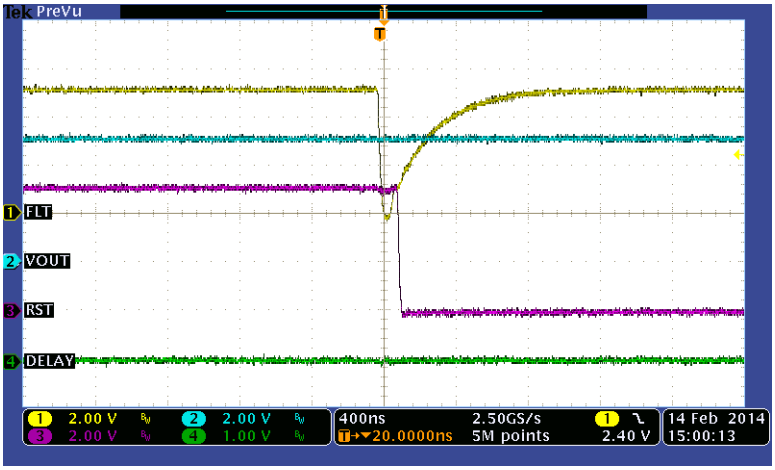

Figure 5. TPS7A63xx-Q1 Response When the WD Fault Mode is Triggered, I_O = 0 mA

2.3.2 300-mA Load is Applied at VOUT (16-Ω Resistor Connected at VOUT)

When a watchdog fault occurs at a 300-mA load, the only difference compared to a no-load condition is that output voltage drops a little after the TPS7A63xx-Q1 device disables. The output capacitor begins to discharge with a 300-mA current when the device is disabled. Figure 7 shows that when the TPS7A63xx-Q1 device is reenabled, the output voltage continues to drop for an additional 100 us because an internal circuit must be prepared after the voltage at the EN pin reaches the active threshold which takes about 100 µs. When these circuits are ready, the internal power MOSFET is turned ON the output voltage stops dropping.

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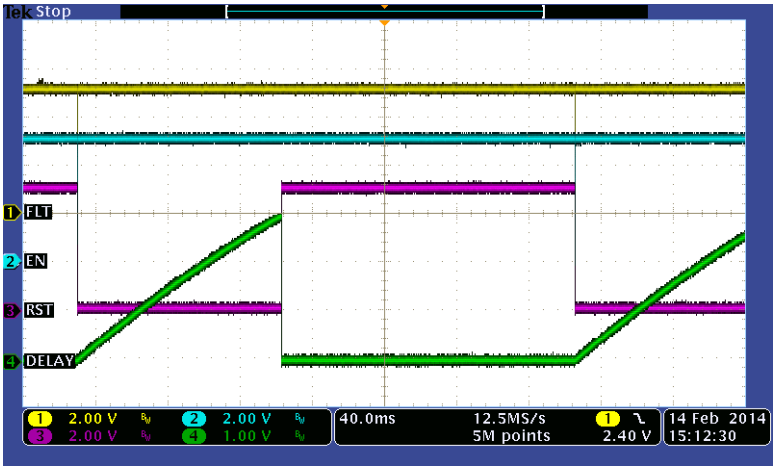

Figure 6. TPS7A63xx Response With 40-ms Time Units, I_O = 300 mA

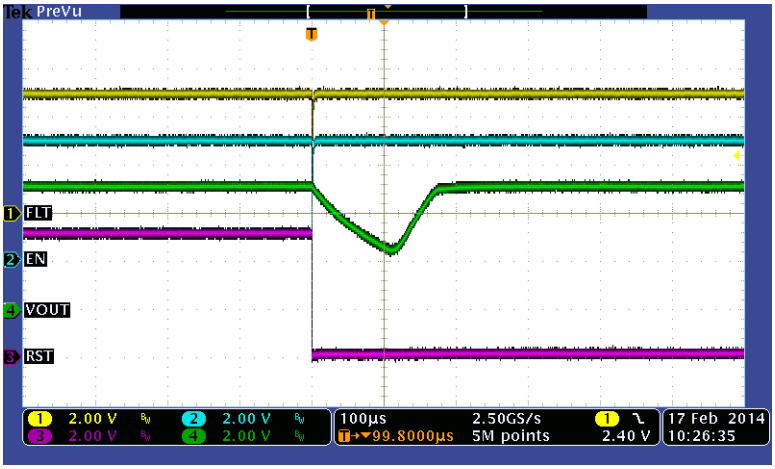

Figure 7. TPS7A63xx VOUT Response With 200-µs Time Units, I_O = 300 mA

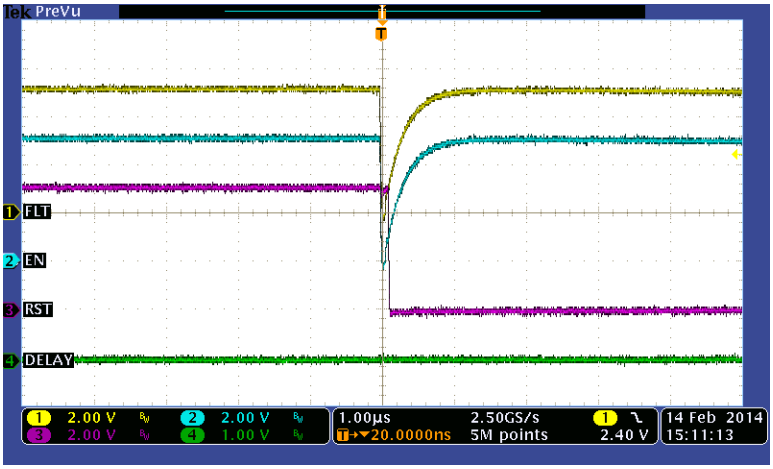

Figure 8. TPS7A63xx Response With 1-µs Time Units, I_O = 300 mA

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3 Conclusion

In conclusion, the test results confirm that the configuration shown in Figure 2 is applicable. When a fault is detected by the watchdog, the RESET pin pulls down for a duration equal to the power-on reset delay-time. The user can adjust the RESET pulldown duration through the capacitor connected at the DELAY pin.

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