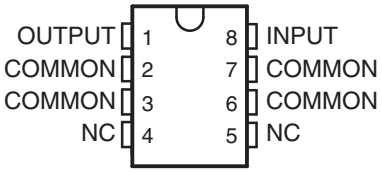
LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

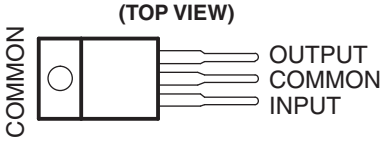
- Very Low Dropout Voltage, Less Than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751L Series
- 60-V Load-Dump Protection
- Reverse Transient Protection Down to –50 V
- Internal Thermal-Overload Protection
- Overvoltage Protection
- Internal Overcurrent-Limiting Circuitry
- Less Than 500-µA Disable (TL751L Series)

TL750L . . . D PACKAGE
(TOP VIEW)

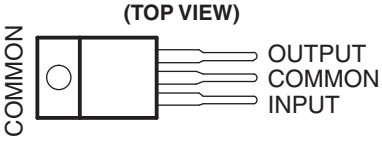


NC – No internal connection

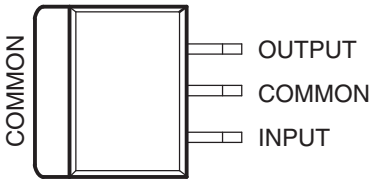
TL750L . . . KC PACKAGE
(TOP VIEW)



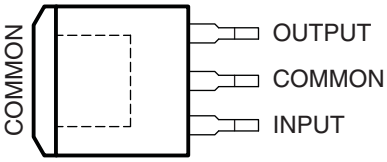
TL750L . . . KCS PACKAGE
(TOP VIEW)



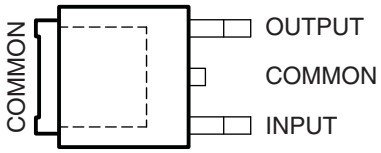
TL750L . . . KTE PACKAGE
(TOP VIEW)



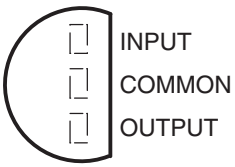
TL750L . . . KTT PACKAGE
(TOP VIEW)



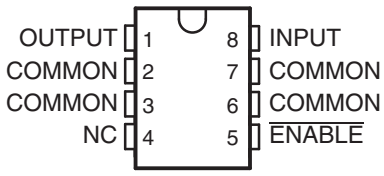
TL750L . . . KVU PACKAGE
(TOP VIEW)



TL750L . . . LP PACKAGE
(TO-92, TO-226AA)
(TOP VIEW)

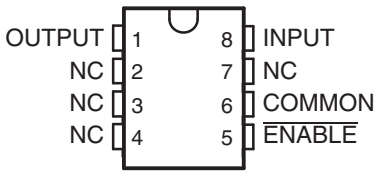


TL751L . . . D PACKAGE
(TOP VIEW)



NC – No internal connection

TL751L . . .P PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TL750L and TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. The TL751L series also has an enable (ENABLE) input. When ENABLE is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION(1)

T_J	V_O TYP AT 25°C	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5 V	PowerFLEX™ – KTE	Reel of 2000	TL750L05CKTER	TL750L05C
		SOIC – D	Tube of 75	TL750L05CD	50L05C
			Reel of 2500	TL750L05CDR	
			Tube of 75	TL751L05CD	51L05C
			Reel of 2500	TL751L05CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L05CLP	750L05C
			Reel of 2000	TL750L05CLPR	
		TO-220 – KC	Tube of 50	TL750L05CKC	TL750L05C
		TO-220 – KCS	Tube of 50	TL750L05CKCS	TL750L05C
		TO-252 – KVU	Reel of 2500	TL750L05CKVUR	750L05C
		TO-263 – KTT	Reel of 500	TL750L05CKTTR	750L05C
	8 V	SOIC – D	Tube of 75	TL750L08CD	50L08C
			Reel of 2500	TL750L08CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L08CLP	750L08C
	10 V	PDIP – P	Tube of 50	TL751L10CP	TL751L10C
		SOIC – D	Tube of 75	TL750L10CD	50L10C
			Reel of 2500	TL750L10CDR	
			Tube of 75	TL751L10CD	51L10C
			Reel of 2500	TL751L10CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L10CLP	750L10C
			Reel of 2000	TL750L10CLPR	
	12 V	SOIC – D	Tube of 75	TL750L12CD	50L12C
			Reel of 2500	TL750L12CDR	
			Tube of 75	TL751L12CD	51L12C
			Reel of 2500	TL751L12CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L12CLP	750L12C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

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Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Continuous input voltage			26	V
	Transient input voltage(2)	T_A = 25°C		60	V
	Continuous reverse input voltage			–15	V
	Transient reverse input voltage	t ≤ 100 ms		–50	V
T_J	Operating virtual junction temperature			150	°C
	Lead temperature	1,6 mm (1/16 in) for 10 s		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The transient input voltage rating applies to the waveform shown in Figure 1.

Package Thermal Data(1)

PACKAGE	BOARD	θ_{JC}	θ_{JA}
PDIP (P)	High K, JESD 51-7	57°C/W	85°C/W
PowerFLEX™ (KTE)	High K, JESD 51-5	3°C/W	23°C/W
SOIC (D)	High K, JESD 51-7	39°C/W	97°C/W
TO-226/TO-92 (LP)	High K, JESD 51-7	55°C/W	140°C/W
TO-220 (KC)	High K, JESD 51-5	3°C/W	19°C/W
TO-220 (KCS)	High K, JESD 51-5	3°C/W	19°C/W
TO-252 (KVU)	High K, JESD 51-5	–	30.3°C/W
TO-263 (KTT)	High K, JESD 51-5	18°C/W	25.3°C/W

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Recommended Operating Conditions

over recommended operating junction temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_I	Input voltage		TL75xL05	6	26	V
			TL75xL08	9	26	
			TL75xL10	11	26	
			TL75xL12	13	26	
V_{IH}	High-level $\overline{\text{ENABLE}}$ input voltage		TL75xLxx	2	15	V
V_{IL} (1)	Low-level $\overline{\text{ENABLE}}$ input voltage	T_J = 25°C	TL75xLxx	–0.3	0.8	V
		T_J = 0°C to 125°C	TL75xLxx	–0.15	0.8	
I_O	Output current		TL75xLxx	0	150	mA
T_J	Operating virtual junction temperature		TL75xLxxC	0	125	°C

(1) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

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TL75xL05 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L05 TL751L05			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	4.8	5	5.2	V
		T_J = 0°C to 125°C	4.75		5.25	
Input regulation voltage	V_I = 9 V to 16 V			5	10	mV
	V_I = 6 V to 26 V			6	30	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			20	50	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 6 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TL75xL08 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L08 TL751L08			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	7.68	8	8.32	V
		T_J = 0°C to 125°C	7.6		8.4	
Input regulation voltage	V_I = 10 V to 17 V			10	20	mV
	V_I = 9 V to 26 V			25	50	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			40	80	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 9 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

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TL75xL10 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L10 TL751L10			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
Input regulation voltage	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TL75xL12 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L12 TL751L12			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.52	12	12.48	V
		T_J = 0°C to 125°C	11.4		12.6	
Input regulation voltage	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

PARAMETER MEASUREMENT INFORMATION

The TL750L, TL751L series are low-dropout regulators. This means that capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and its equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and temperature range. Figure 1 shows the recommended range of ESR for a given load with a 10-μF capacitor on the output.

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TYPICAL CHARACTERISTICS

TL750L05
EQUIVALENT SERIES RESISTANCE
vs
LOAD CURRENT

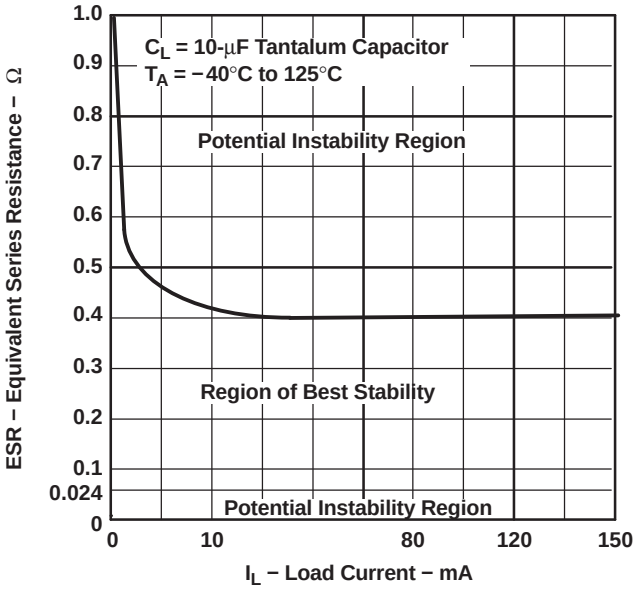


Figure 1.

TRANSIENT INPUT VOLTAGE
vs
TIME

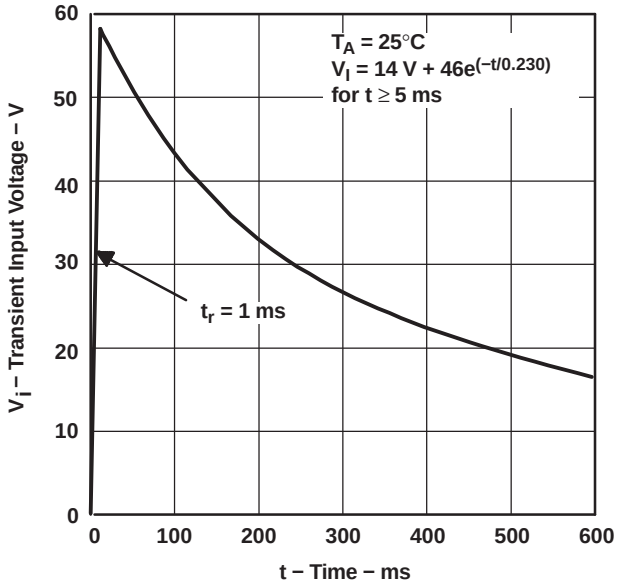


Figure 2.

TL750L05
INPUT CURRENT
vs
INPUT VOLTAGE

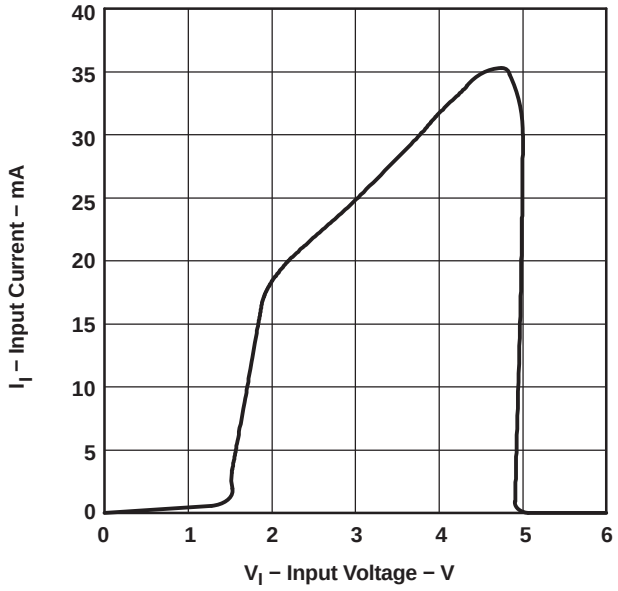


Figure 3.

TL750L12
INPUT CURRENT
vs
INPUT VOLTAGE

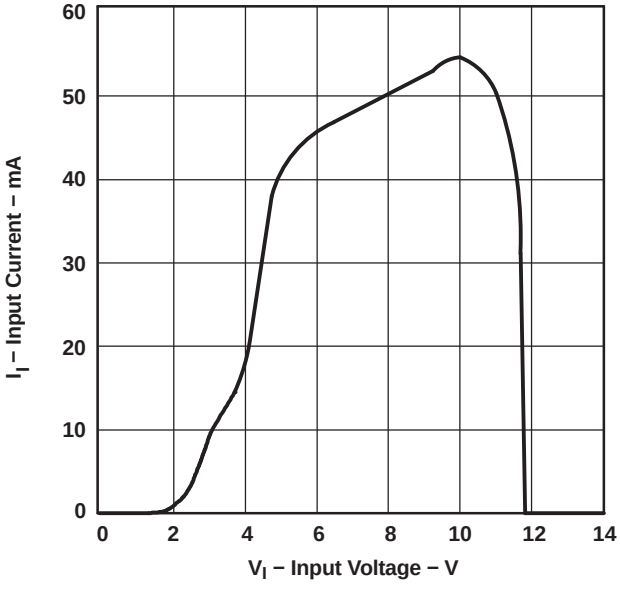


Figure 4.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL750L05CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C
TL750L05CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C
TL750L05CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C
TL750L05CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L05C
TL750L05CKCS	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750L05C
TL750L05CKCS.A	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750L05C
TL750L05CKCSE3	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750L05C
TL750L05CKTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TL750L05C
TL750L05CKTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TL750L05C
TL750L05CKTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TL750L05C
TL750L05CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	750L05C
TL750L05CKVURG3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	750L05C
TL750L05CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L05C
TL750L05CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L05C
TL750L05CLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L05C
TL750L05CLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	750L05C
TL750L05CLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	750L05C
TL750L05CLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	750L05C
TL750L08CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C
TL750L08CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C
TL750L08CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C
TL750L08CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	50L08C
TL750L08CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L08C
TL750L08CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L08C
TL750L08CLPE3	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L08C
TL750L10CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C
TL750L10CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL750L10CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C
TL750L10CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L10C
TL750L10CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L10C
TL750L10CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L10C
TL750L10CLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	750L10C
TL750L10CLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	750L10C
TL750L12CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C
TL750L12CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C
TL750L12CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C
TL750L12CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	50L12C
TL750L12CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L12C
TL750L12CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	750L12C
TL751L05CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C
TL751L05CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C
TL751L05CDE4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C
TL751L05CDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C
TL751L05CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C
TL751L05CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L05C
TL751L10CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L10C
TL751L10CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L10C
TL751L10CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L10C
TL751L10CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L10C
TL751L10CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 125	TL751L10C
TL751L10CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 125	TL751L10C
TL751L12CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C
TL751L12CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C
TL751L12CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C
TL751L12CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C
TL751L12CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	51L12C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

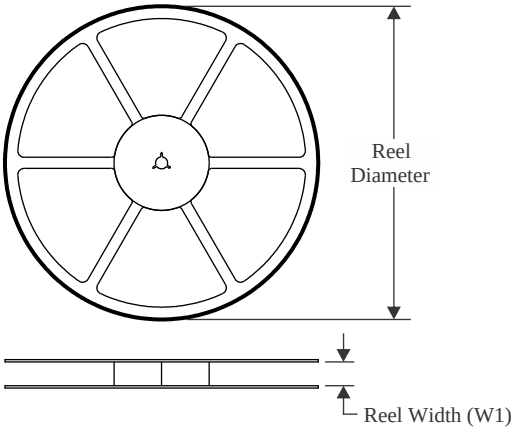
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

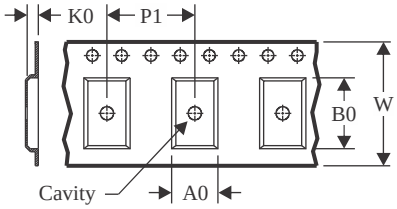
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

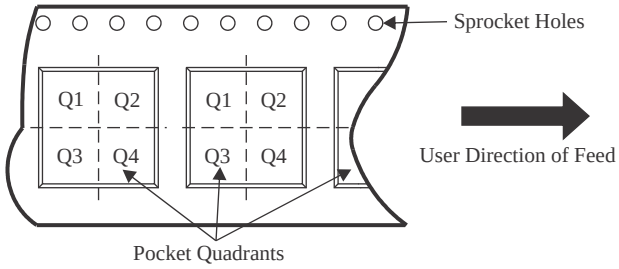


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

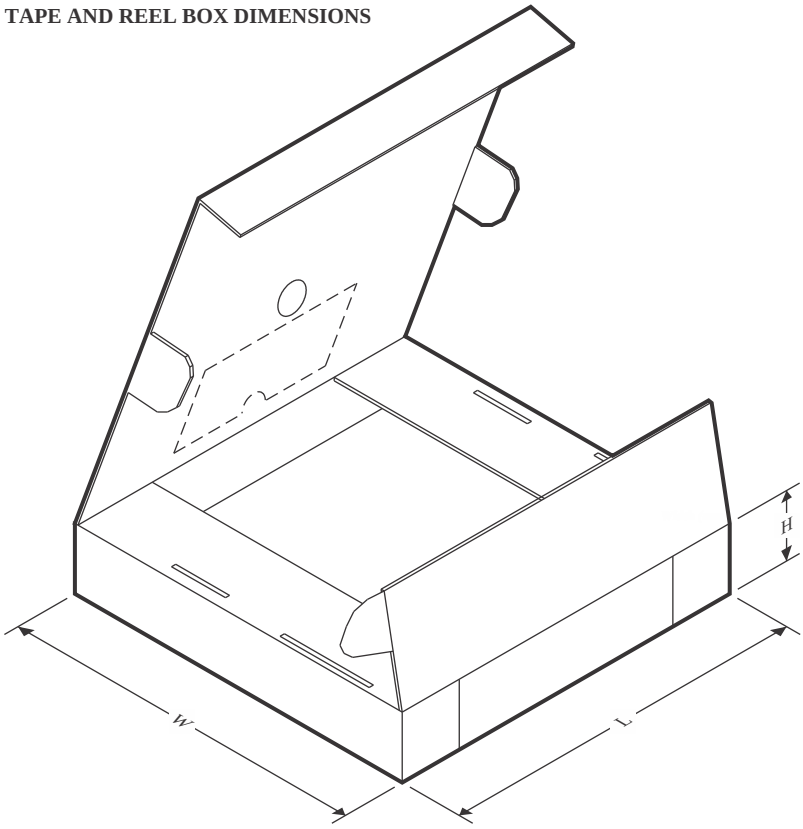
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L05CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL750L05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750L08CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L10CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L12CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L10CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L12CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

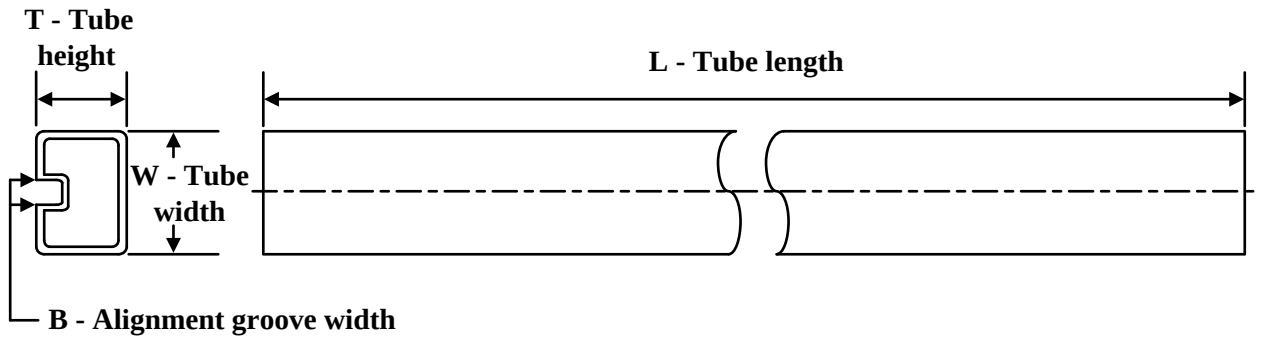
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

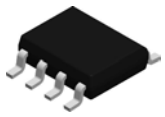
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750L05CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL750L05CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750L05CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750L08CDR	SOIC	D	8	2500	340.5	338.1	25.0
TL750L10CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L12CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL751L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L10CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L12CDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL750L05CD	D	SOIC	8	75	507	8	3940	4.32
TL750L05CD.A	D	SOIC	8	75	507	8	3940	4.32
TL750L05CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TL750L05CKCS.A	KCS	TO-220	3	50	532	34.1	700	9.6
TL750L05CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TL750L08CD	D	SOIC	8	75	507	8	3940	4.32
TL750L08CD.A	D	SOIC	8	75	507	8	3940	4.32
TL750L10CD	D	SOIC	8	75	507	8	3940	4.32
TL750L10CD.A	D	SOIC	8	75	507	8	3940	4.32
TL750L12CD	D	SOIC	8	75	507	8	3940	4.32
TL750L12CD.A	D	SOIC	8	75	507	8	3940	4.32
TL751L05CD	D	SOIC	8	75	507	8	3940	4.32
TL751L05CD.A	D	SOIC	8	75	507	8	3940	4.32
TL751L05CDE4	D	SOIC	8	75	507	8	3940	4.32
TL751L05CDG4	D	SOIC	8	75	507	8	3940	4.32
TL751L10CD	D	SOIC	8	75	507	8	3940	4.32
TL751L10CD.A	D	SOIC	8	75	507	8	3940	4.32
TL751L10CP	P	PDIP	8	50	506	13.97	11230	4.32
TL751L10CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL751L12CD	D	SOIC	8	75	507	8	3940	4.32
TL751L12CD.A	D	SOIC	8	75	507	8	3940	4.32

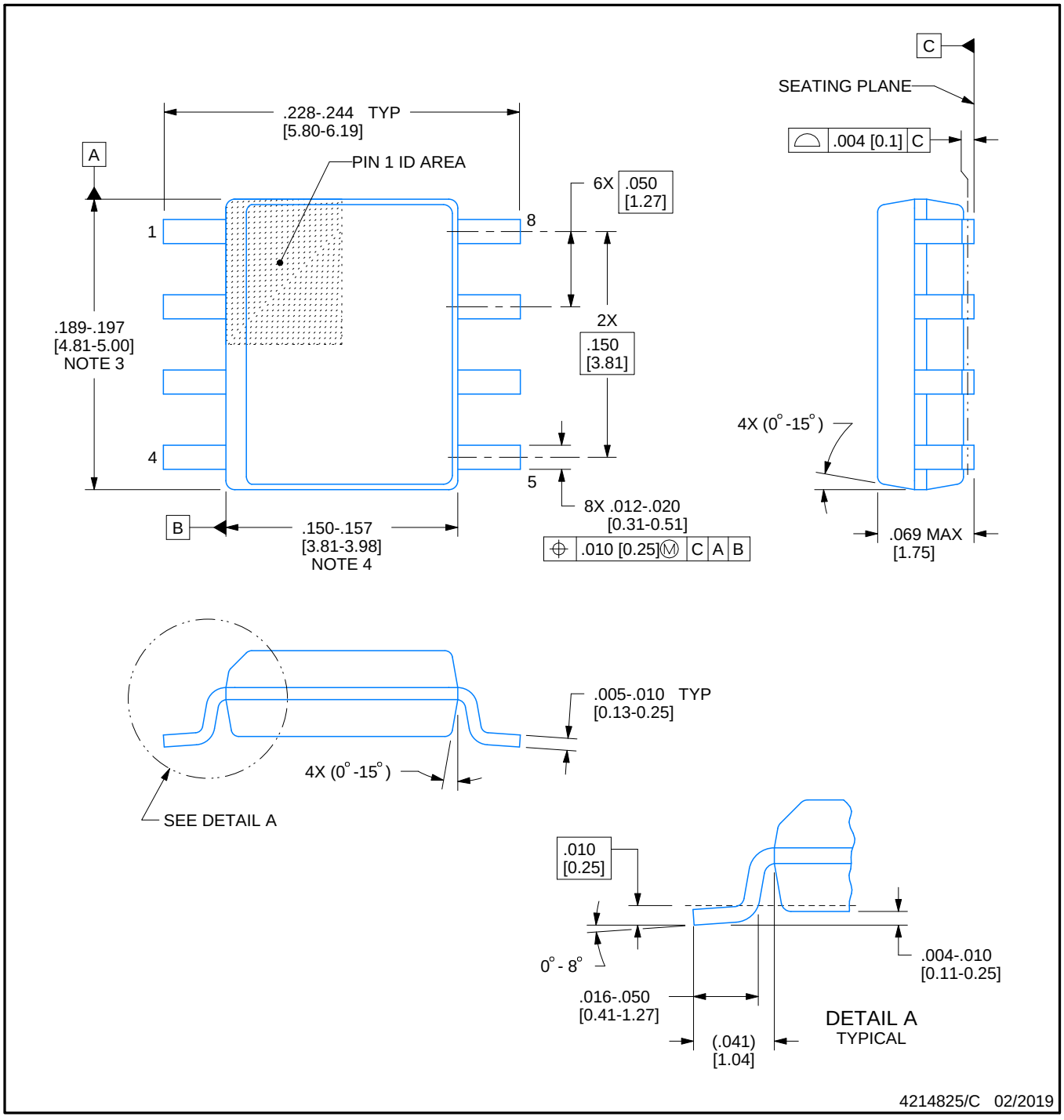


PACKAGE OUTLINE

D0008A

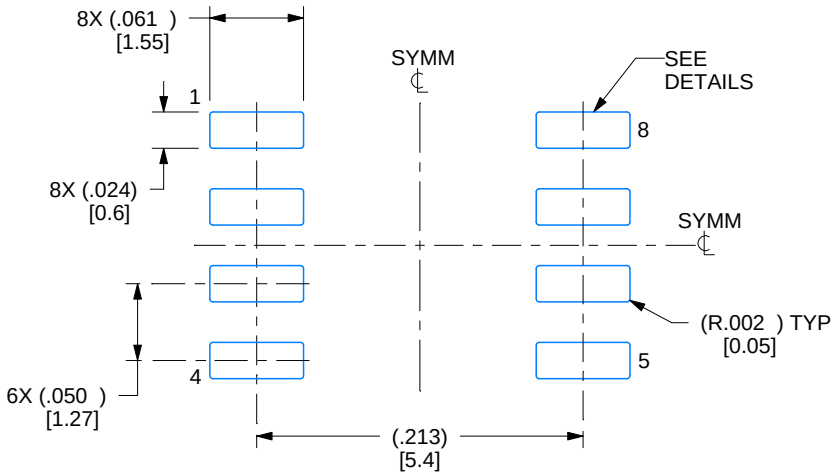
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

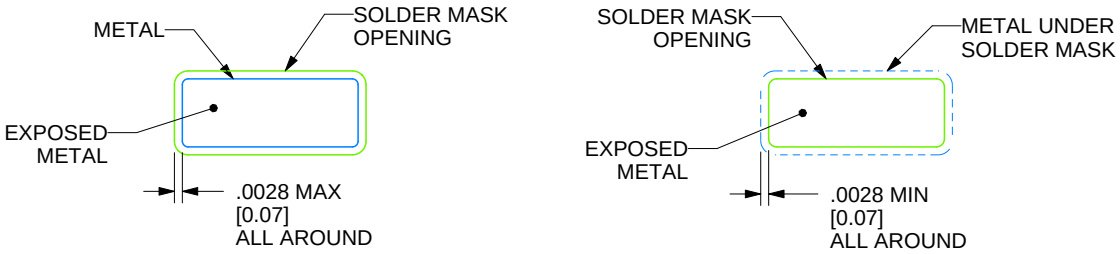


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

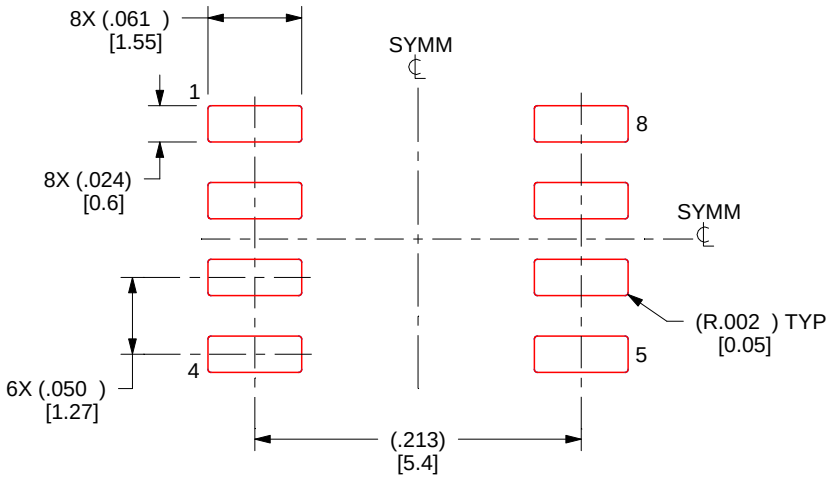
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

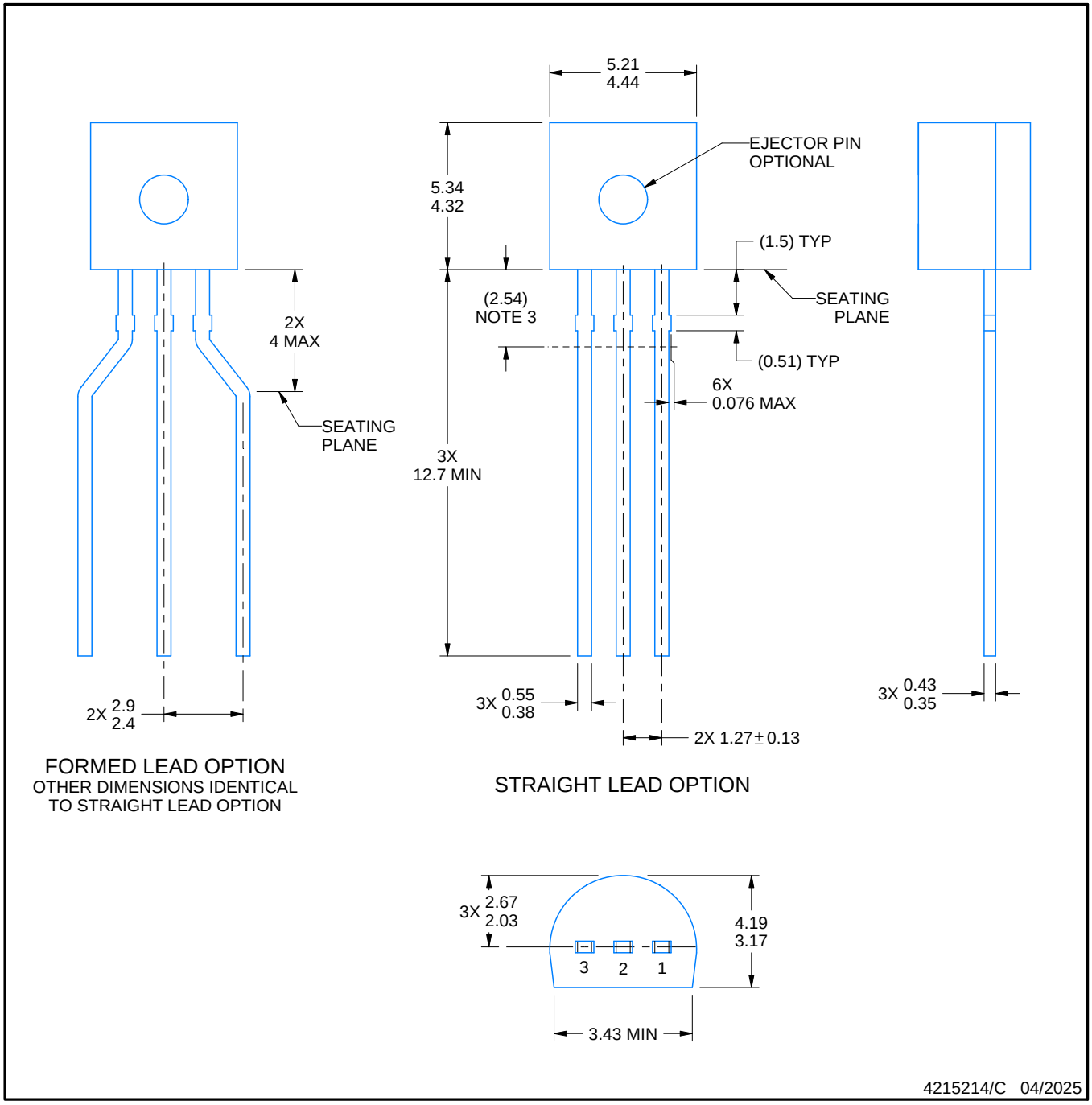
LP0003A



PACKAGE OUTLINE

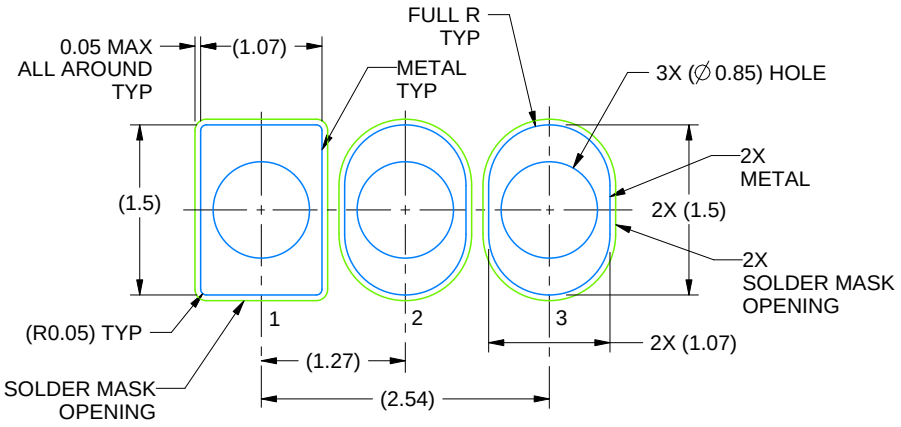
TO-92 - 5.34 mm max height

TO-92

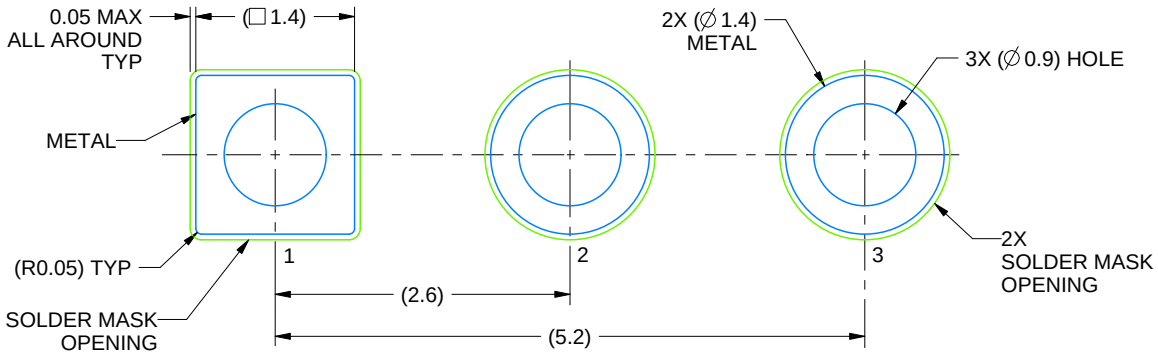


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



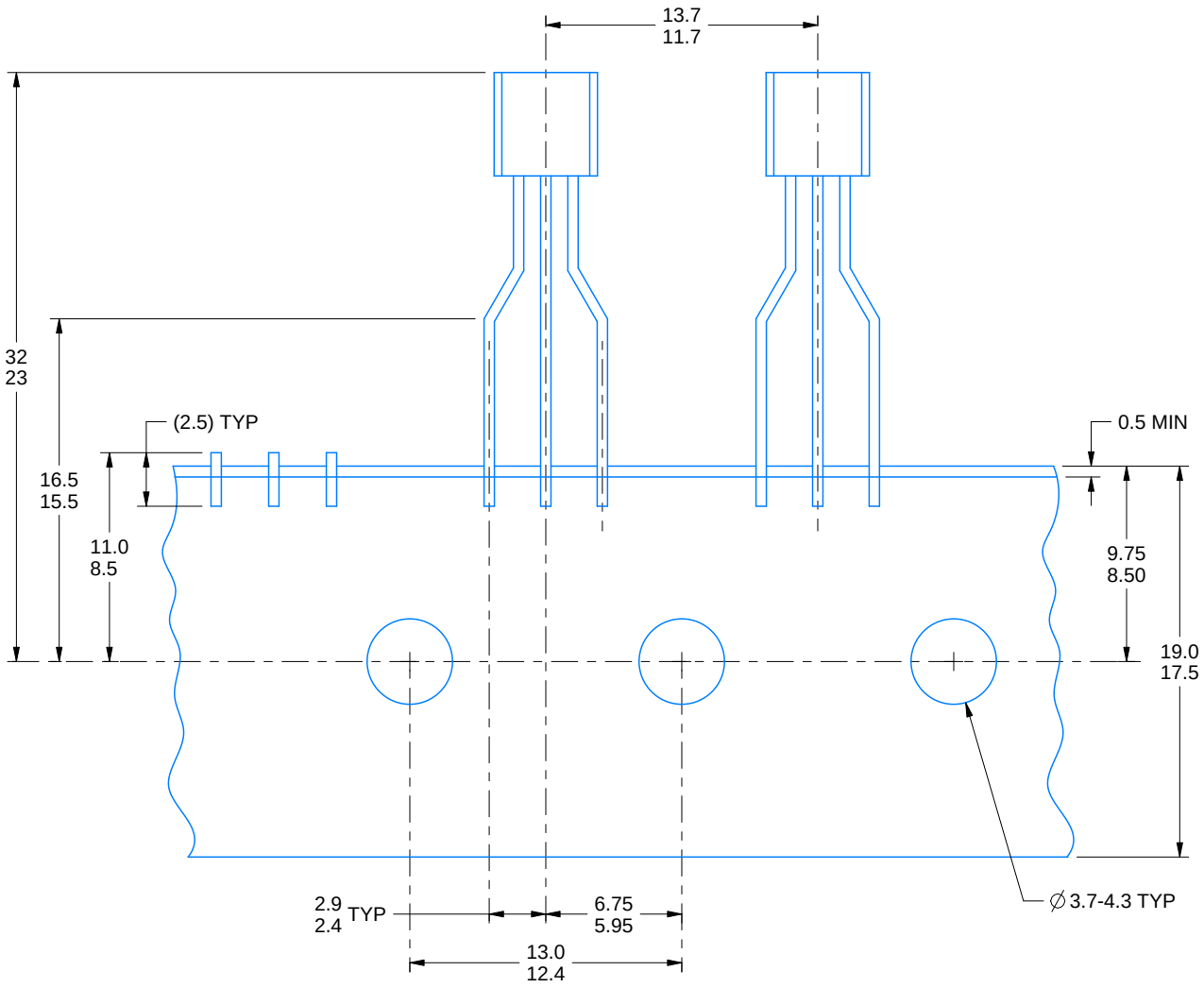
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025

LP0003A

TO-92 - 5.34 mm max height

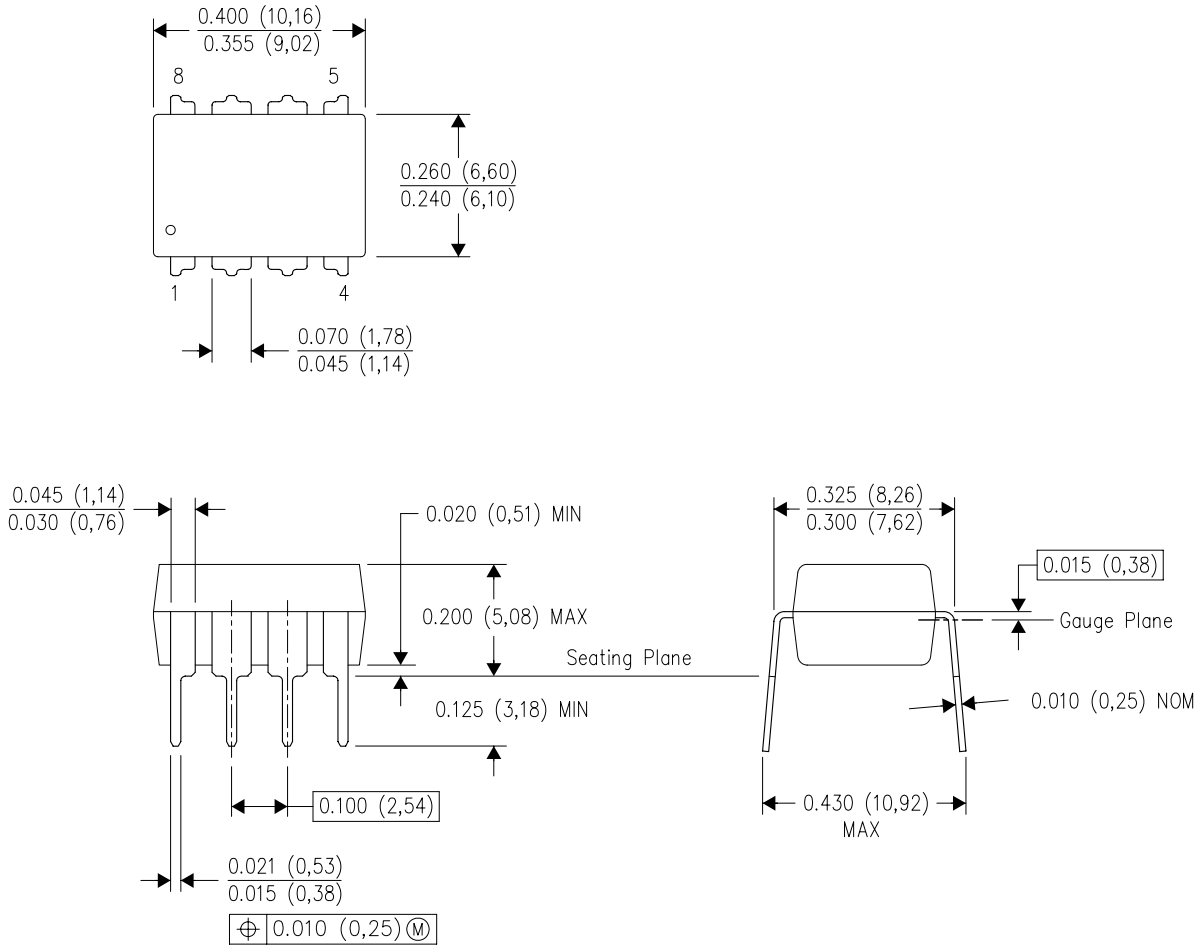
TO-92



FOR FORMED LEAD OPTION PACKAGE

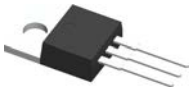
4215214/C 04/2025

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

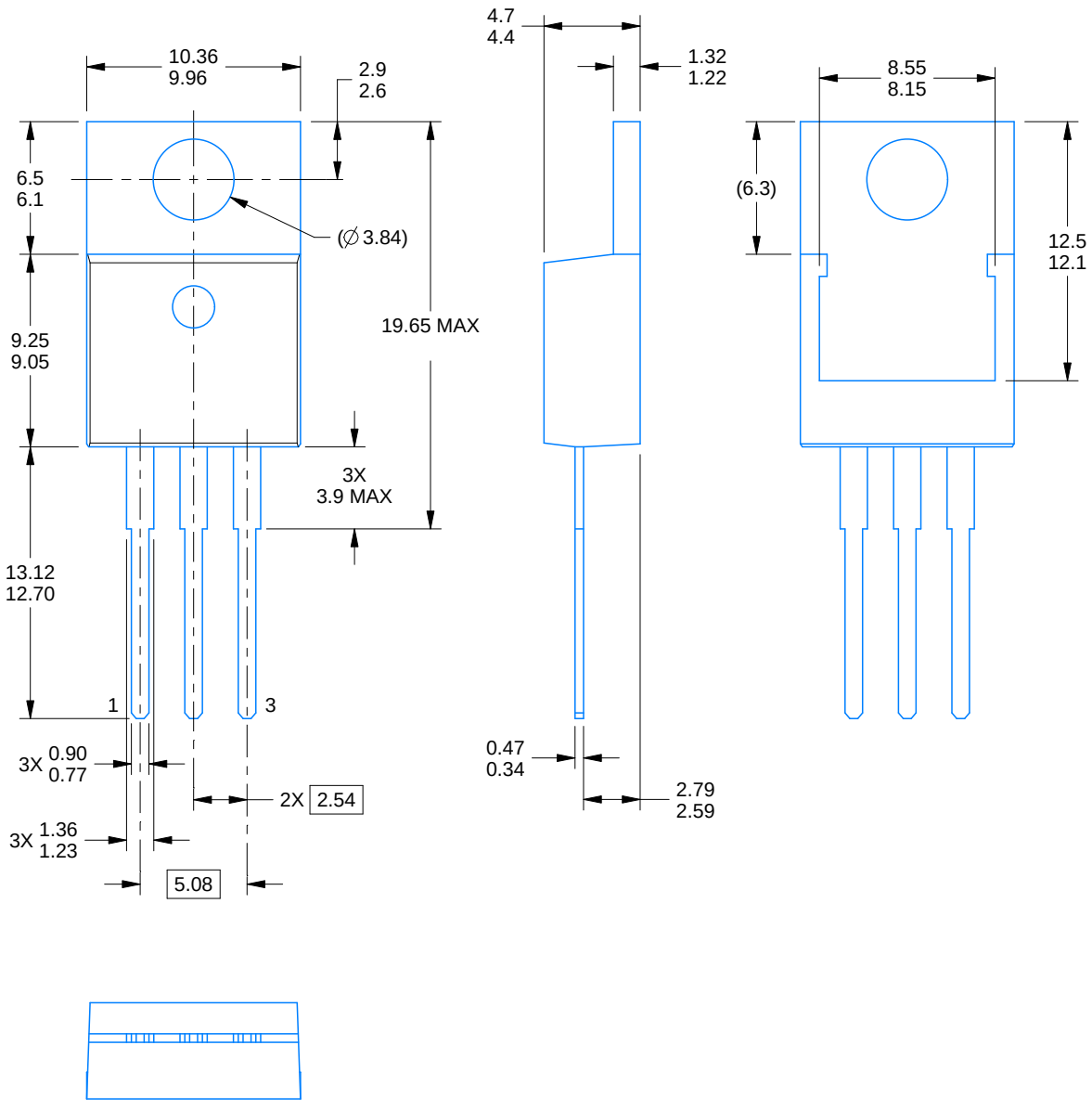
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

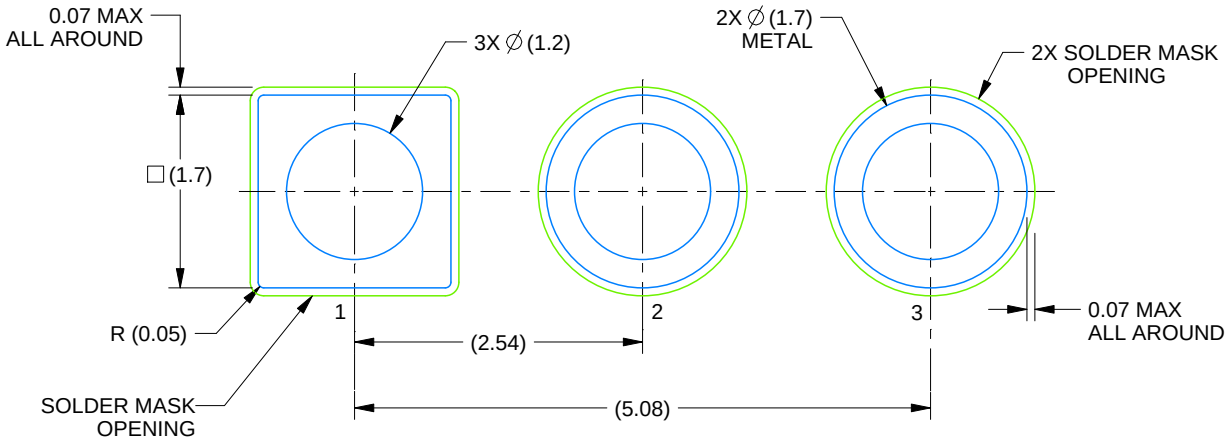
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



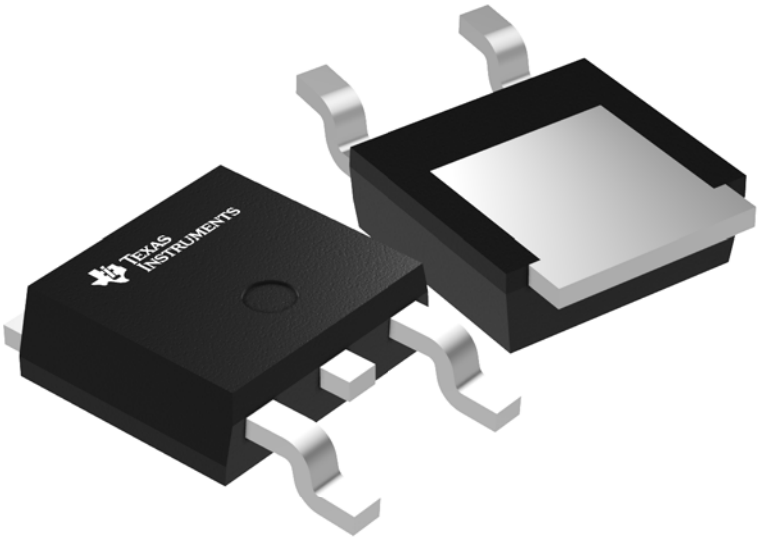
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

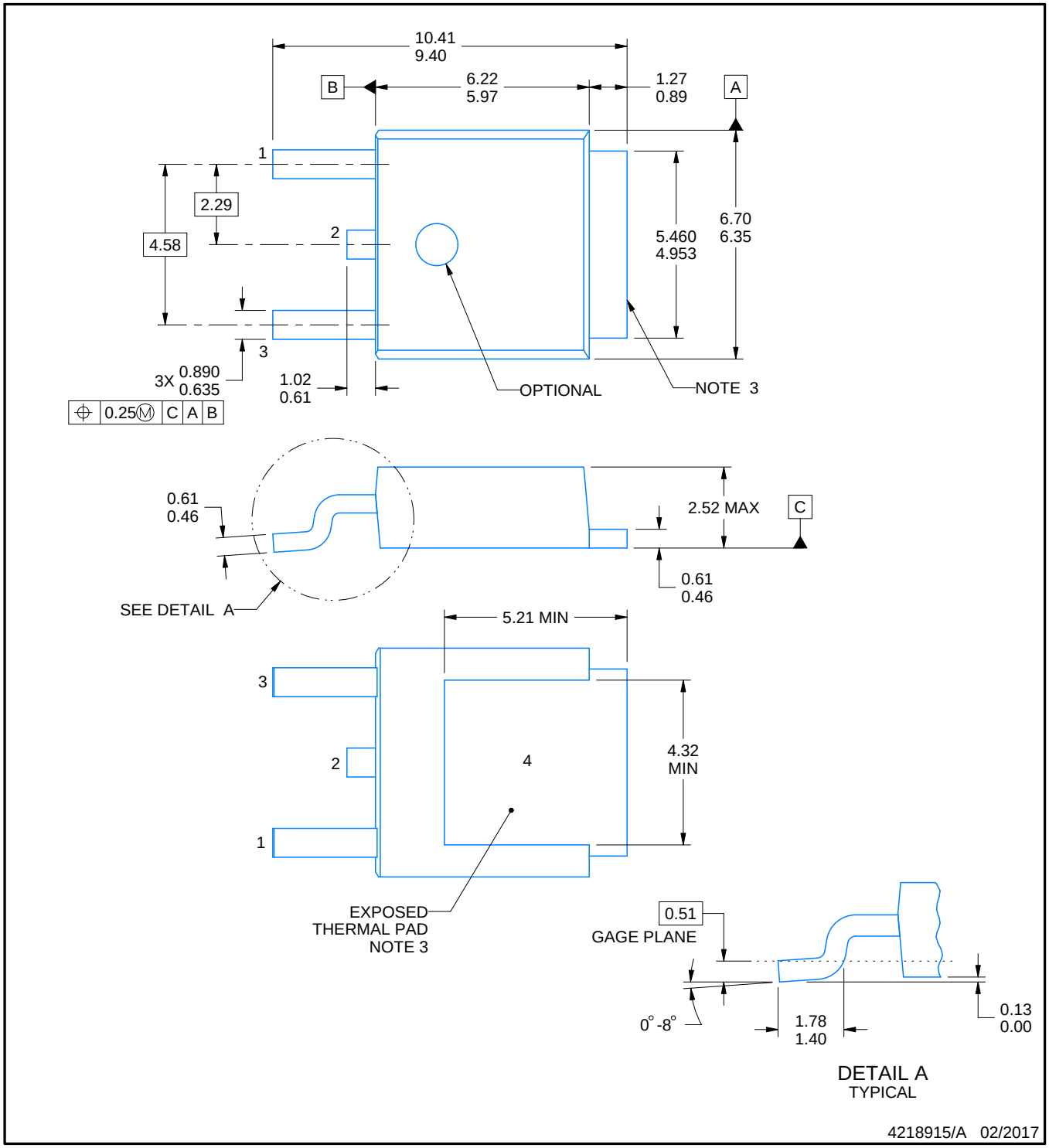


PACKAGE OUTLINE

KVU0003A

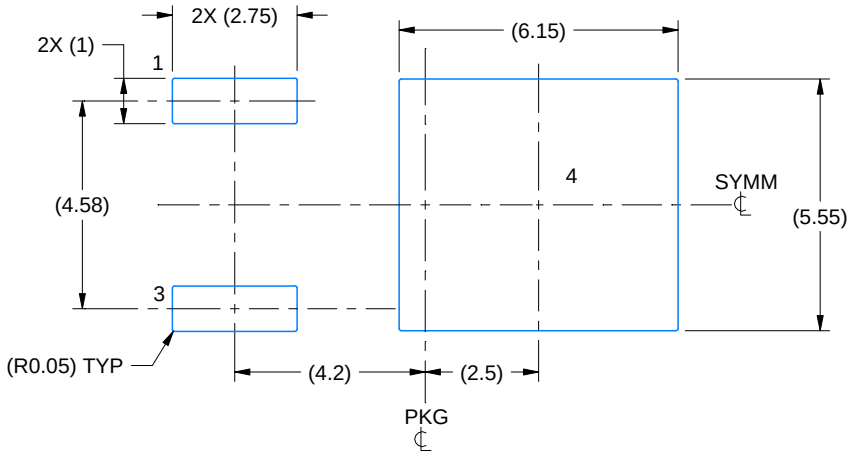
TO-252 - 2.52 mm max height

TO-252

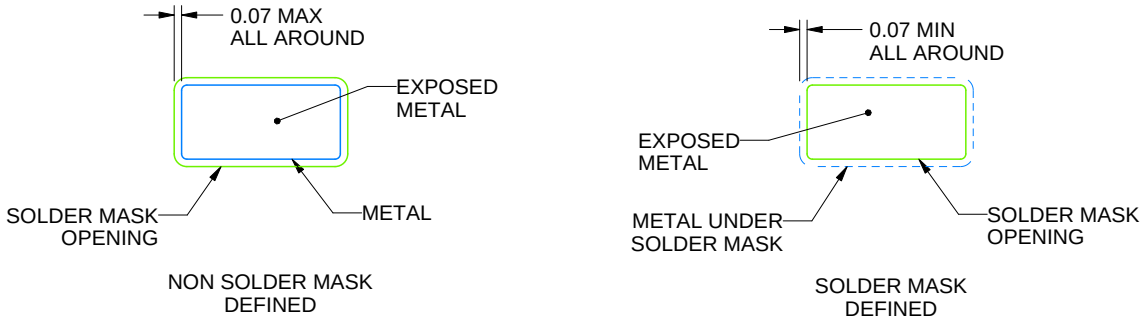


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

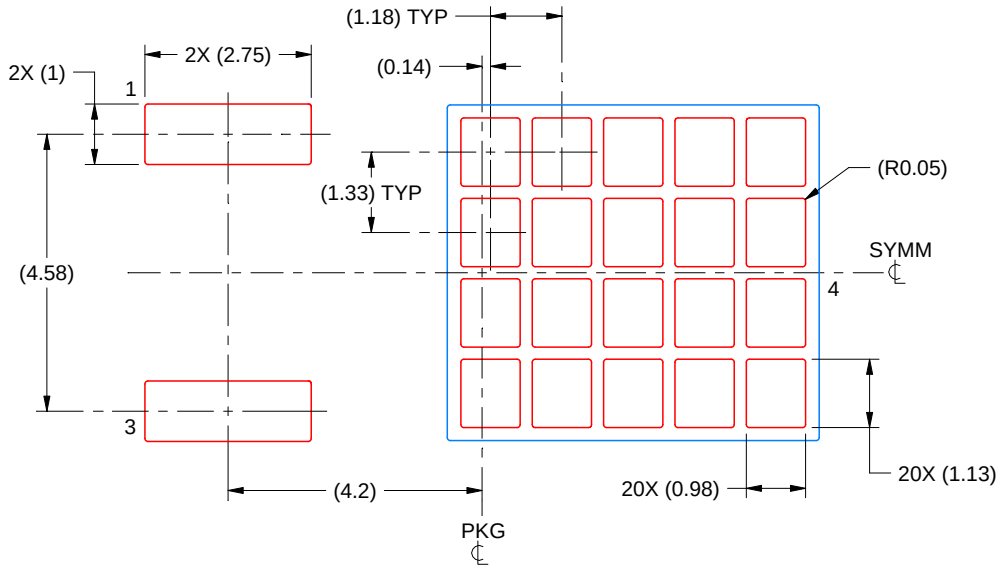
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

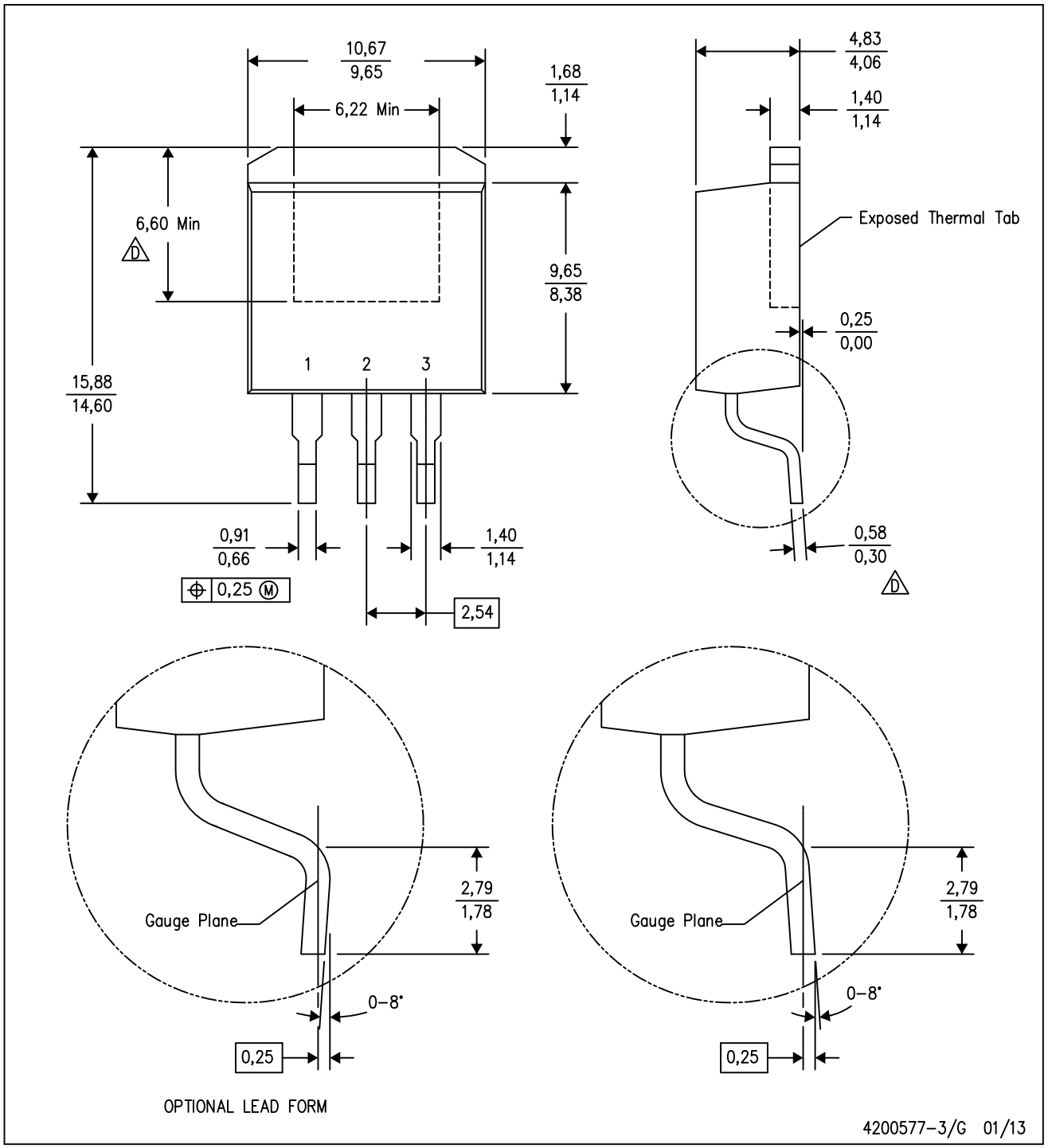
EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

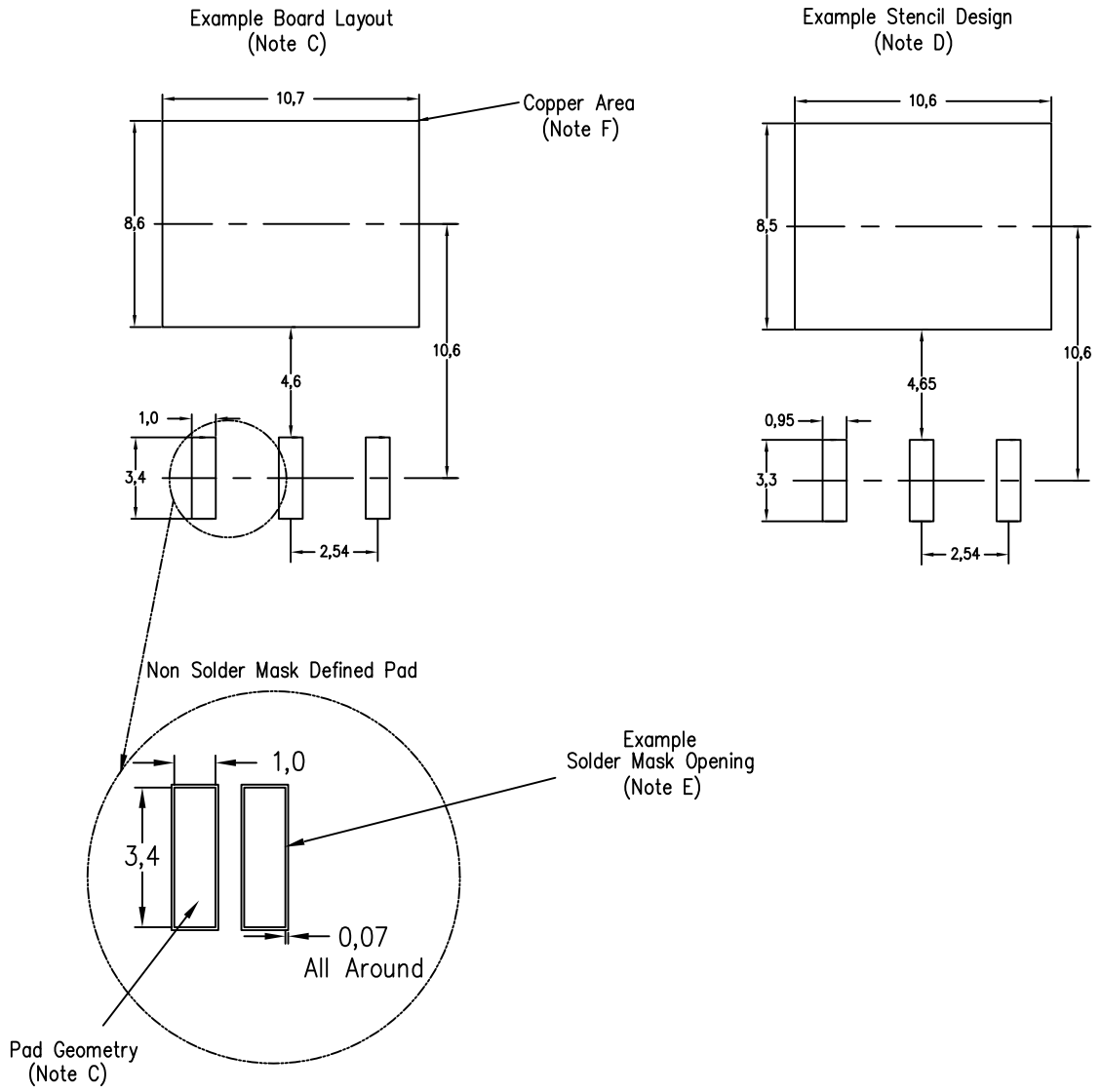
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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