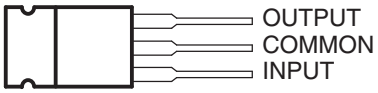
LOW-DROPOUT VOLTAGE REGULATORS

Check for Samples: TL750M SERIES

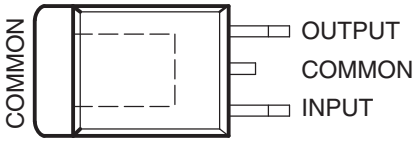
FEATURES

- **Low Dropout Voltage, Less Than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **60-V Load-Dump Protection**
- **Overvoltage Protection**
- **Internal Thermal-Overload Protection**
- **Internal Overcurrent-Limiting Circuitry**

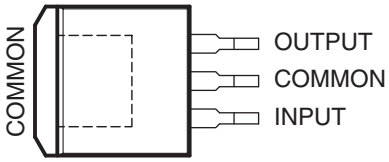
KCS PACKAGE(1)
(TOP VIEW)



KVU PACKAGE(1)
(TOP VIEW)



KTT PACKAGE(1)
(TOP VIEW)



(1) The common terminal is in electrical contact with the mounting base.

DESCRIPTION/ORDERING INFORMATION

The TL750M series devices are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M devices incorporate onboard overvoltage and current-limiting protection circuitry to protect the devices and the regulated system. The devices are fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M series ideal for standby power systems.

The TL750M offers 5-V, 8-V, 10-V, and 12-V options. The devices are characterized for operation over the virtual junction temperature range 0°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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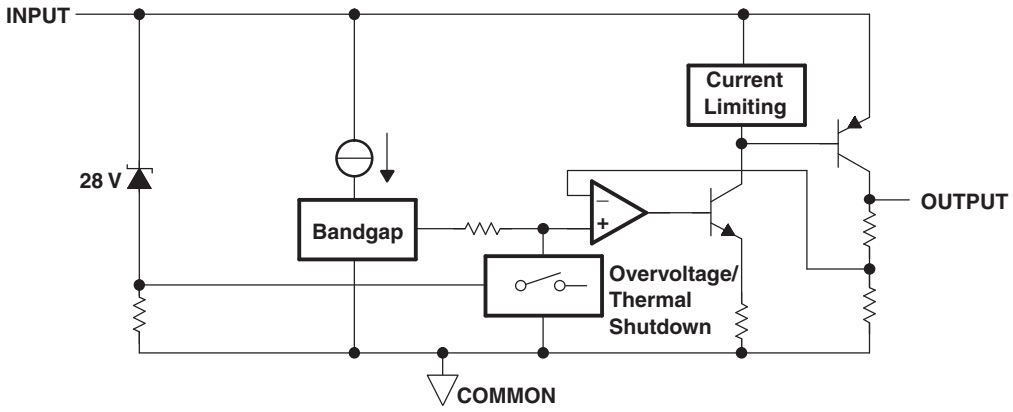
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	V_O TYP	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5 V	PowerFLEX™ – KVU	Reel of 3000	TL750M05CKVUR	750M05C
		TO-220 – KCS	Tube of 50	TL750M05CKCS	TL750M05C
		TO-263 – KTT	Reel of 500	TL750M05CKTTR	TL750M05C
	8 V	TO-220 – KCS	Tube of 50	TL750M08CKCS	TL750M08C
		PowerFLEX – KVU	Reel of 3000	TL750M08CKVUR	750M08C
	10 V	TO-220 – KCS	Tube of 50	TL750M10CKCS	TL750M10C
		PowerFLEX – KVU	Reel of 3000	TL750M10CKVUR	750M10C
	12 V	TO-220 – KCS	Tube of 50	TL750M12CKCS	TL750M12C
		PowerFLEX – KVU	Reel of 3000	TL750M12CKVUR	750M12C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(1)

over virtual junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Continuous input voltage			26	V
	Transient input voltage (see Figure 3)			60	V
	Continuous reverse input voltage			–15	V
	Transient reverse input voltage	t = 100 ms		–50	V
θ_{JA}	Package thermal impedance(2) (3)	KCS package		22	°C/W
		KTT package		25.3	
		KVU package		28	
T_J	Virtual-junction temperature range		0	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.
(3) The package thermal impedance is calculated in accordance with JESD 51.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TL750M			UNITS
		KCS (3 PINS)	KVU (3 PINS)	KTT (3 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	28.7	50.9	27.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	59.8	57.9	43.2	
θ_{JB}	Junction-to-board thermal resistance	0.5	34.8	17.3	
ψ_{JT}	Junction-to-top characterization parameter	5.3	6	2.8	
ψ_{JB}	Junction-to-board characterization parameter	0.4	23.7	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.1	0.4	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Input voltage	TL750M05	6	26	V
		TL750M08	9	26	
		TL750M10	11	26	
		TL750M12	13	26	
I_O	Output current			750	mA
T_J	Operating virtual-junction temperature		0	125	°C

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TL750M05 ELECTRICAL CHARACTERISTICS(1)

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M05			UNIT
		MIN	TYP	MAX	
Output voltage		4.95	5	5.05	V
	T_J = 0°C to 125°C	4.9		5.1	
Input voltage regulation	V_I = 9 V to 16 V, I_O = 250 mA		10	25	mV
	V_I = 6 V to 26 V, I_O = 250 mA		12	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		20	50	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

TL750M08 ELECTRICAL CHARACTERISTICS(1)

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M08			UNIT
		MIN	TYP	MAX	
Output voltage		7.92	8	8.08	V
	T_J = 0°C to 125°C	7.84		8.16	
Input voltage regulation	V_I = 10 V to 17 V, I_O = 250 mA		12	40	mV
	V_I = 9 V to 26 V, I_O = 250 mA		15	68	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		24	80	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

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TL750M10 ELECTRICAL CHARACTERISTICS(1)

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M10			UNIT
		MIN	TYP	MAX	
Output voltage		9.9	10	10.1	V
	T_J = 0°C to 125°C	9.8		10.2	
Input voltage regulation	V_I = 12 V to 18 V, I_O = 250 mA		15	43	mV
	V_I = 11 V to 26 V, I_O = 250 mA		20	75	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		30	100	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		1000		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

TL750M12 ELECTRICAL CHARACTERISTICS(1)

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M12			UNIT
		MIN	TYP	MAX	
Output voltage		11.88	12	12.12	V
	T_J = 0°C to 125°C	11.76		12.24	
Input voltage regulation	V_I = 14 V to 19 V, I_O = 250 mA		15	43	mV
	V_I = 13 V to 26 V, I_O = 250 mA		20	78	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		30	120	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		1000		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

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PARAMETER MEASUREMENT INFORMATION

The TL750Mxx is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figure 1 and Figure 2 can establish the capacitance value and ESR range for the best regulator performance.

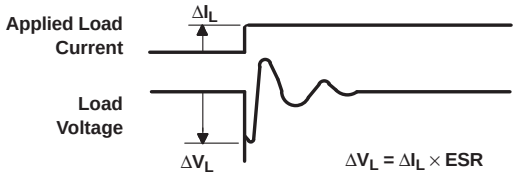
Figure 1 shows the recommended range of ESR for a given load with a 10-μF capacitor on the output. This figure also shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen because it is the worst case. Figure 2 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 μF and a maximum ESR limit of 2 Ω. This figure establishes the amount that the minimum ESR limit shown in Figure 1 can be adjusted for different capacitor values.

For example, where the minimum load needed is 200 mA, Figure 1 suggests an ESR range of 0.8 Ω to 2 Ω for 10 μF. Figure 2 shows that changing the capacitor from 10 μF to 400 μF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This allows an ESR range of 0.13 Ω to 2 Ω , achieving an expanded ESR range by using a larger capacitor at the output. For better stability in low-current applications, a small resistance placed in series with the capacitor (see Table 1) is recommended, so that ESRs better approximate those shown in Figure 1 and Figure 2.

Table 1. Compensation for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 μF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 μF	0.6 Ω	T491D336M010AS	0.5 Ω



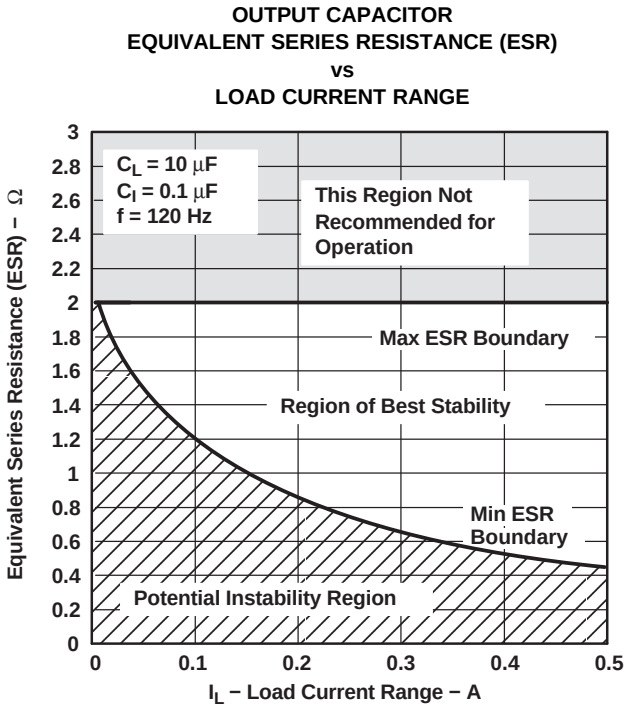


Figure 1.

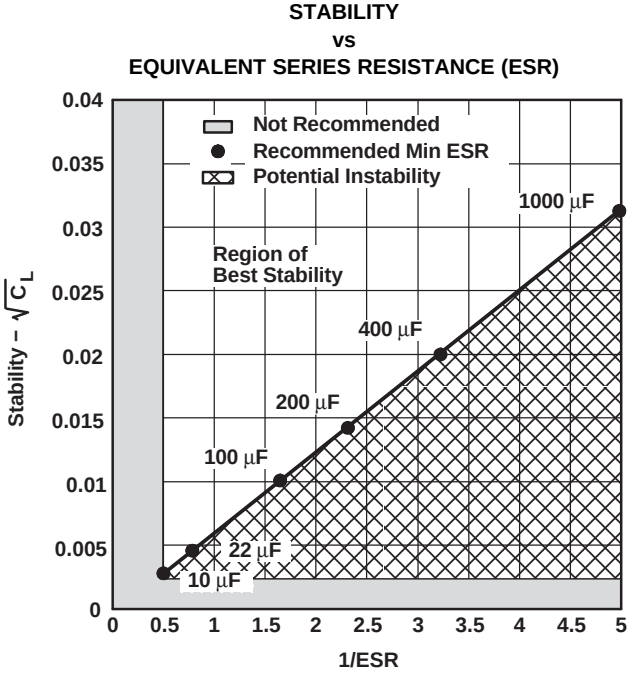


Figure 2.

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TYPICAL CHARACTERISTICS

Table 2. Table of Graphs

		FIGURE
Transient input voltage vs Time		3
Output voltage vs Input voltage		4
Input current vs Input voltage	I_O = 10 mA	5
	I_O = 100 mA	6
Dropout voltage vs Output current		7
Quiescent voltage vs Output current		8
Load transient response		9
Line transient response		10

TRANSIENT INPUT VOLTAGE vs TIME

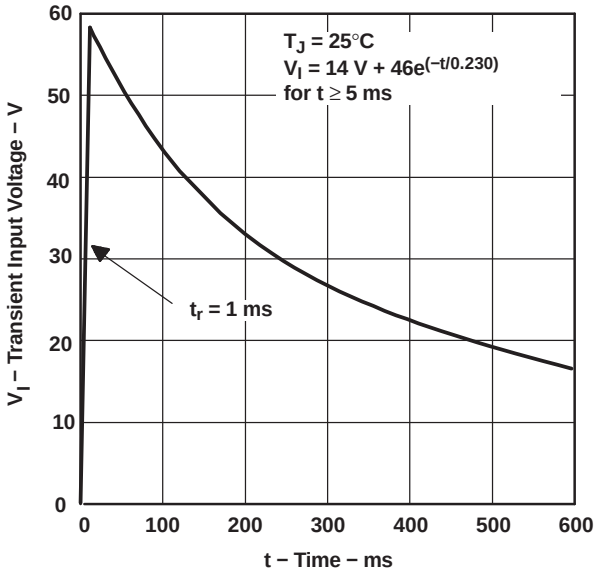


Figure 3.

OUTPUT VOLTAGE vs INPUT VOLTAGE

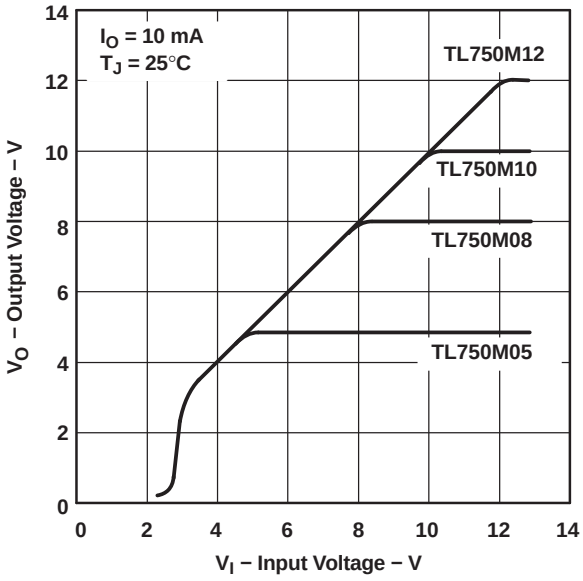


Figure 4.

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INPUT CURRENT vs INPUT VOLTAGE

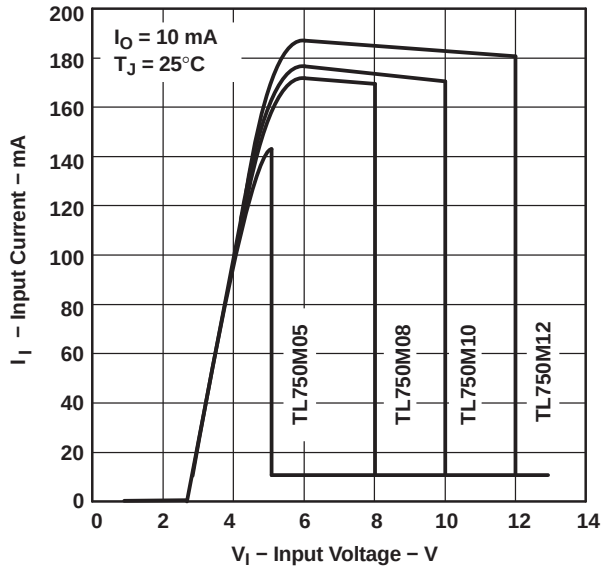


Figure 5.

INPUT CURRENT vs INPUT VOLTAGE

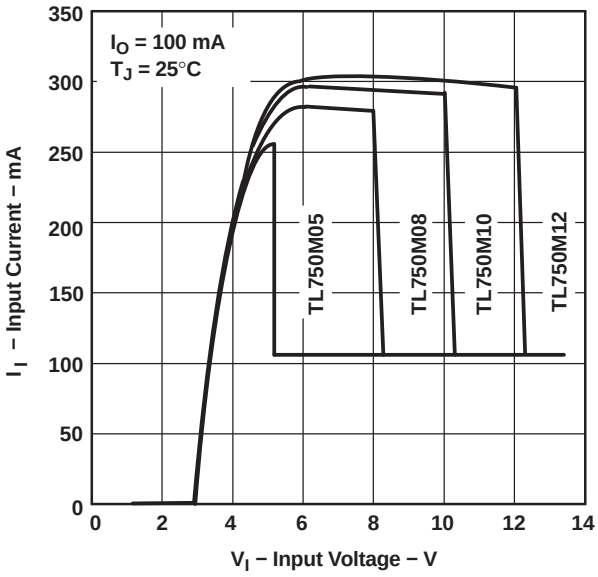


Figure 6.

DROPOUT VOLTAGE vs OUTPUT CURRENT

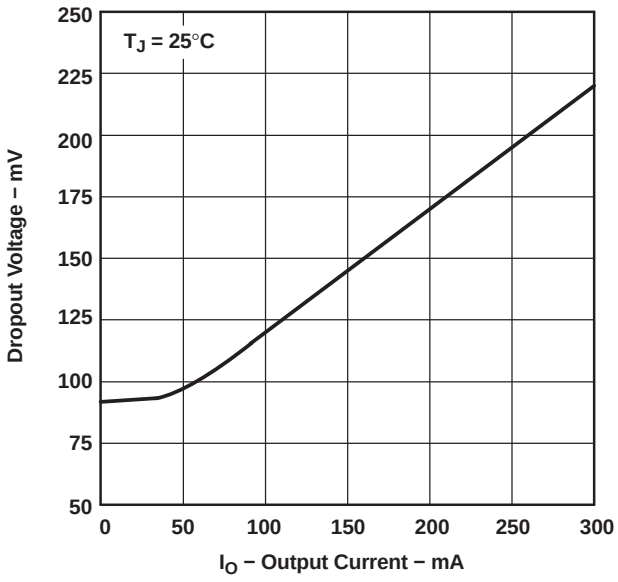


Figure 7.

QUIESCENT CURRENT vs OUTPUT CURRENT

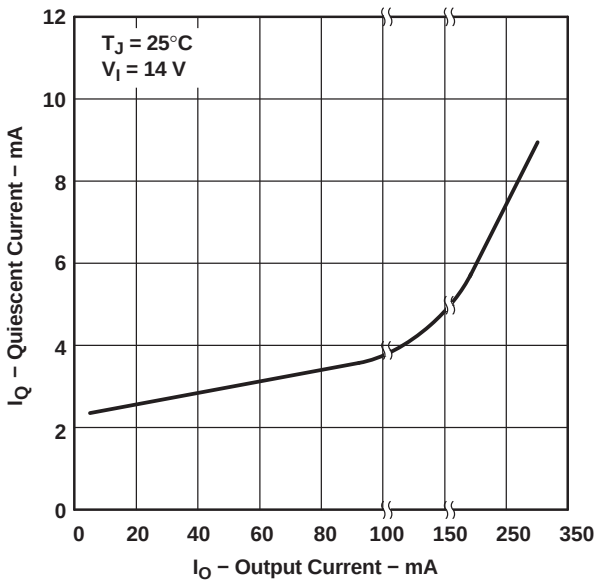


Figure 8.

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LOAD TRANSIENT RESPONSE

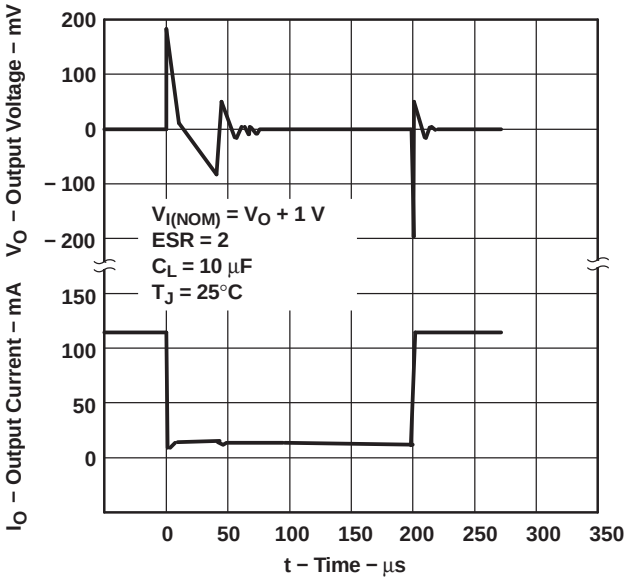


Figure 9.

LINE TRANSIENT RESPONSE

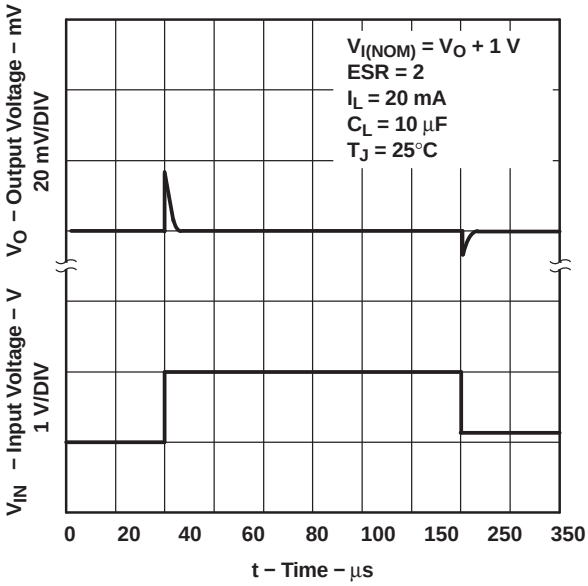


Figure 10.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL750M05CKCSE3	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M05C
TL750M05CKCSE3.A	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M05C
TL750M05CKTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TL750M05C
TL750M05CKTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	TL750M05C
TL750M05CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M05C
TL750M05CKVURG3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M05C
TL750M08CKCSE3	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M08C
TL750M08CKCSE3.A	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M08C
TL750M08CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M08C
TL750M08CKVURG3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M08C
TL750M10CKCSE3	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M10C
TL750M10CKCSE3.A	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M10C
TL750M10CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M10C
TL750M10CKVURG3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M10C
TL750M12CKCSE3	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M12C
TL750M12CKCSE3.A	Active	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	TL750M12C
TL750M12CKVURG3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M12C
TL750M12CKVURG3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	0 to 125	50M12C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TL750M :

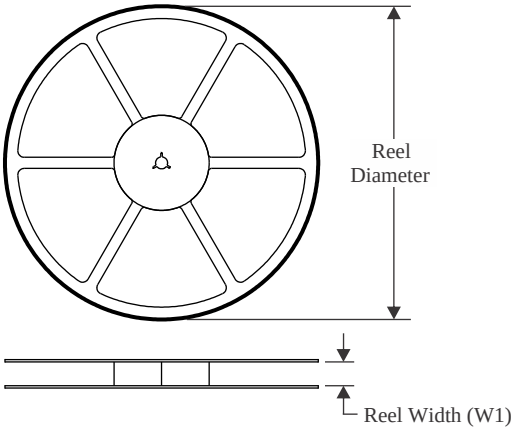
- Automotive : TL750M-Q1

NOTE: Qualified Version Definitions:

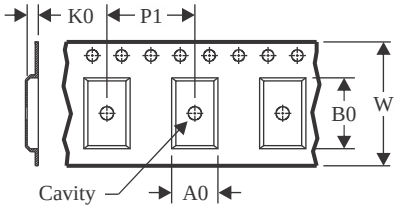
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

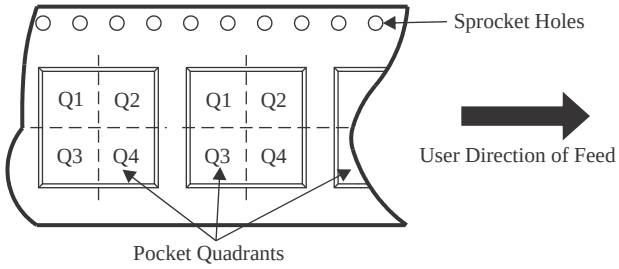


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

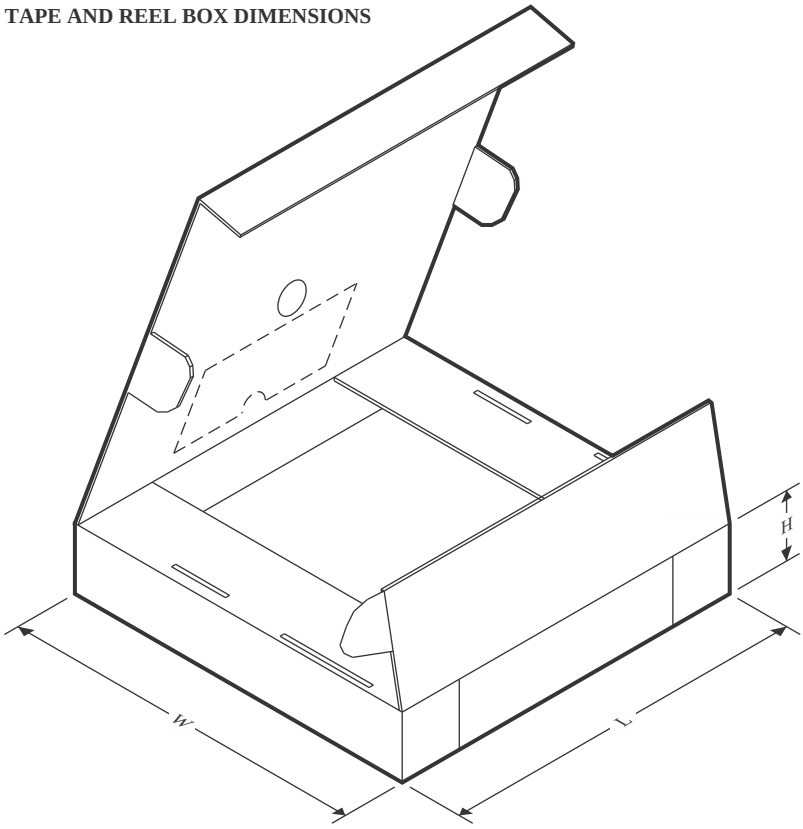
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750M05CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL750M05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M08CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M10CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M12CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

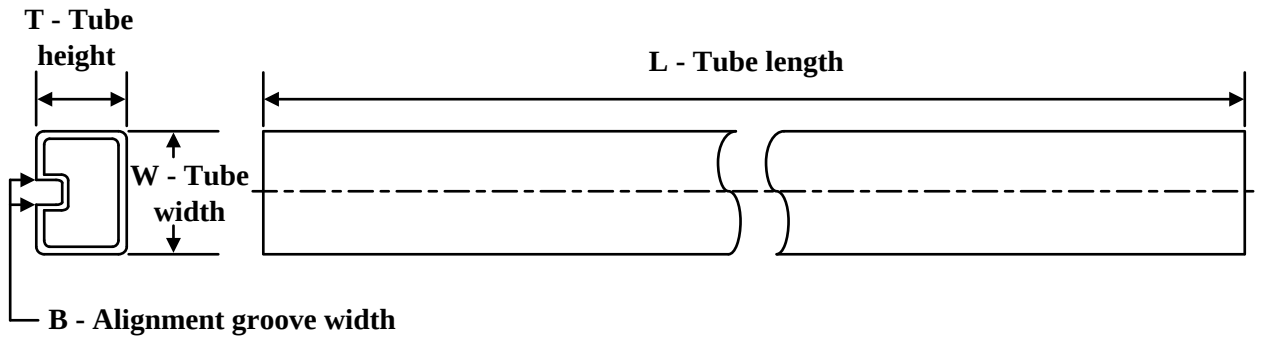
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750M05CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750M05CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M08CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M10CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M12CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

TUBE



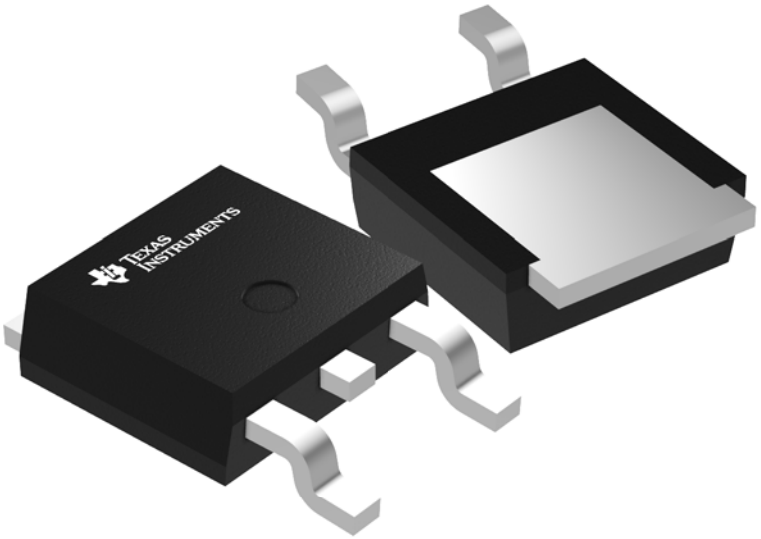
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL750M05CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M05CKCSE3.A	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M08CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M08CKCSE3.A	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M10CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M10CKCSE3.A	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M12CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TL750M12CKCSE3.A	KCS	TO-220	3	50	532	34.1	700	9.6

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

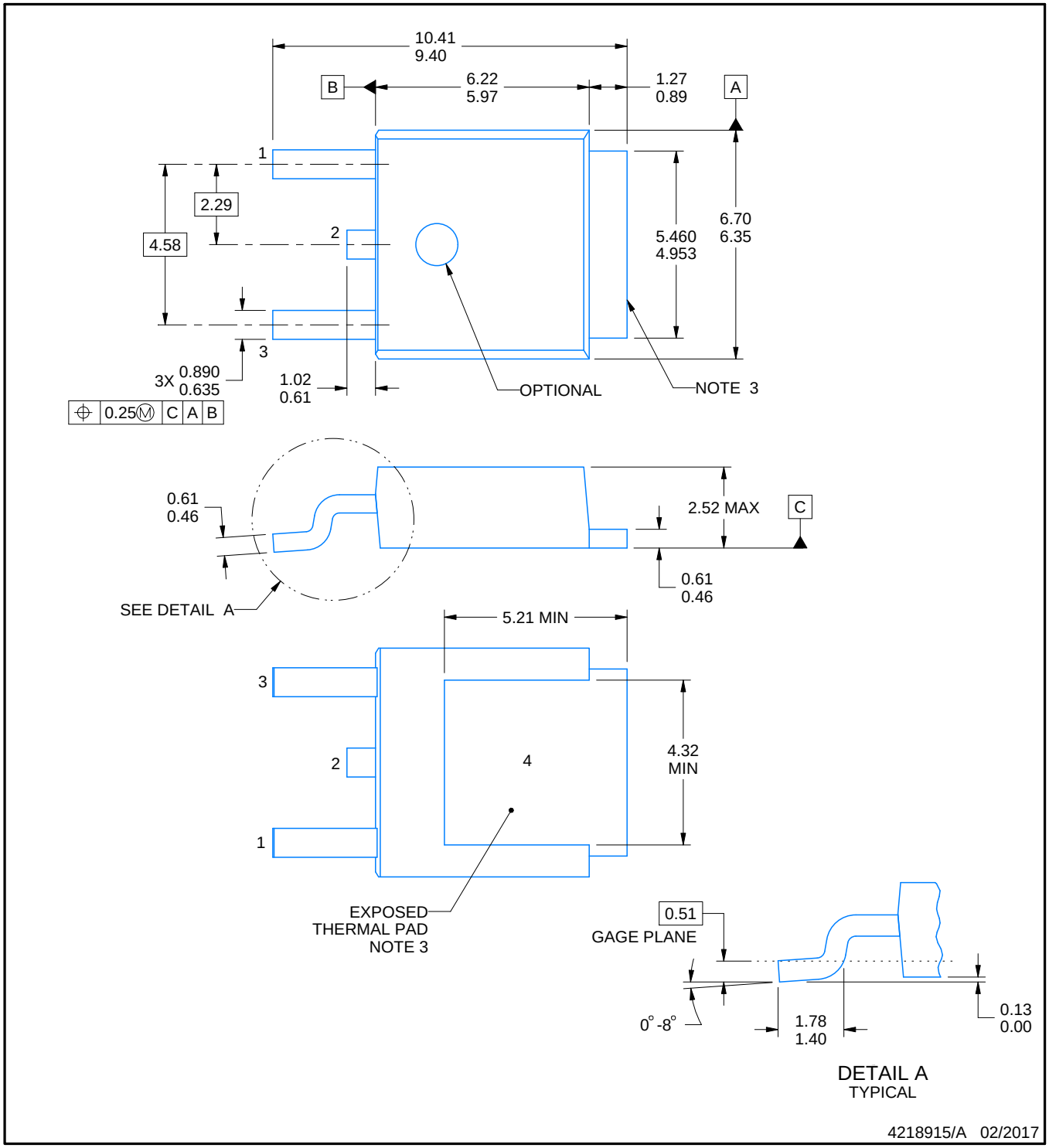


PACKAGE OUTLINE

KVU0003A

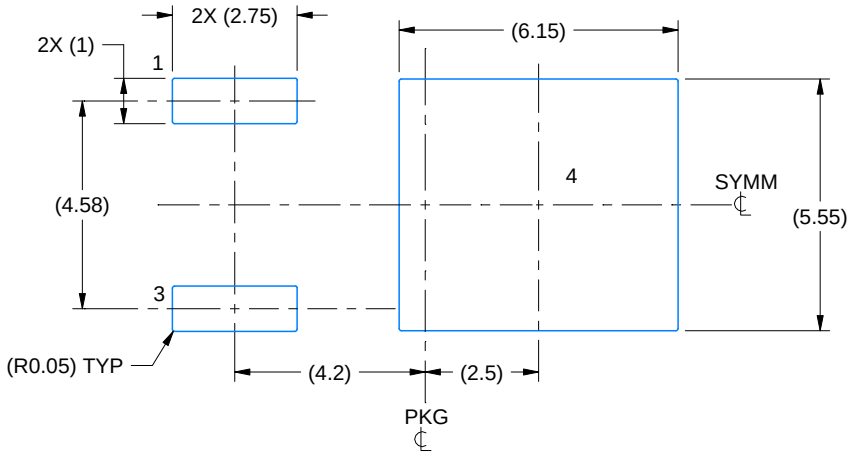
TO-252 - 2.52 mm max height

TO-252

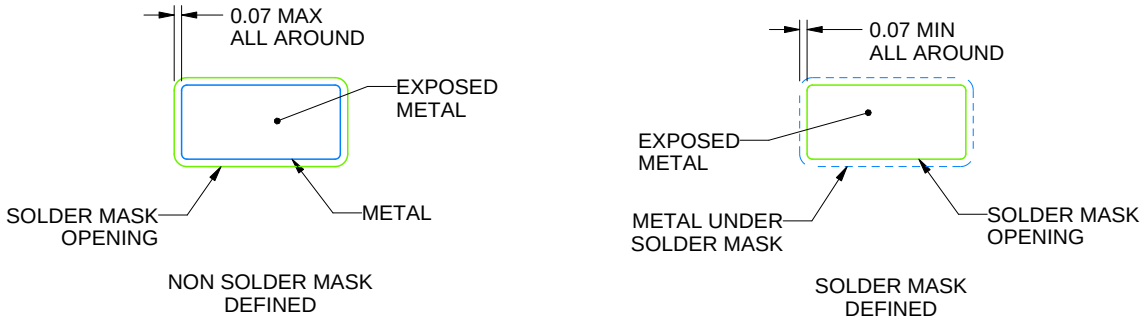


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

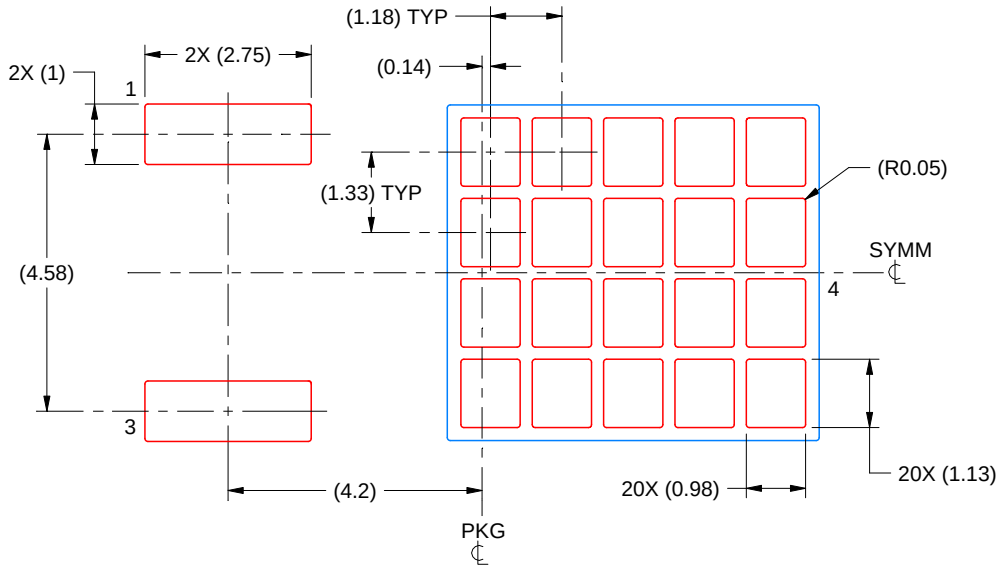
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

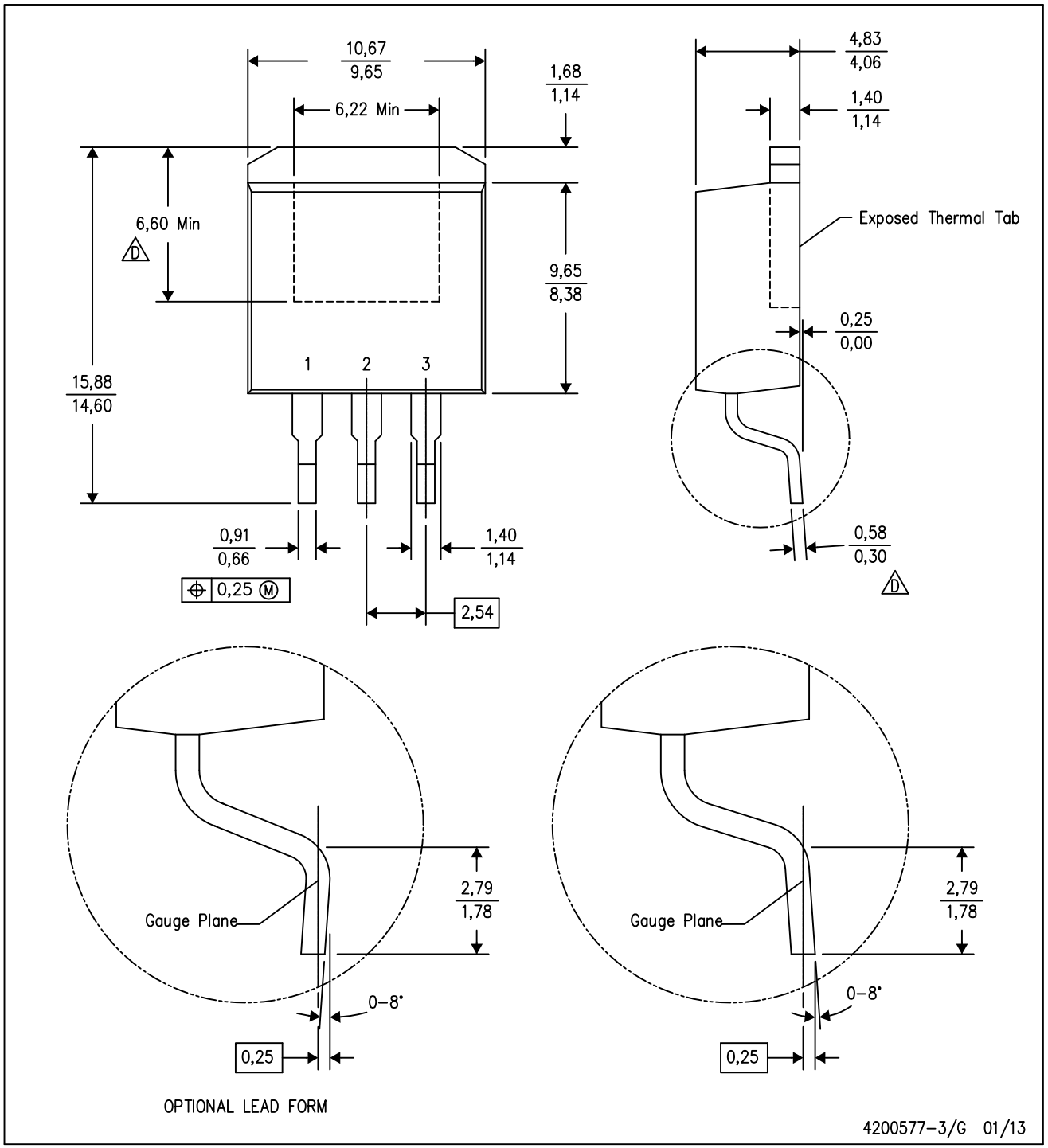
EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

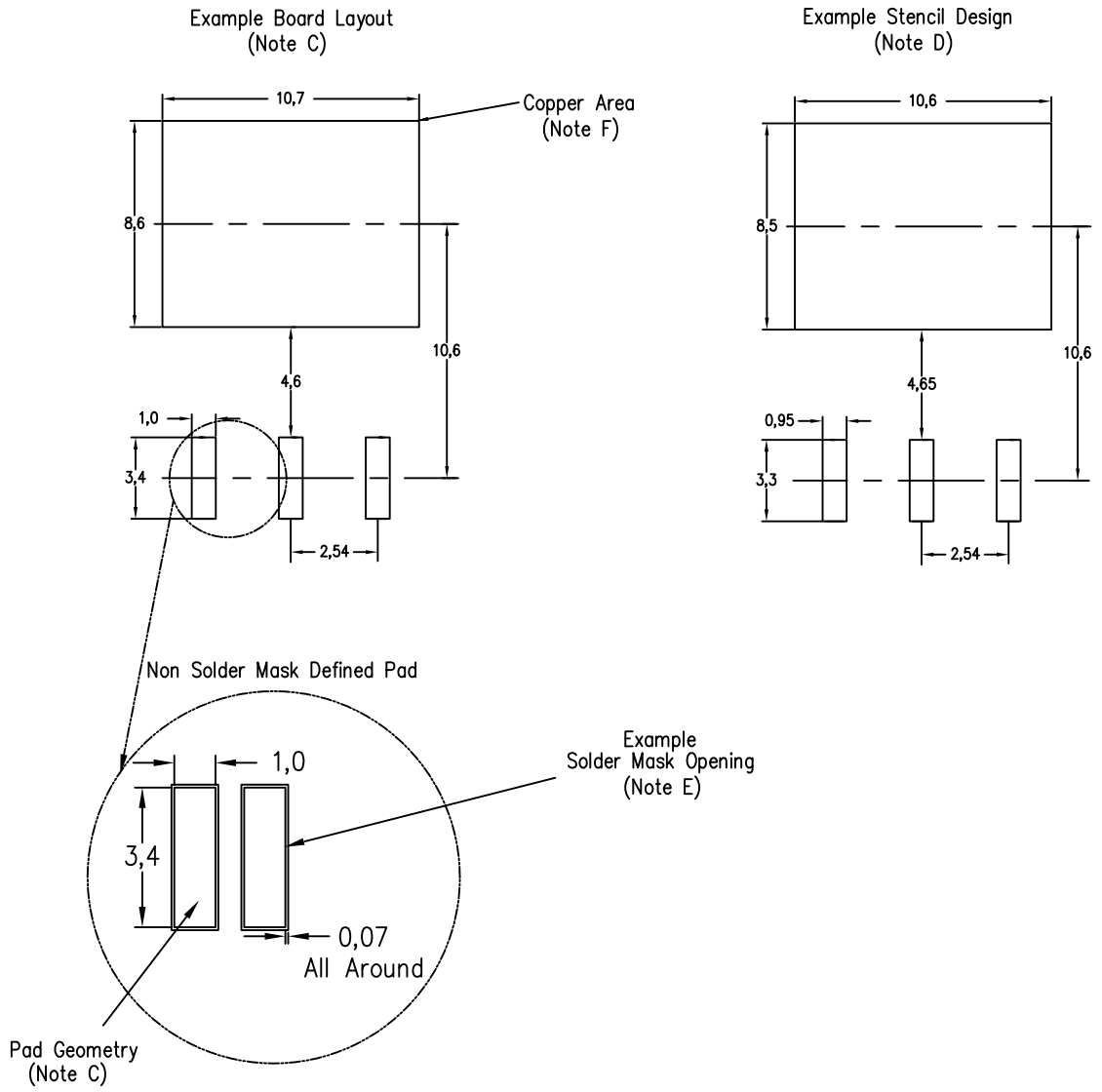
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



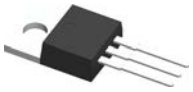
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

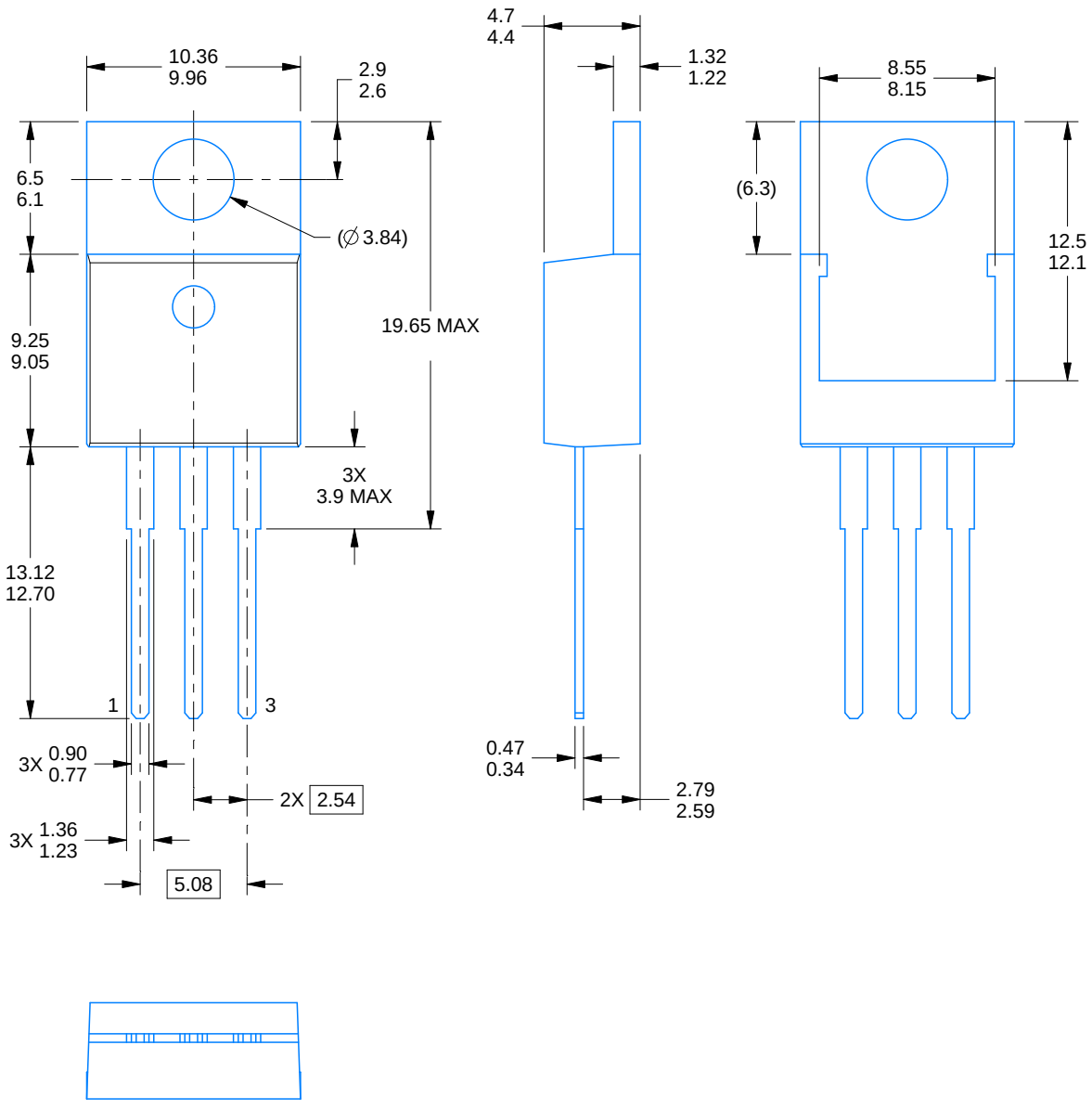
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

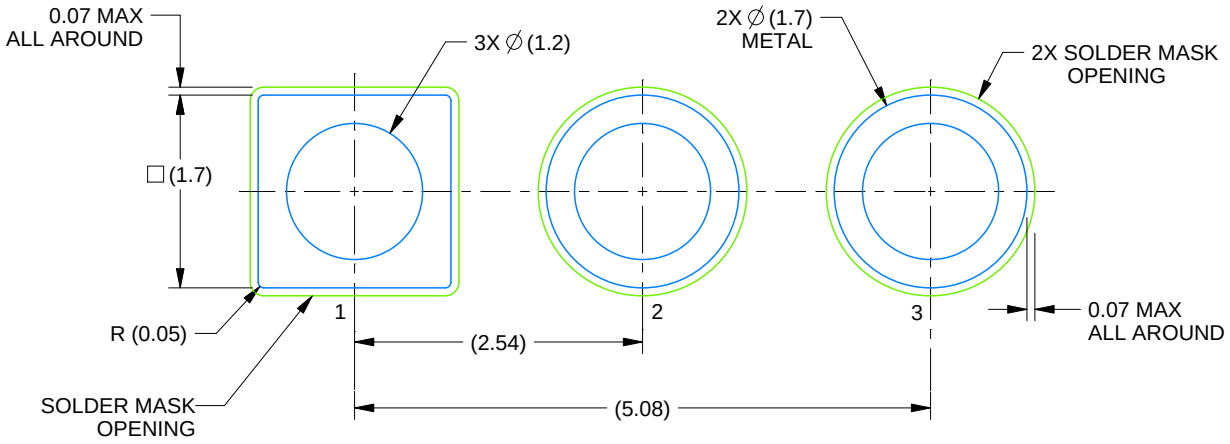
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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