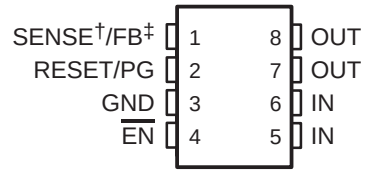
- **Available in 5-V, 4.85-V, 3.3-V, 3.0-V, and 2.5-V Fixed-Output and Adjustable Versions**
- **Dropout Voltage <85 mV Max at I_O = 100 mA (TPS7250)**
- **Low Quiescent Current, Independent of Load, 180 μA Typ**
- **8-Pin SOIC and 8-Pin TSSOP Package**
- **Output Regulated to ±2% Over Full Operating Range for Fixed-Output Versions**
- **Extremely Low Sleep-State Current, 0.5 μA Max**
- **Power-Good (PG) Status Output**

D, P, OR PW PACKAGE
(TOP VIEW)



† SENSE – Fixed voltage options only (TPS7225, TPS7230, TPS7233, TPS7248, and TPS7250)

‡ FB – Adjustable version only (TPS7201)

description

The TPS72xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, micropower operation, and miniaturized packaging. These regulators feature extremely low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in small-outline integrated-circuit (SOIC) packages and 8-terminal thin shrink small-outline (TSSOP), the TPS72xx series devices are ideal for cost-sensitive designs and for designs where board space is at a premium.

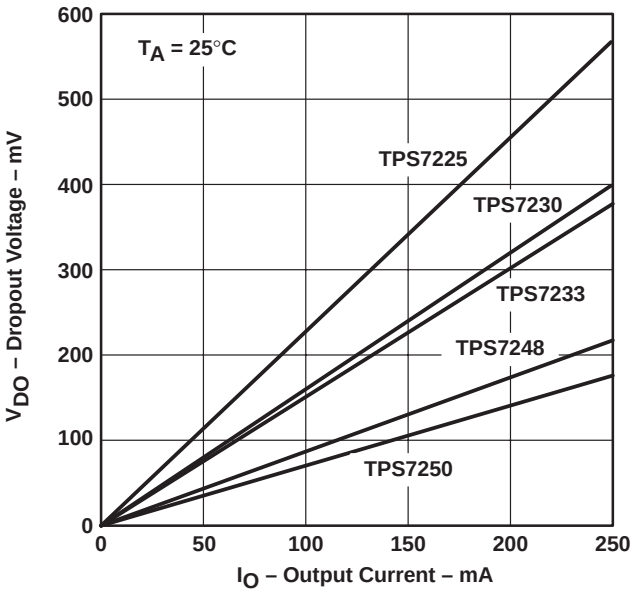


Figure 1. Typical Dropout Voltage Versus Output Current

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS device. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low – maximum of 85 mV at 100 mA of load current (TPS7250) – and is directly proportional to the load current (see Figure 1). Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (300 μA maximum) and is stable over the entire range of output load current (0 mA to 250 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage and micropower operation result in a significant increase in system battery operating life.

The TPS72xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 0.5 μA maximum at T_J = 25°C. Other features include a power-good function that reports low output voltage and may be used to implement a power-on reset or a low-battery indicator.

The TPS72xx is offered in 2.5-V, 3-V, 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

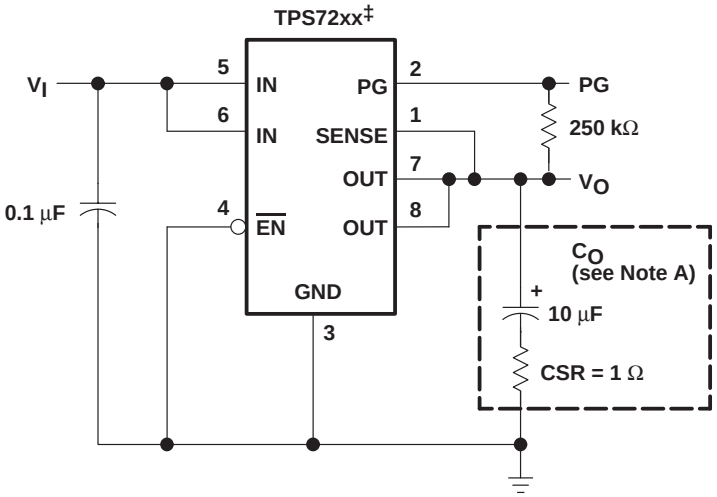
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PDIP (P)	TSSOP (PW)	
–55°C to 150°C	4.9	5	5.1	TPS7250QD	TPS7250QP	TPS7250QPWR	TPS7250Y
	4.75	4.85	4.95	TPS7248QD	TPS7248QP	TPS7248QPWR	TPS7248Y
	3.23	3.3	3.37	TPS7233QD	TPS7233QP	TPS7233QPWR	TPS7233Y
	2.94	3	3.06	TPS7230QD	TPS7230QP	TPS7230QPWR	TPS7230Y
	2.45	2.5	2.55	TPS7225QD	TPS7225QP	TPS7225QPWR	TPS7225Y
	Adjustable 1.2 V to 9.75 V			TPS7201QD	TPS7201QP	TPS7201QPWR	TPS7201Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7250QDR). The PW package is only available left-end taped and reeled. The TPS7201Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.



‡ TPS7225Q, TPS7230Q, TPS7233Q, TPS7248Q, TPS7250Q (fixed-voltage options)

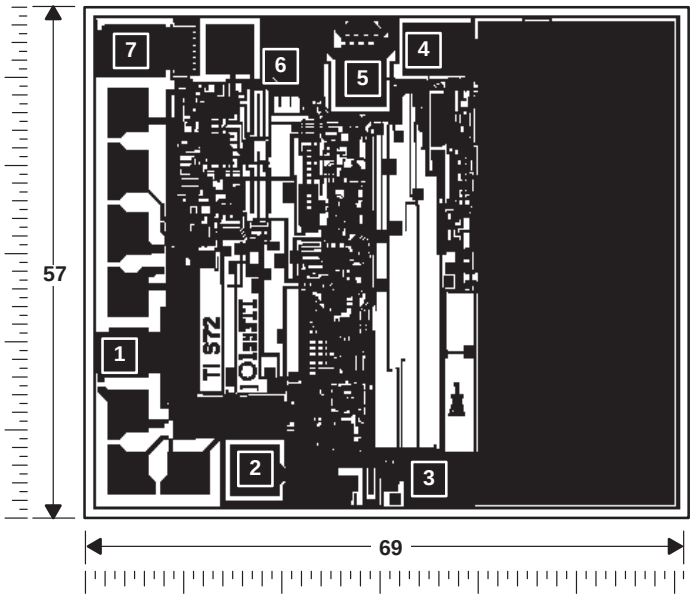
NOTE A: Capacitor selection is nontrivial. See application information section for details.

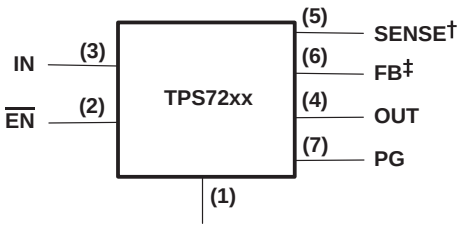
Figure 2. Typical Application Configuration

TPS72xx chip information

These chips, when properly assembled, display characteristics similar to the TPS72xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

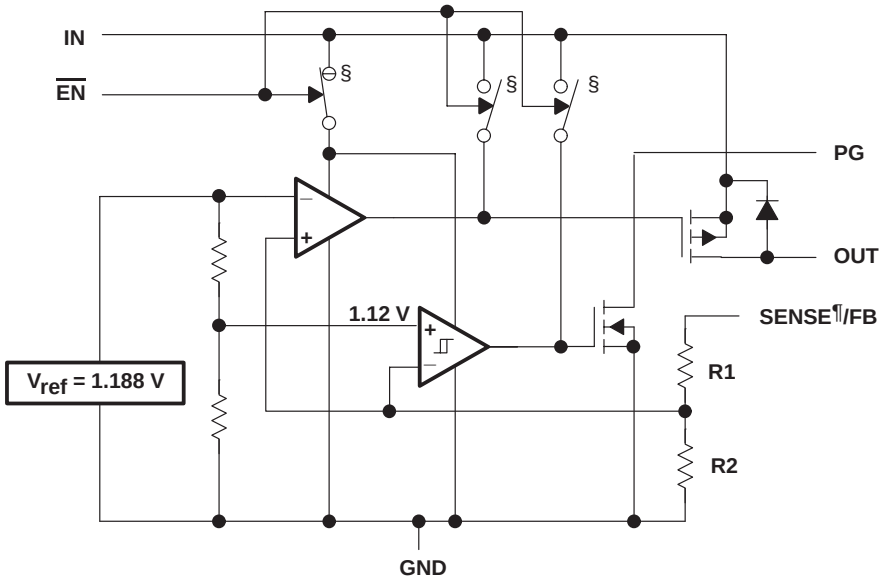
ALL DIMENSIONS ARE IN MILS.

† Fixed-voltage options only (TPS7225, TPS7230, TPS7233, TPS7248, and TPS7250)

‡ Adjustable version only (TPS7201)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to the SENSE-pin connection discussion in the application information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7201	0	∞	Ω
TPS7225	257	233	kΩ
TPS7230	357	233	kΩ
TPS7233	420	233	kΩ
TPS7248	726	233	kΩ
TPS7250	756	233	kΩ

NOTE A: Resistors are nominal values only.

COMPONENT COUNT	
MOS transistors	108
Bilpolar transistors	41
Diodes	4
Capacitors	15
Resistors	75

§ Switch positions are shown with $\overline{EN}$ low (active).

¶ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to the SENSE-pin connection discussion in application information section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I, PG, SENSE, $\overline{EN}$ . . . . . –0.3 V to 11 V
Output current, I_O . . . . . 1.5 A
Continuous total power dissipation . . . . . See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J . . . . . –55°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Note 1 and Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1175 mW	8.74 mW/°C	782 mW	650 mW	301 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Note 1 and Figure 4)

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2063 mW	16.5 mW/°C	1320 mW	1073 mW	413 mW
P	2738 mW	20.49 mW/°C	1816 mW	1508 mW	689 mW
PW	2900 mW	23.2 mW/°C	1856 mW	1508 mW	580 mW

NOTE 1: Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum of 150°C. For guidelines on maintaining junction temperature within the recommended operating range, see application information section.

MAXIMUM CONTINUOUS DISSIPATION vs FREE-AIR TEMPERATURE

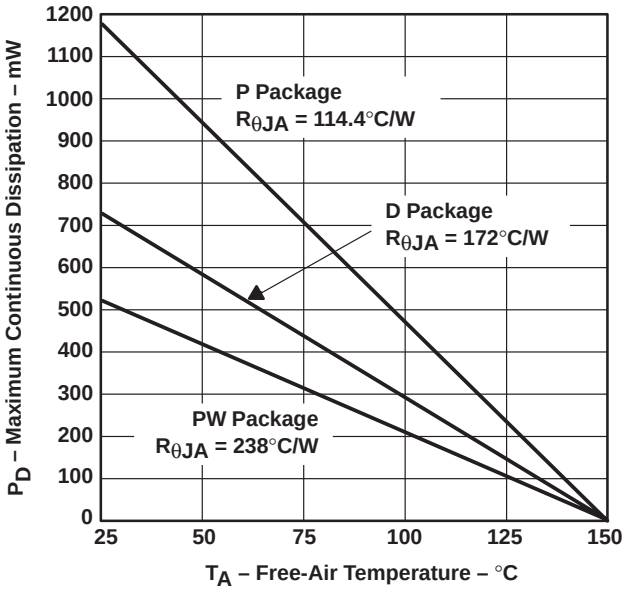


Figure 3

MAXIMUM CONTINUOUS DISSIPATION vs CASE TEMPERATURE

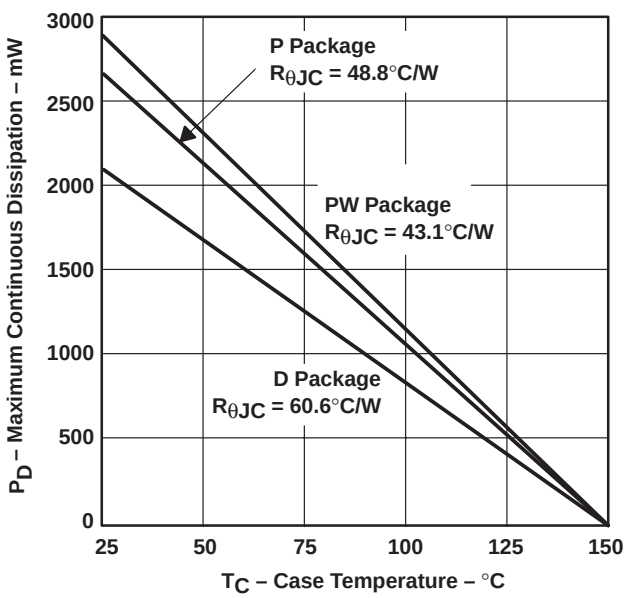


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7201Q	3	10	V
	TPS7225Q	3.65	10	
	TPS7230Q	3.96	10	
	TPS7233Q	3.98	10	
	TPS7248Q	5.24	10	
	TPS7250Q	5.41	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current, I_O		0	250	mA
Operating virtual junction temperature, T_J		–40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, *the usable range can be extended for lighter loads*. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7201 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 under the TPS7201 electrical characteristics table. The minimum value of 3 V is the absolute lower limit for the recommended input-voltage range for the TPS7201.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS72xxQ			UNIT
				MIN	TYP	MAX	
Ground current (active mode)	EN ≤ 0.5 V, 0 mA ≤ I_O ≤ 250 mA	$V_I = V_O$ + 1 V,	25°C		180	225	μA
			–40°C to 125°C			325	
Input current (standby mode)	$\overline{EN} = V_I$,	3 V ≤ V_I ≤ 10 V	25°C			0.5	μA
			–40°C to 125°C			1	
Output current limit threshold	V_O = 0 V	V_I = 10 V	25°C		0.6	1	A
			–40°C to 125°C			1.5	
Pass-element leakage current in standby mode	EN = V_I,	3 V ≤ V_I ≤ 10 V	25°C			0.5	μA
			–40°C to 125°C			1	
PG leakage current	V_{PG} = 10 V,	Normal operation	25°C			0.5	μA
			–40°C to 125°C			0.5	
Output voltage temperature coefficient			–40°C to 125°C		31	75	ppm/°C
Thermal shutdown junction temperature					165		°C
$\overline{EN}$ logic high (standby mode)	3 V ≤ V_I ≤ 6 V		–40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V			2.7			
$\overline{EN}$ logic low (active mode)	3 V ≤ V_I ≤ 10 V		25°C			0.5	V
			–40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage			25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V		25°C	–0.5		0.5	μA
			–40°C to 125°C	–0.5		0.5	
Minimum V_I for active pass element			25°C		1.9	2.5	V
			–40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 μA		25°C		1.1	1.5	V
			–40°C to 125°C			1.9	

† CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q electrical characteristics, I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7201Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.188		V
	3 V ≤ V_I ≤ 10 V, See Note 2	5 mA ≤ I_O ≤ 250 mA,	–40°C to 125°C	1.152		1.224	V
Reference voltage temperature coefficient			–40°C to 125°C		31	75	ppm/°C
Pass-element series resistance (see Note 3)	V_I = 2.4 V,§	50 μA ≤ I_O ≤ 100 mA	25°C		2.1		Ω
	V_I = 2.4 V,§	100 mA ≤ I_O ≤ 200 mA	25°C		2.9		
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		1.6	2.7	
			–40°C to 125°C			4.5	
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		1		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		0.8		
Input regulation	V_I = 3 V to 10 V, See Note 2	50 μA ≤ I_O ≤ 250 mA,	25°C			23	mV
			–40°C to 125°C			36	
Output regulation	I_O = 5 mA to 250 mA, See Note 2	3 V ≤ V_I ≤ 10 V,	25°C		15	25	mV
			–40°C to 125°C			36	
	I_O = 50 μA to 250 mA, See Note 2	3 V ≤ V_I ≤ 10 V,	25°C		17	27	
			–40°C to 125°C			43	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	49	60		dB
			–40°C to 125°C	32			
		I_O = 250 mA, See Note 2	25°C	45	50		
			–40°C to 125°C	30			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		235		μVrms
		C_O = 10 μF	25°C		190		
		C_O = 100 μF	25°C		125		
PG trip-threshold voltage¶	V_{FB} voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{FB(nom)}$		V
PG hysteresis voltage¶	Measured at V_{FB}		25°C		12		mV
PG output low voltage¶	I_{PG} = 400 μA,	V_I = 2.13 V	25°C		0.1	0.4	V
			–40°C to 125°C			0.4	
FB input current			25°C	–10	0.1	10	nA
			–40°C to 125°C	–20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ This voltage is not recommended.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2. When V_I < 2.9 V and I_O > 100 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

TPS7225Q electrical characteristics, I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7225Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 3.5 V,	I_O = 10 mA	25°C		2.5		V
	3.5 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	2.45		2.55	
Dropout voltage	I_O = 250 mA,	V_I = 2.97 V	25°C		560	850	mV
			–40°C to 125°C			1.1	V
Pass-element series resistance	(2.97 V – V_O)/I_O, I_O = 250 mA	V_I = 2.97 V,	25°C		2.24	3.4	Ω
			–40°C to 125°C			3.84	
Input regulation	V_I = 3.5 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C		9	27	mV
			–40°C to 125°C			33	
Output regulation	I_O = 5 mA to 250 mA,	3.5 V ≤ V_I ≤ 10 V	25°C		28	36	mV
			–40°C to 125°C			60	
	I_O = 50 μA to 250 mA,	3.5 V ≤ V_I ≤ 10 V	25°C		24	41	
			–40°C to 125°C			73	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	47	58		dB
			–40°C to 125°C	45			
		I_O = 250 mA	25°C	40	46		
			–40°C to 125°C	38			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		248		μVrms
		C_O = 10 μF	25°C		200		
		C_O = 100 μF	25°C		130		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 2.13 V	25°C		0.3	0.44	V
			–40°C to 125°C			0.5	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7230Q electrical characteristics, I_O = 10 mA, V_I = 4 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7230Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V,	I_O = 10 mA	25°C		3		V
	4 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	2.94		3.06	
Dropout voltage	I_O = 100 mA,	V_I = 2.97 V	25°C		145	185	mV
			–40°C to 125°C			270	
	I_O = 250 mA,	V_I = 2.97 V	25°C		390	502	
			–40°C to 125°C			900	
Pass-element series resistance	(2.97 V – V_O)/I_O, I_O = 250 mA	V_I = 2.97 V,	25°C		1.56	2.01	Ω
			–40°C to 125°C			3.6	
Input regulation	V_I = 4 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C		9	27	mV
			–40°C to 125°C			33	
Output regulation	I_O = 5 mA to 250 mA,	4 V ≤ V_I ≤ 10 V	25°C		34	45	mV
			–40°C to 125°C			74	
	I_O = 50 μA to 250 mA,	4 V ≤ V_I ≤ 10 V	25°C		42	60	
			–40°C to 125°C			98	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	45	56		dB
			–40°C to 125°C	44			
		I_O = 250 mA	25°C	40	45		
			–40°C to 125°C	38			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		256		μVrms
		C_O = 10 μF	25°C		206		
		C_O = 100 μF	25°C		132		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 2.55 V	25°C		0.25	0.44	V
			–40°C to 125°C			0.44	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7233Q electrical characteristics, I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7233Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		14	20	mV
			–40°C to 125°C			30	
	I_O = 100 mA,	V_I = 3.23 V	25°C		140	180	
			–40°C to 125°C			232	
	I_O = 250 mA,	V_I = 3.23 V	25°C		360	460	
			–40°C to 125°C			610	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,	25°C		1.5	1.84	Ω
			–40°C to 125°C			2.5	
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C		8	25	mV
			–40°C to 125°C			33	
Output regulation	I_O = 5 mA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		32	42	mV
			–40°C to 125°C			71	
	I_O = 50 μA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		41	55	
			–40°C to 125°C			98	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	40	52		dB
			–40°C to 125°C	38			
		I_O = 250 mA	25°C	35	44		
			–40°C to 125°C	33			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		265		μVrms
		C_O = 10 μF	25°C		212		
		C_O = 100 μF	25°C		135		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		32		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7248Q electrical characteristics, I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7248Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 5.85 V,	I_O = 10 mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	4.75		4.95	
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V	25°C		10	19	mV
			–40°C to 125°C			30	
	I_O = 100 mA,	V_I = 4.75 V	25°C		90	100	
			–40°C to 125°C			150	
	I_O = 250 mA,	V_I = 4.75 V	25°C		216	250	
			–40°C to 125°C			285	
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,	25°C		0.8	1	Ω
			–40°C to 125°C			1.4	
Input regulation	V_I = 5.85 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C			34	mV
			–40°C to 125°C			50	
Output regulation	I_O = 5 mA to 250 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		43	55	mV
			–40°C to 125°C			95	
	I_O = 50 μA to 250 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		55	75	
			–40°C to 125°C			135	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	42	53		dB
			–40°C to 125°C	36			
		I_O = 250 mA	25°C	36	46		
			–40°C to 125°C	34			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		370		μVrms
		C_O = 10 μF	25°C		290		
		C_O = 100 μF	25°C		168		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.12 V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7250Q electrical characteristics, I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7250Q			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		8	12	mV
			–40°C to 125°C			30	
	I_O = 100 mA,	V_I = 4.88 V	25°C		76	85	
			–40°C to 125°C			136	
	I_O = 250 mA,	V_I = 4.88 V	25°C		190	206	
			–40°C to 125°C			312	
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 250 mA	V_I = 4.88 V,	25°C		0.76	0.825	Ω
			–40°C to 125°C			1.25	
Input regulation	V_I = 6 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C			28	mV
			–40°C to 125°C			35	
Output regulation	I_O = 5 mA to 250 mA,	6 V ≤ V_I ≤ 10 V	25°C		46	61	mV
			–40°C to 125°C			100	
	I_O = 50 μA to 250 mA,	6 V ≤ V_I ≤ 10 V	25°C		59	79	
			–40°C to 125°C			150	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	41	52		dB
			–40°C to 125°C	37			
		I_O = 250 mA	25°C	36	46		
			–40°C to 125°C	32			
Output noise spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		390		μVrms
		C_O = 10 μF	25°C		300		
		C_O = 100 μF	25°C		175		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C		0.95 × $V_{O(nom)}$		V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.19	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS72xxY			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O$ + 1 V, 0 mA ≤ I_O ≤ 250 mA		180		μA
Output current limit threshold	V_O = 0 V, V_I = 10 V		0.6		A
Thermal shutdown junction temperature			165		°C
$\overline{EN}$ hysteresis voltage			50		mV
Minimum V_I for active pass element			1.9		V
Minimum V_I for valid PG	I_{PG} = 300 μA		1.1		V

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7201Y			UNIT
			MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA		1.188		V
Pass-element series resistance (see Note 3)	V_I = 2.4 V,§	50 μA ≤ I_O ≤ 100 mA		2.1		Ω
	V_I = 2.4 V,§	100 mA ≤ I_O ≤ 200 mA		2.9		
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 250 mA		1.6		
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 250 mA		1		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 250 mA		0.8		
Output regulation	3 V ≤ V_I ≤ 10 V, See Note 2	I_O = 5 mA to 250 mA,		15		mV
	3 V ≤ V_I ≤ 10 V, See Note 2	I_O = 50 μA to 250 mA,		17		
Ripple rejection	V_I = 3.5 V, f = 120 Hz	I_O = 50 μA		60		dB
		I_O = 250 mA, See Note 2		50		
Output noise spectral density	V_I = 3.5 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 3.5 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		235		μVrms
		C_O = 10 μF		190		
		C_O = 100 μF		125		
PG hysteresis voltage¶	V_I = 3.5 V,	Measured at V_{FB}		12		mV
PG output low voltage¶	V_I = 2.13 V,	I_{PG} = 400 μA		0.1		V
FB input current	V_I = 3.5 V			0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ This voltage is not recommended.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2 When V_I < 2.9 V and I_O > 100 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3 To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7225Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 3.5 V,	I_O = 10 mA		2.5		V
Dropout voltage	V_I = 2.97 V,	I_O = 250 mA		560		mV
Pass-element series resistance	(2.97 V – V_O)/I_O, I_O = 250 mA	V_I = 2.97 V,		2.24		Ω
Input regulation	V_I = 3.5 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		9		mV
Output regulation	3.5 V ≤ V_I ≤ 10 V	I_O = 5 mA to 250 mA		28		mV
	3.5 V ≤ V_I ≤ 10 V	I_O = 50 μA to 250 mA		24		
Ripple rejection	V_I = 3.5 V, f = 120 Hz	I_O = 50 μA		58		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 3.5 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 3.5 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		248		μVrms
		C_O = 10 μF		200		
		C_O = 100 μF		130		
PG hysteresis voltage	V_I = 3.5 V			50		mV
PG output low voltage	V_I = 2.13 V	I_{PG} = 1.2 mA		0.3		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7230Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4 V,	I_O = 10 mA		3		V
Dropout voltage	V_I = 2.97 V,	I_O = 100 mA		145		mV
	V_I = 2.97 V,	I_O = 250 mA		390		
Pass-element series resistance	(2.97 V – V_O)/I_O, I_O = 250 mA	V_I = 2.97 V,		1.56		Ω
Input regulation	V_I = 4 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		9		mV
Output regulation	4 V ≤ V_I ≤ 10 V	I_O = 5 mA to 250 mA		34		mV
	4 V ≤ V_I ≤ 10 V	I_O = 50 μA to 250 mA		41		
Ripple rejection	V_I = 4 V, f = 120 Hz	I_O = 50 μA		56		dB
		I_O = 250 mA		45		
Output noise spectral density	V_I = 4 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 4 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		256		μVrms
		C_O = 10 μF		206		
		C_O = 100 μF		132		
PG hysteresis voltage	V_I = 4 V			50		mV
PG output low voltage	V_I = 2.55 V	I_{PG} = 1.2 mA		0.25		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡		TPS7233Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	V_I = 3.23 V,	I_O = 10 mA		14		mV
	V_I = 3.23 V,	I_O = 100 mA		140		
	V_I = 3.23 V,	I_O = 250 mA		360		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,		1.5		Ω
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		8		mV
Output regulation	4.3 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 250 mA		32		mV
	4.3 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 250 mA		41		
Ripple rejection	V_I = 4.3 V, f = 120 Hz	I_O = 50 μA		52		dB
		I_O = 250 mA		44		
Output noise spectral density	V_I = 4.3 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 4.3 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		265		μVrms
		C_O = 10 μF		212		
		C_O = 100 μF		135		
PG hysteresis voltage	V_I = 4.3 V			32		mV
PG output low voltage	V_I = 2.8 V,	I_{PG} = 1.2 mA		0.22		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF (CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7248Y MIN	TPS7248Y TYP	TPS7248Y MAX	UNIT
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	V_I = 4.75 V,	I_O = 10 mA		10		mV
	V_I = 4.75 V,	I_O = 100 mA		90		
	V_I = 4.75 V,	I_O = 250 mA		216		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,		0.8		Ω
Output regulation	5.85 V ≤ V_I ≤ 10 V	I_O = 5 mA to 250 mA		43		mV
	5.85 V ≤ V_I ≤ 10 V	I_O = 50 μA to 250 mA		55		
Ripple rejection	V_I = 5.85 V, f = 120 Hz	I_O = 50 μA		53		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 5.85 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 5.85 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		370		μVrms
		C_O = 10 μF		290		
		C_O = 100 μF		168		
PG hysteresis voltage	V_I = 5.85 V			50		mV
PG output low voltage	V_I = 4.12 V	I_{PG} = 1.2 mA		0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡		TPS7250Y MIN	TPS7250Y TYP	TPS7250Y MAX	UNIT
Output voltage	V_I = 6 V,	I_O = 10 mA		5		V
Dropout voltage	V_I = 4.88 V	I_O = 10 mA		8		mV
	V_I = 4.88 V	I_O = 100 mA		76		
	V_I = 4.88 V,	I_O = 250 mA		190		
Pass-element series resistance	(4.88 V – V_O)/I_O, I_O = 250 mA	V_I = 4.88 V,		0.76		Ω
Input regulation	V_I = 6 V to 10 V,	50 μA ≤ I_O ≤ 250 mA				mV
Output regulation	6 V ≤ V_I ≤ 10 V,	I_O = 5 mA to 250 mA		46		mV
	6 V ≤ V_I ≤ 10 V,	I_O = 50 μA to 250 mA		59		
Ripple rejection	V_I = 6 V, f = 120 Hz	I_O = 50 μA		52		dB
		I_O = 250 mA		46		
Output noise spectral density	V_I = 6 V,	f = 120 Hz		2		μV/√Hz
Output noise voltage	V_I = 6 V, 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		390		μVrms
		C_O = 10 μF		300		
		C_O = 100 μF		175		
PG hysteresis voltage	V_I = 6 V			50		mV
PG output low voltage	V_I = 4.25 V,	I_{PG} = 1.2 mA		0.19		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

Table of Graphs

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V_{DO}	Dropout voltage	vs Output current	8
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		vs Added ceramic capacitance (C_O = 10 μF)	30

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

TYPICAL CHARACTERISTICS

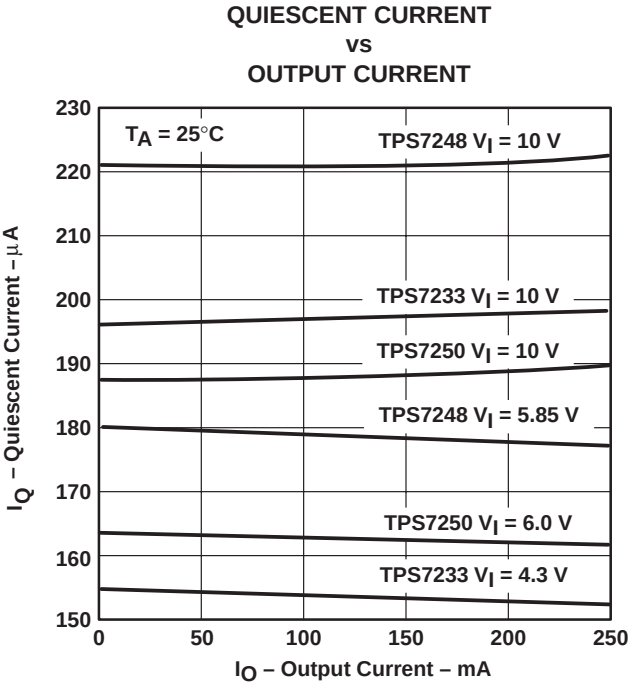


Figure 5

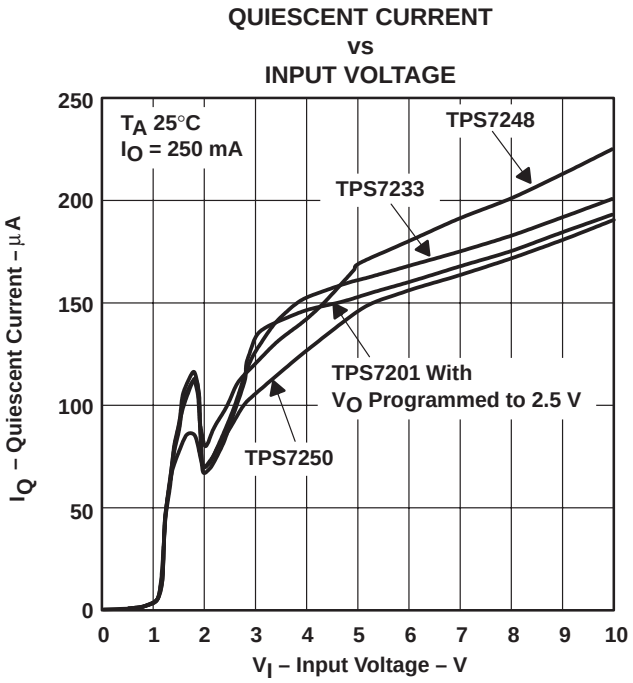


Figure 6

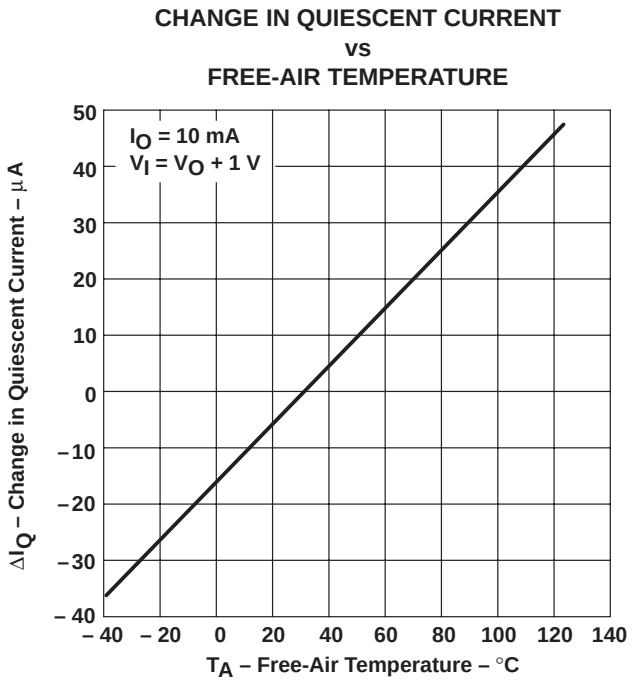


Figure 7

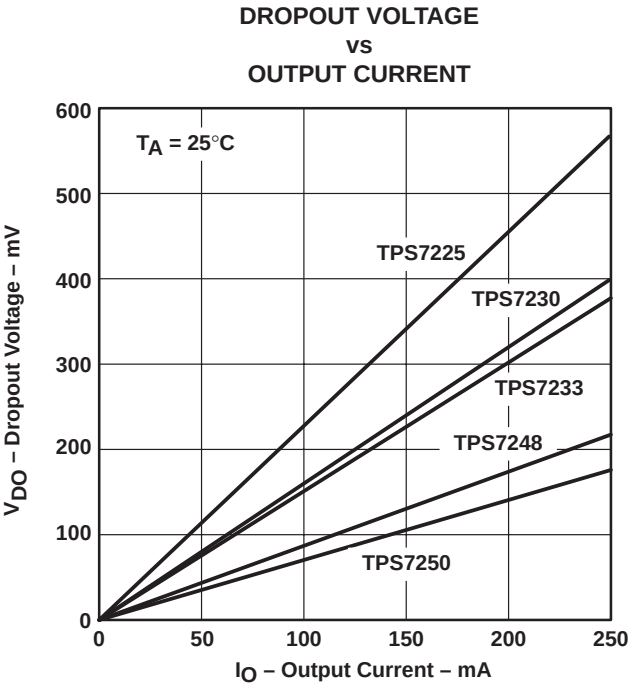


Figure 8

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

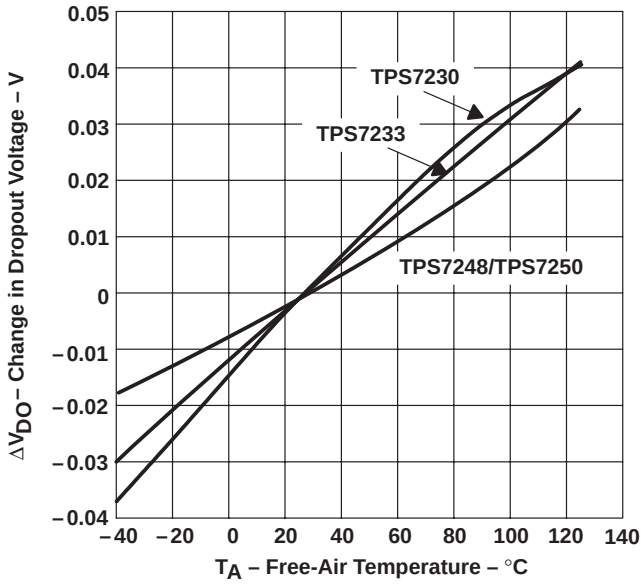
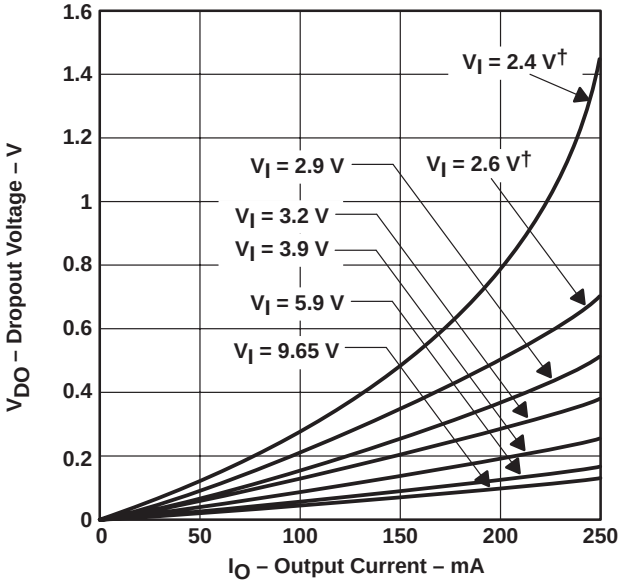


Figure 9

TPS7201
DROPOUT VOLTAGE vs OUTPUT CURRENT



† This voltage is not recommended.

Figure 10

PASS ELEMENT SERIES RESISTANCE vs INPUT VOLTAGE

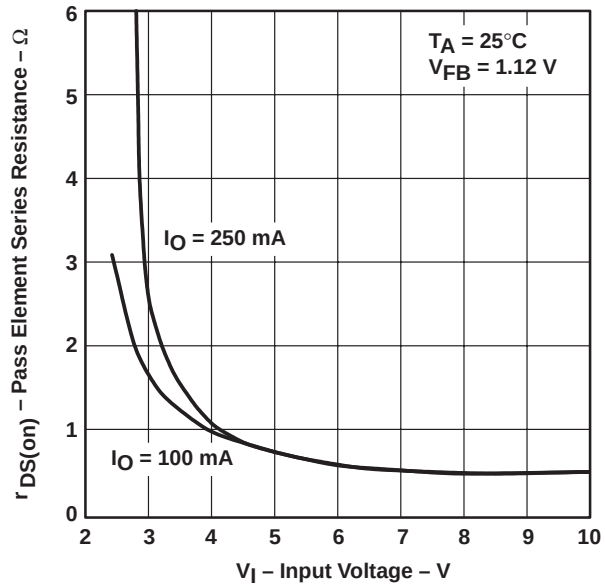


Figure 11

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

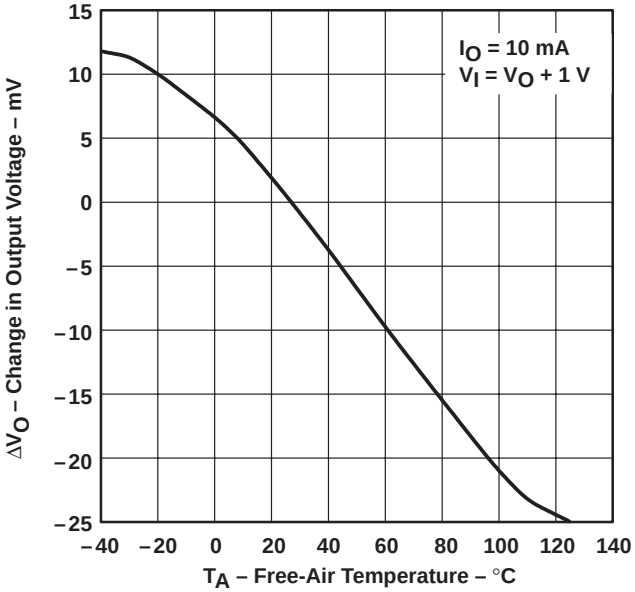


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE

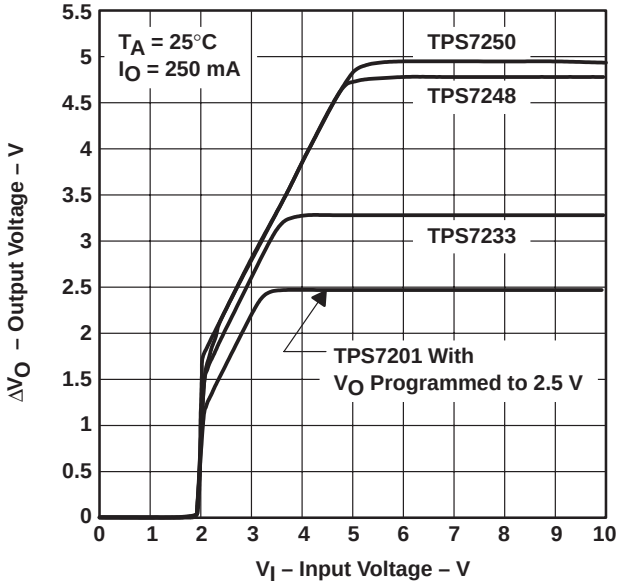


Figure 13

LINE REGULATION

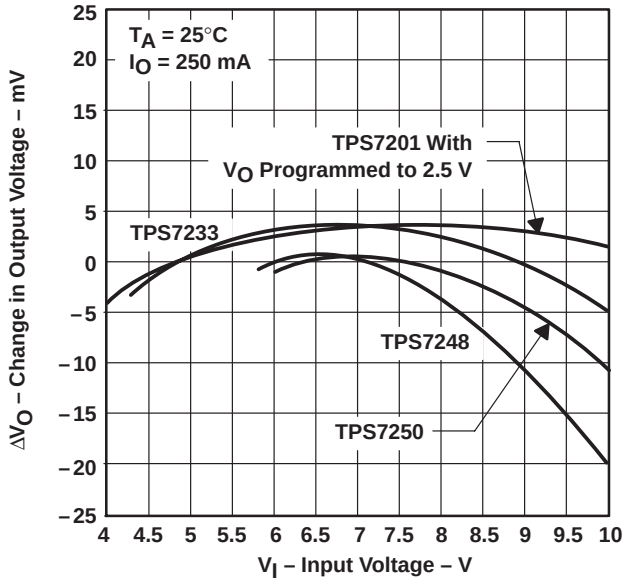


Figure 14

LOAD REGULATION

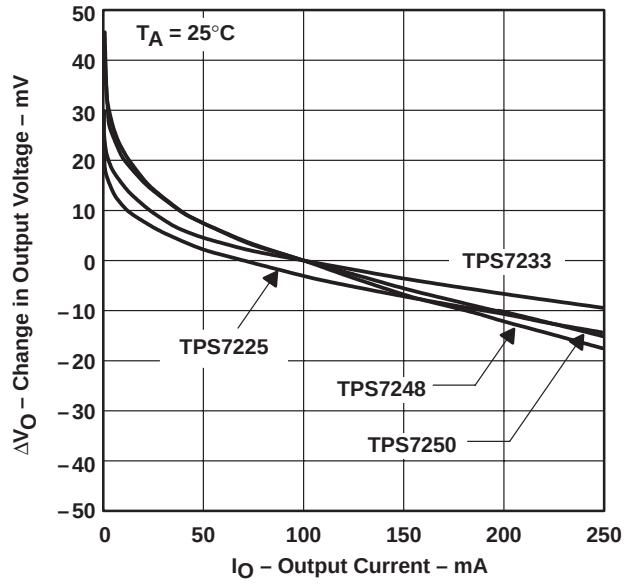
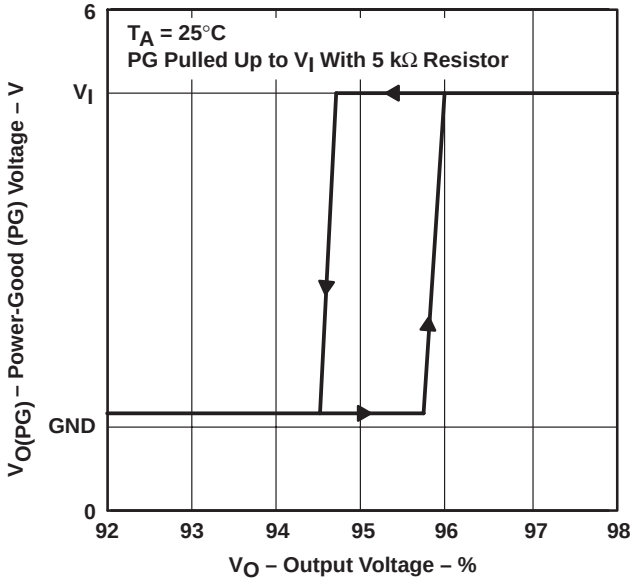


Figure 15

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE†



† V_O as a percent of $V_O$nom.

Figure 16

TYPICAL CHARACTERISTICS

POWER-GOOD (PG) ON-RESISTANCE vs INPUT VOLTAGE

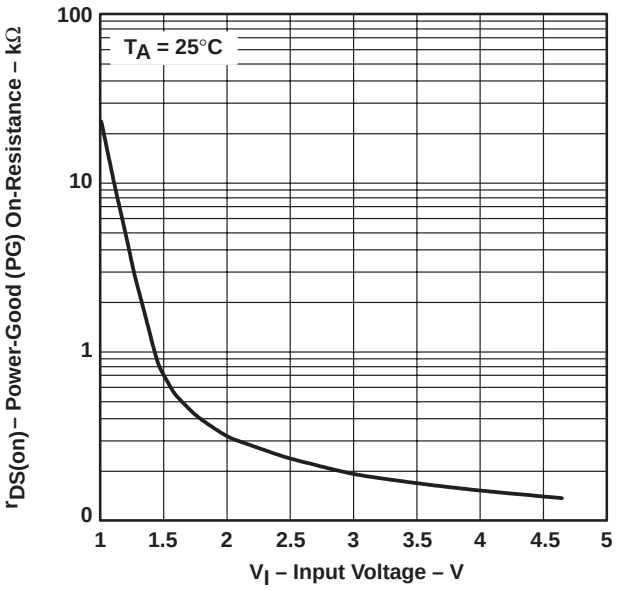


Figure 17

MINIMUM INPUT VOLTAGE FOR VALID PG vs FREE-AIR TEMPERATURE

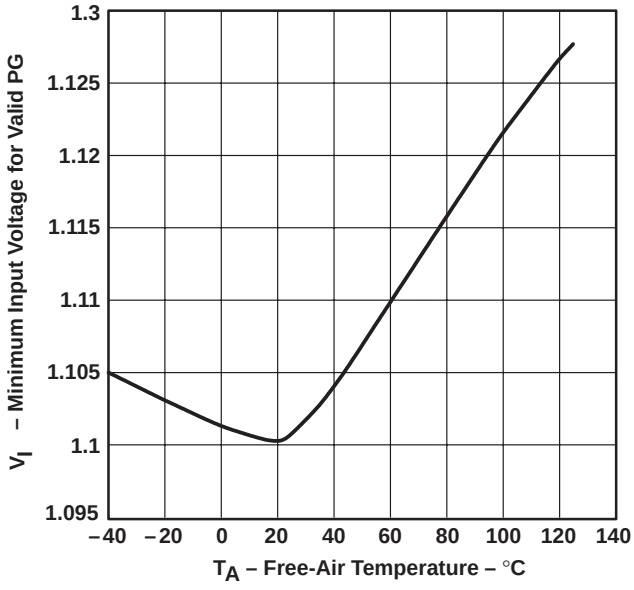


Figure 18

OUTPUT VOLTAGE RESPONSE FROM $\overline{\text{ENABLE}}$ ($\overline{\text{EN}}$)

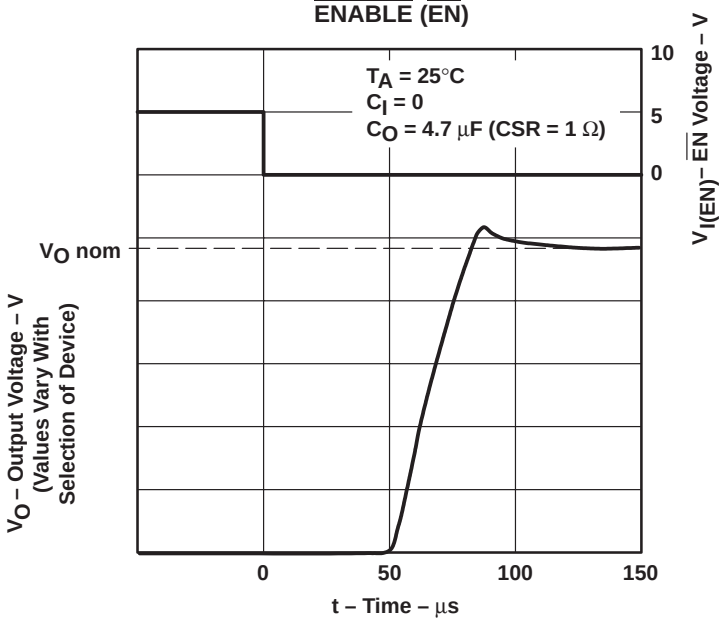


Figure 19

TYPICAL CHARACTERISTICS

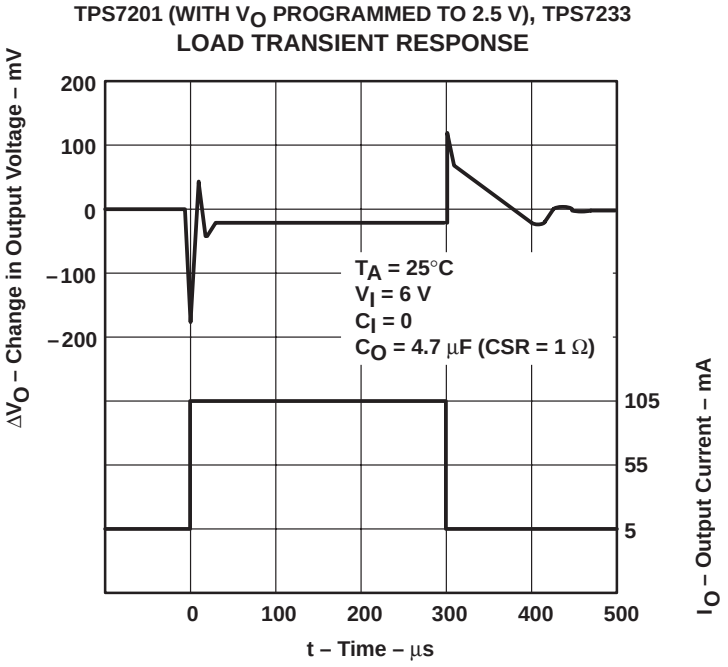


Figure 20

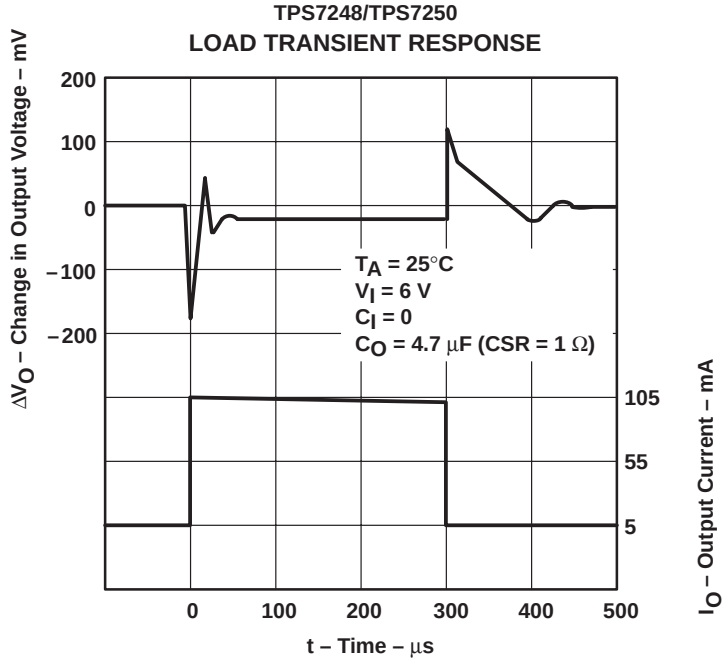


Figure 21

TYPICAL CHARACTERISTICS

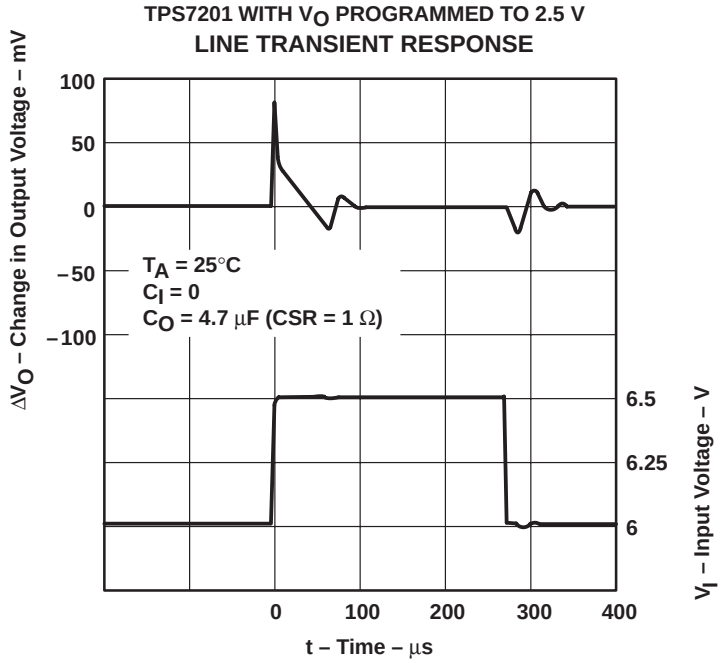


Figure 22

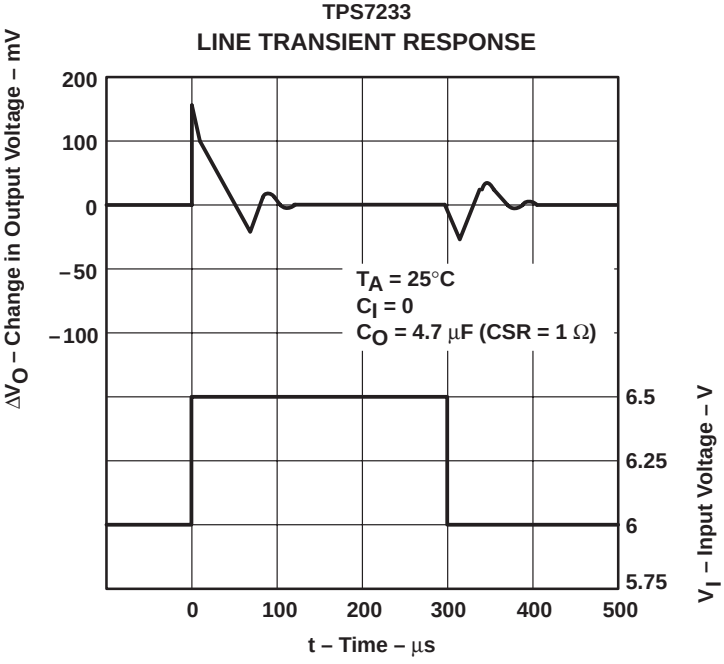


Figure 23

TYPICAL CHARACTERISTICS

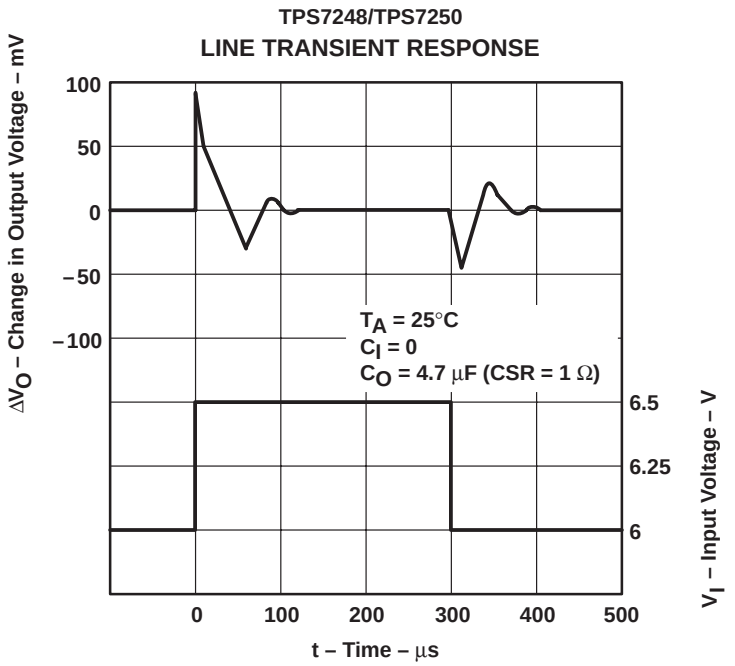


Figure 24

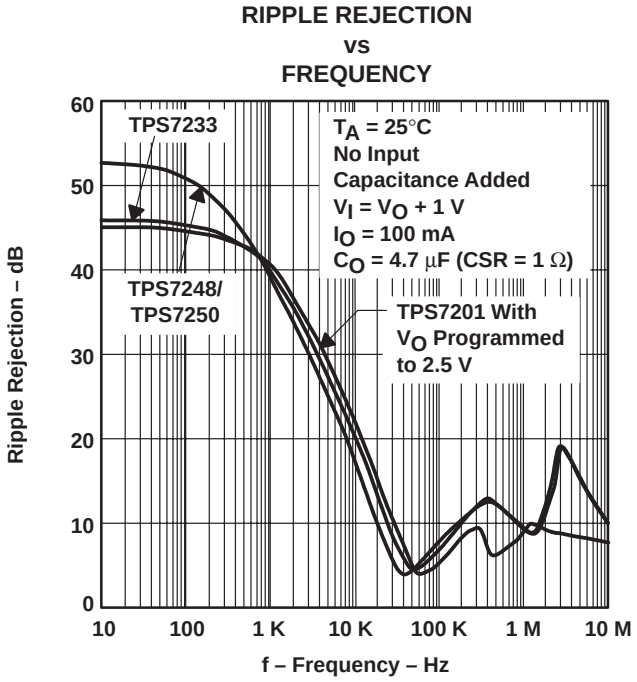


Figure 25

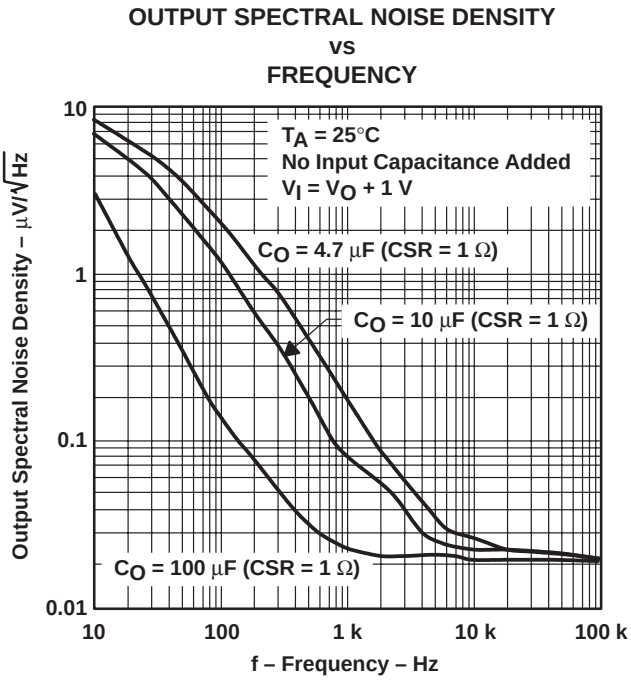


Figure 26

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

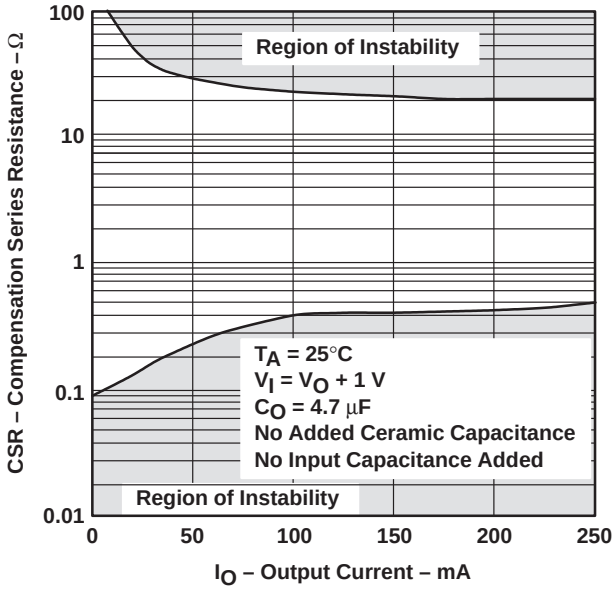


Figure 27

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

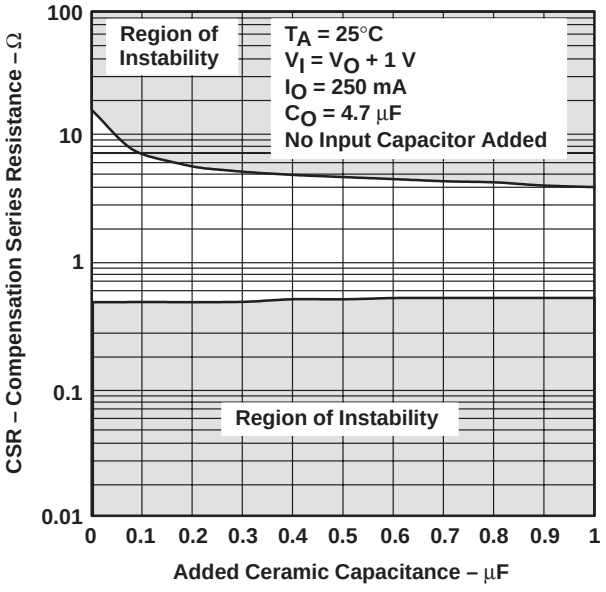


Figure 28

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

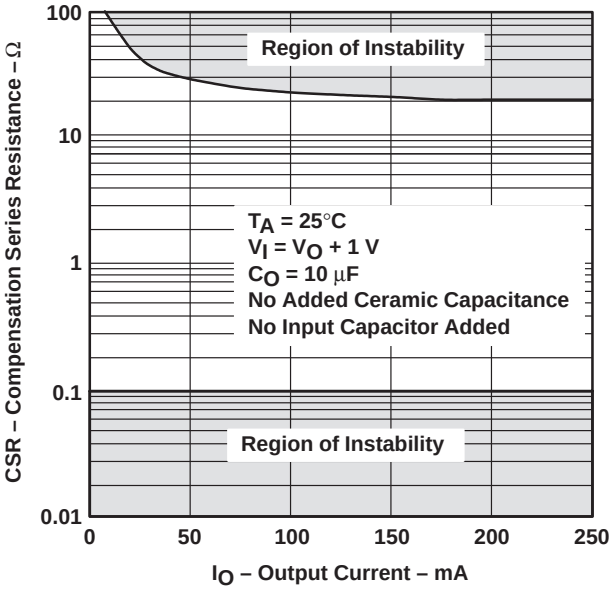


Figure 29

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

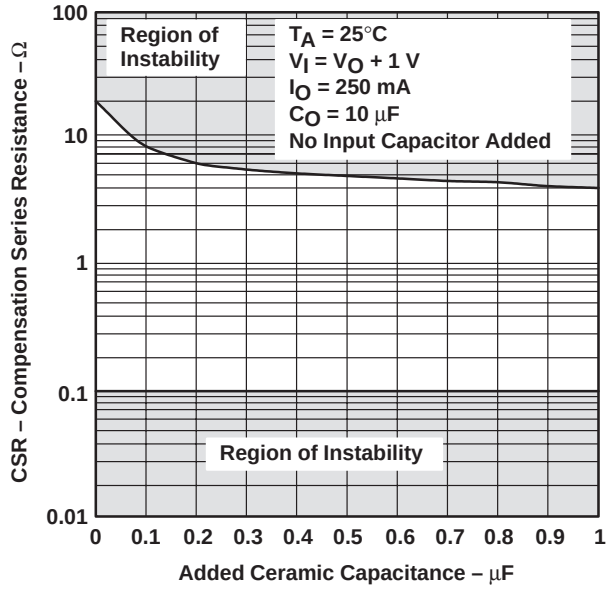


Figure 30

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The design of the TPS72xx family of low-dropout (LDO) regulators is based on the higher-current TPS71xx family. These new families of regulators have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low supply currents that remain constant over the full-output-current range of the device, and an enable input to reduce supply currents to less than 0.5 μA when the regulator is turned off.

device operation

The TPS72xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS transistor is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS72xx is essentially constant from no-load to maximum.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load increases reduce the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 5°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

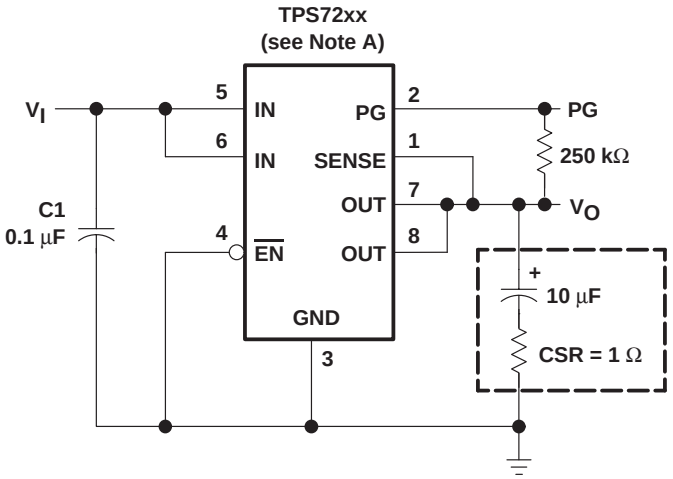
A logic high on the enable input, $\overline{EN}$, shuts off the output and reduces the supply current to less than 0.5 μA. $\overline{EN}$ should be grounded in applications where the shutdown feature is not used.

Power good (PG) is an open-drain output signal used to indicate output-voltage status. A comparator circuit continuously monitors the output voltage. When the output drops to approximately 95% of its nominal regulated value, the comparator turns on and pulls PG low.

Transient loads or line pulses can also cause activation of PG if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μs can cause a signal on PG if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1-μs transient causes a PG signal when using an output capacitor with greater than 3.5 Ω of ESR. It is interesting to note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1-μs transient must drop at least 500 mV below the threshold before tripping the PG circuit. A 2-μs transient trips PG at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

A typical application circuit is shown in Figure 31.

APPLICATION INFORMATION



NOTE A: TPS7225, TPS7230, TPS7233, TPS7248, TPS7250 (fixed-voltage options).

Figure 31. Typical Application Circuit

external capacitor requirements

Although not required, a 0.047-μF to 0.1-μF ceramic bypass input capacitor, connected between IN and GND and located close to the TPS72xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

An output capacitor is required to stabilize the internal feedback loop. For most applications, a 10-μF to 15-μF solid-tantalum capacitor with a 0.5-Ω resistor (see capacitor selection table) in series is sufficient. The maximum capacitor ESR should be limited to 1.3 Ω to allow for ESR doubling at cold temperatures. Figure 32 shows the transient response of a 5-mA to 85-mA load using a 10-μF output capacitor with a total ESR of 1.7 Ω.

A 4.7-μF solid-tantalum capacitor in series with a 1-Ω resistor may also be used (see Figures 27 and 28) provided the ESR of the capacitor does not exceed 1 Ω at room temperature and 2 Ω over the full operating temperature range.

APPLICATION INFORMATION

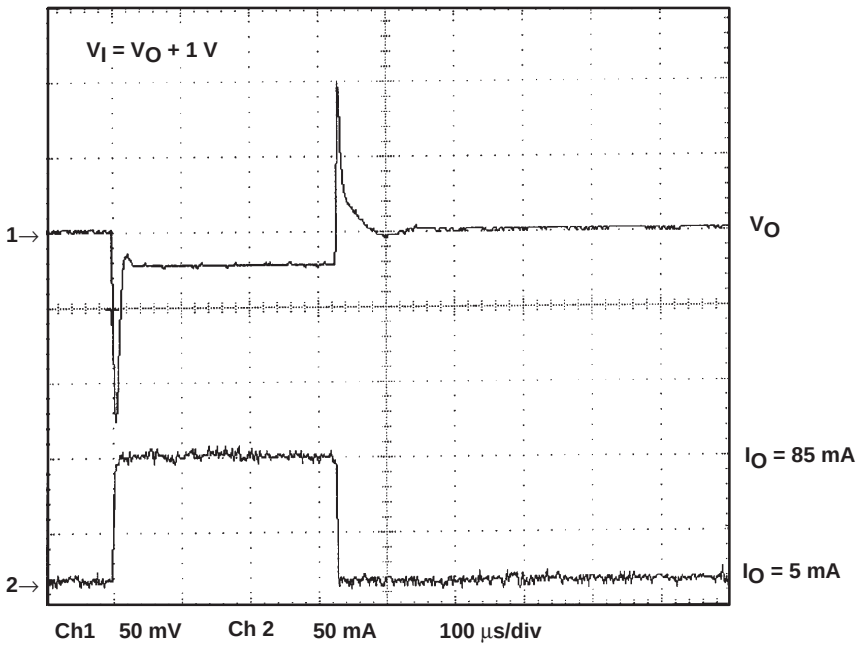


Figure 32. Load Transient Response (CSR total = 1.7 Ω), TPS7248Q

A partial listing of surface-mount capacitors usable with the TPS72xx family is provided below. This information (along with the stability graphs, Figures 27 through 30) is included to assist the designer in selecting suitable capacitors.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and T_A = 25°C. Listings are sorted by height.

sense-pin connection

SENSE must be connected to OUT for proper operation of the regulator. Normally this connection should be as short as possible; however, remote sense may be implemented in critical applications when proper care of the circuit path is exercised. SENSE internally connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and any noise pickup on the PCB trace will feed through to the regulator output. SENSE must be routed to minimize noise pickup. Filtering SENSE using an RC network is not recommended because of the possibility of inducing regulator instability.

APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS7201 adjustable regulator is programmed using an external resistor divider as shown in Figure 33. The output voltage is calculated using:

$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

V_{ref} = 1.188 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \quad (2)$$

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)†	
	R1	R2
2.5	191	169
3.3	309	169
3.6	348	169
4	402	169
5	549	169
6.4	750	169

† 1% values shown.

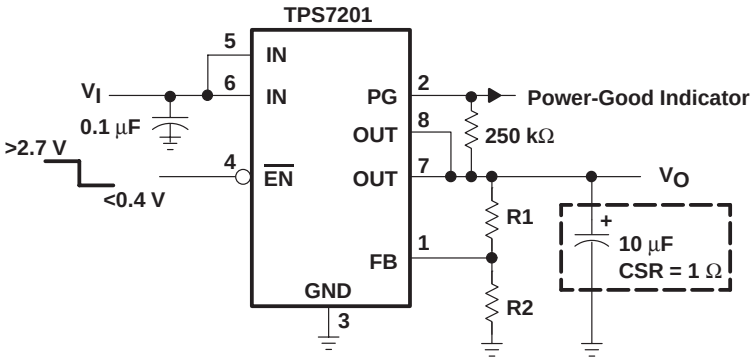


Figure 33. TPS7201 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. These restrictions limit the power dissipation that the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature, i.e.,150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \cdot I_O$$

Power dissipation resulting from quiescent current is negligible.

regulator protection

The TPS72xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS72xx also features internal current limiting and thermal protection. During normal operation, the TPS72xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7201QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7201Q
TPS7201QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7201Q
TPS7201QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7201Q
TPS7201QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7201Q
TPS7201QDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7201Q
TPS7201QP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7201QP
TPS7201QP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7201QP
TPS7201QPW	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7201
TPS7201QPW.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7201
TPS7201QPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7201
TPS7201QPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7201
TPS7225QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	7225Q
TPS7225QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	7225Q
TPS7225QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	7225Q
TPS7225QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	7225Q
TPS7225QP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 150	TPS7225QP
TPS7225QP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 150	TPS7225QP
TPS7225QPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	PT7225
TPS7225QPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	PT7225
TPS7230QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	7230Q
TPS7230QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	7230Q
TPS7230QP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7230QP
TPS7230QP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7230QP
TPS7230QPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7230
TPS7230QPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7230
TPS7233QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7233Q
TPS7233QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7233Q
TPS7233QDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7233Q
TPS7233QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7233Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7233QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7233Q
TPS7233QP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7233QP
TPS7233QP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7233QP
TPS7233QPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7233QP
TPS7233QPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7233
TPS7233QPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7233
TPS7248QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7248Q
TPS7248QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7248Q
TPS7250QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7250Q
TPS7250QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7250Q
TPS7250QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7250Q
TPS7250QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7250Q
TPS7250QP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7250QP
TPS7250QP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPS7250QP
TPS7250QPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7250
TPS7250QPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PT7250

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

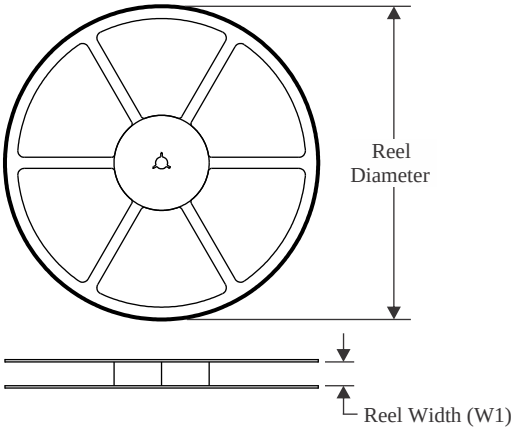
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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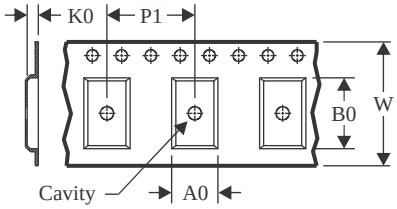
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

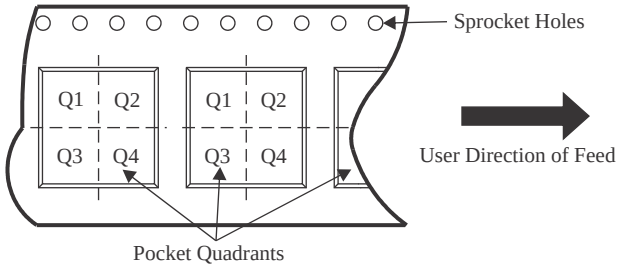


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

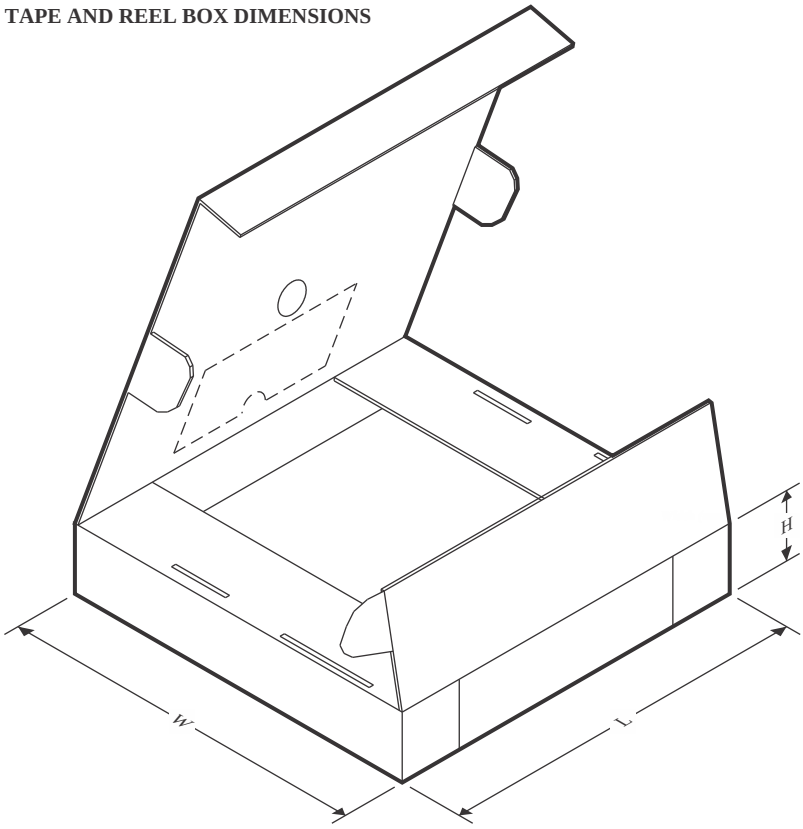
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7201QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7201QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS7225QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7225QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS7230QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS7233QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7233QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS7250QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7250QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

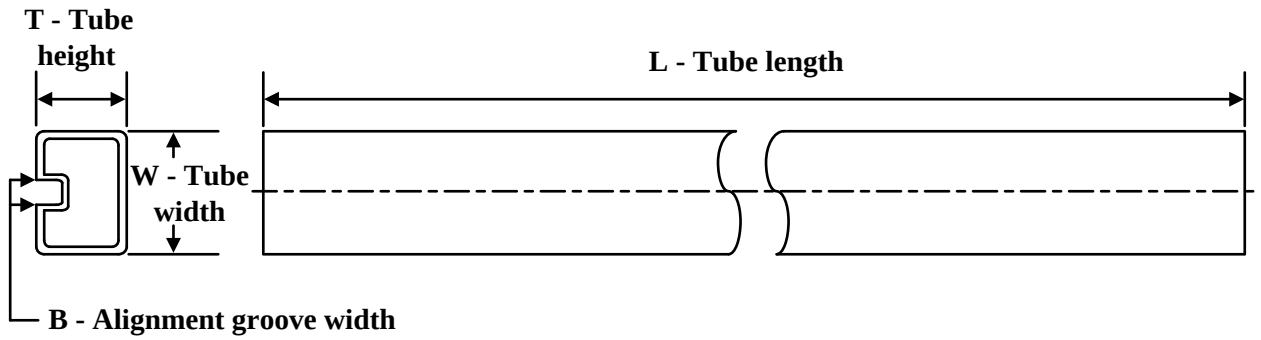
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

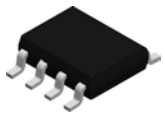
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7201QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS7201QPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TPS7225QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS7225QPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TPS7230QPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TPS7233QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS7233QPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TPS7250QDR	SOIC	D	8	2500	350.0	350.0	43.0
TPS7250QPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7201QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS7201QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS7201QP	P	PDIP	8	50	506	13.97	11230	4.32
TPS7201QP.A	P	PDIP	8	50	506	13.97	11230	4.32
TPS7201QPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS7201QPW.A	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS7225QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS7225QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS7225QP	P	PDIP	8	50	506	13.97	11230	4.32
TPS7225QP.A	P	PDIP	8	50	506	13.97	11230	4.32
TPS7230QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS7230QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS7230QP	P	PDIP	8	50	506	13.97	11230	4.32
TPS7230QP.A	P	PDIP	8	50	506	13.97	11230	4.32
TPS7233QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS7233QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS7233QDG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS7233QP	P	PDIP	8	50	506	13.97	11230	4.32
TPS7233QP.A	P	PDIP	8	50	506	13.97	11230	4.32
TPS7233QPE4	P	PDIP	8	50	506	13.97	11230	4.32
TPS7248QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS7248QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS7250QD	D	SOIC	8	75	505.46	6.76	3810	4
TPS7250QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS7250QP	P	PDIP	8	50	506	13.97	11230	4.32
TPS7250QP.A	P	PDIP	8	50	506	13.97	11230	4.32

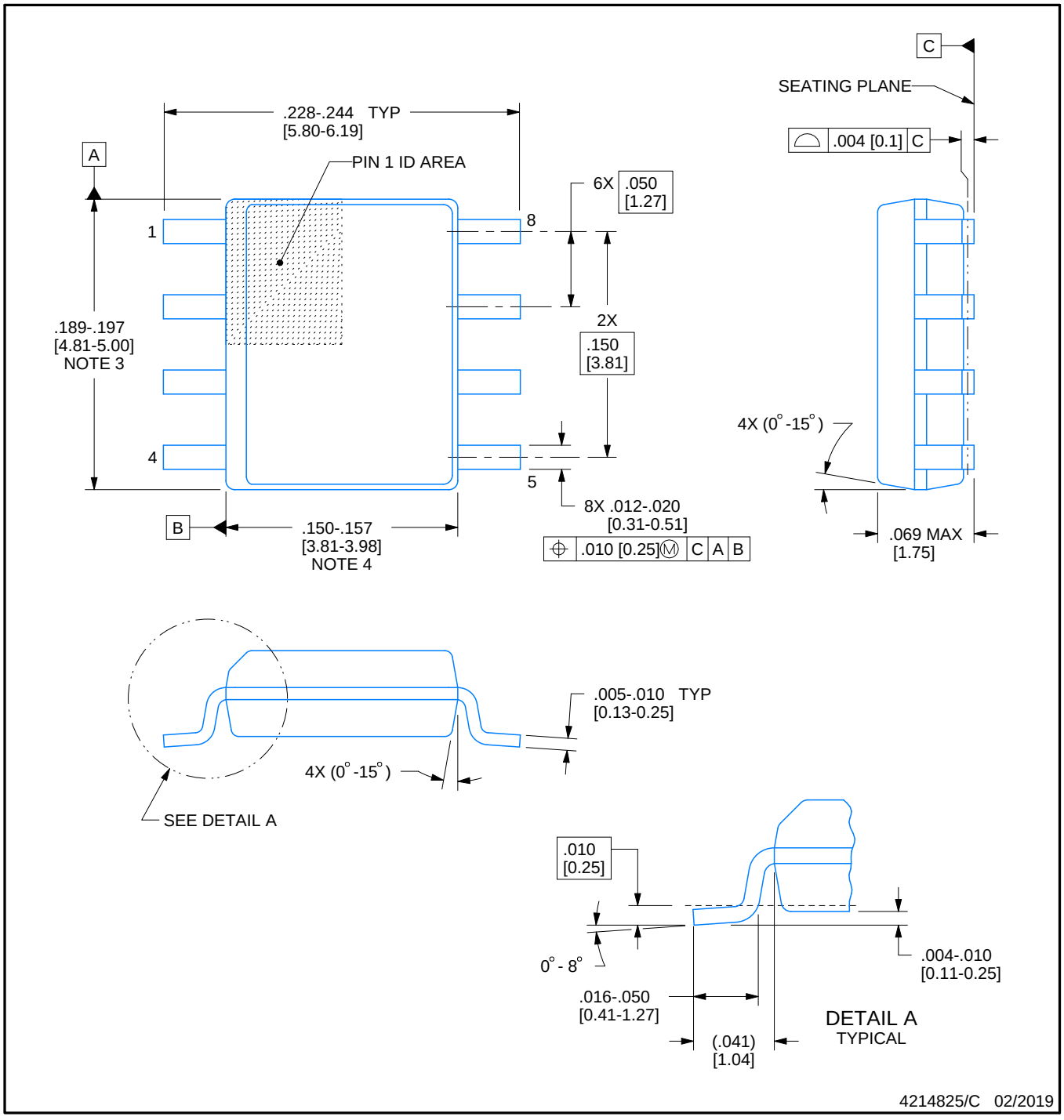


PACKAGE OUTLINE

D0008A

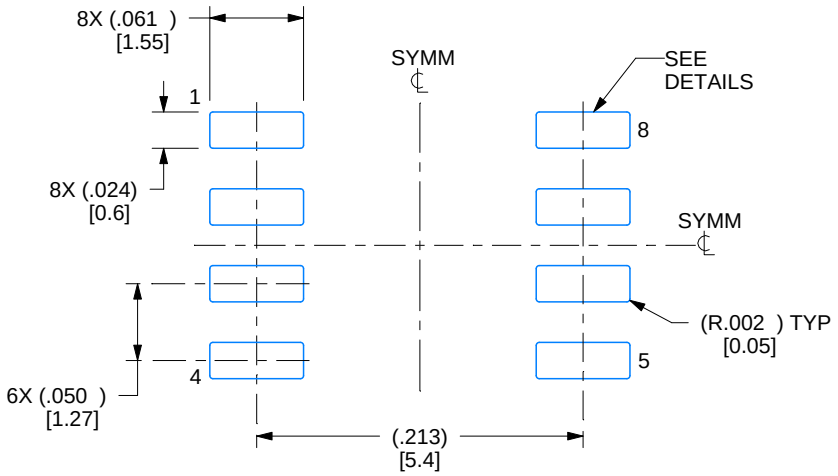
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

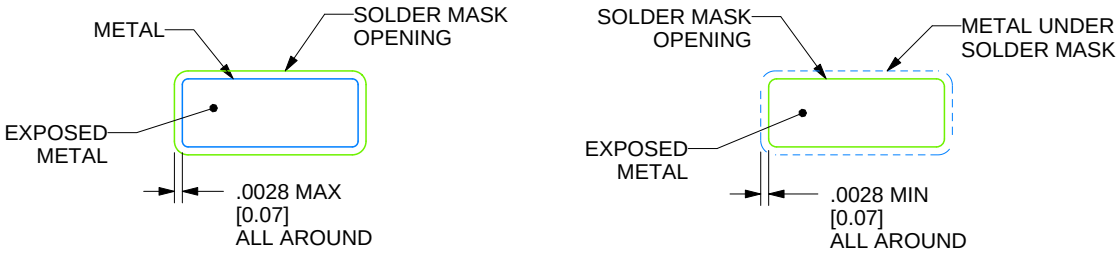


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

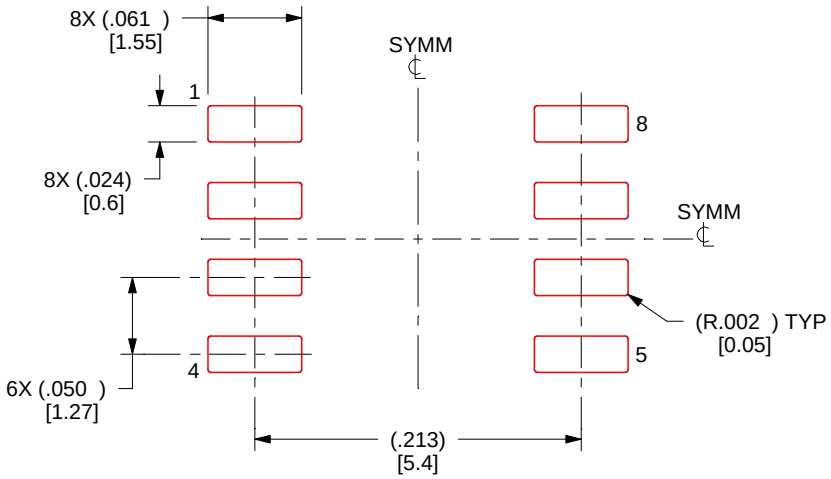
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



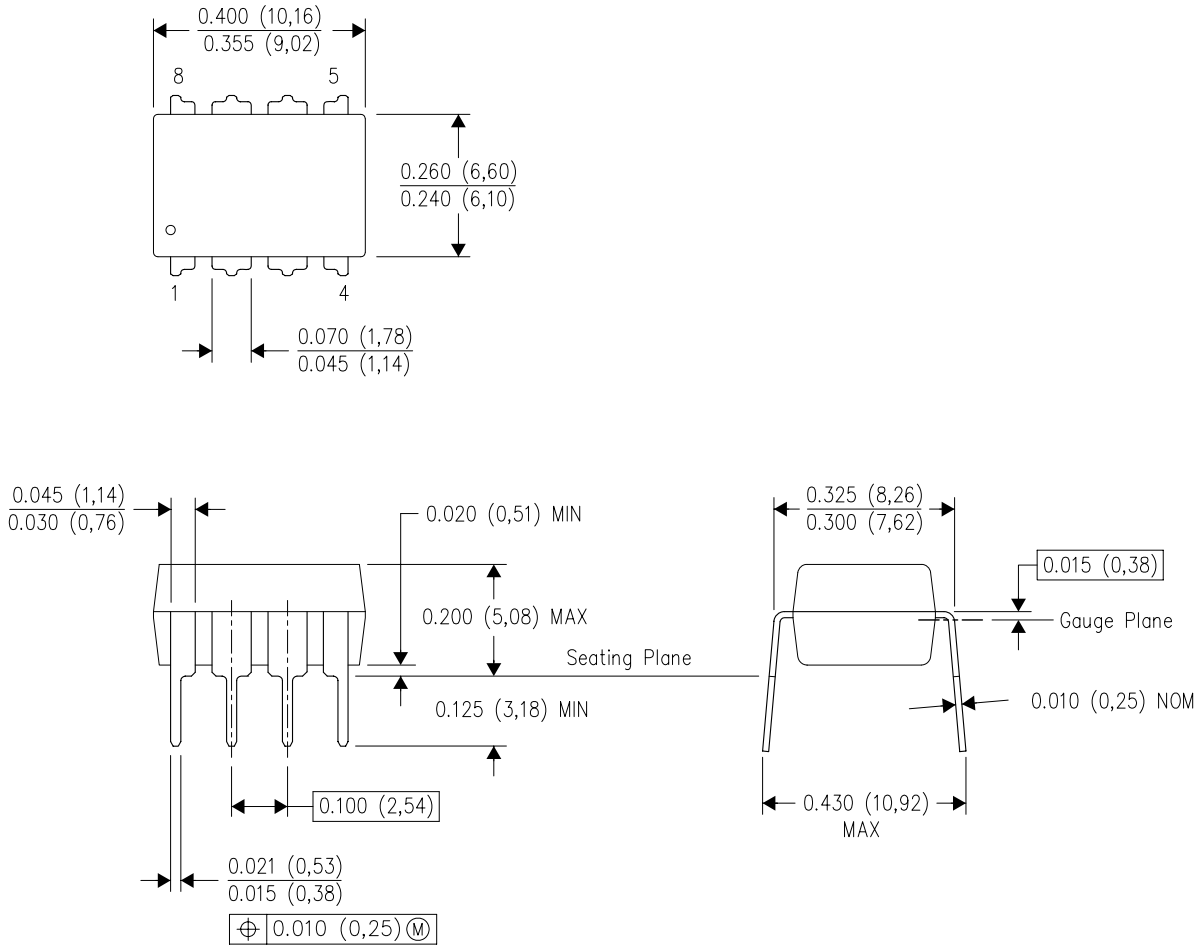
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



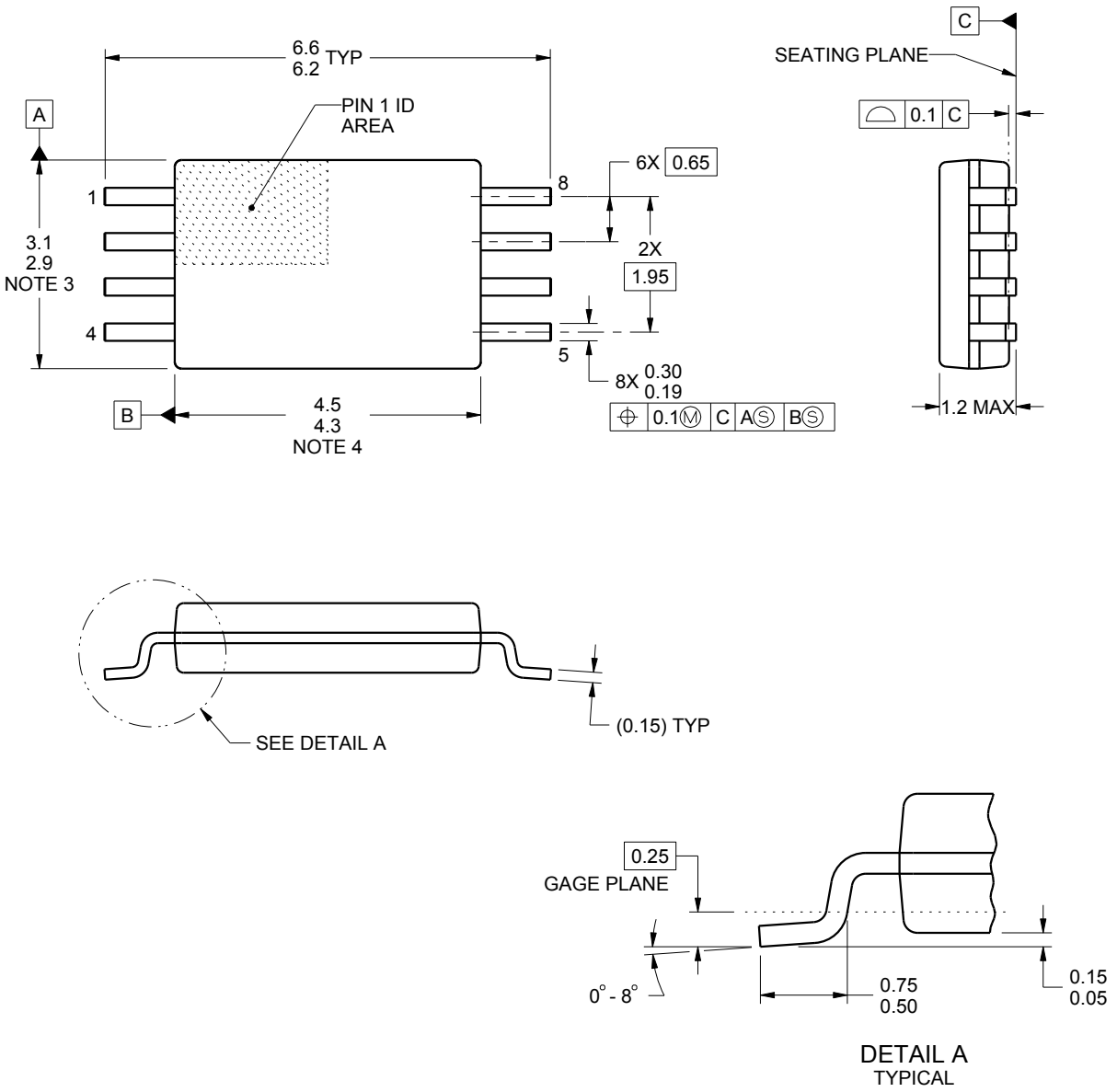
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

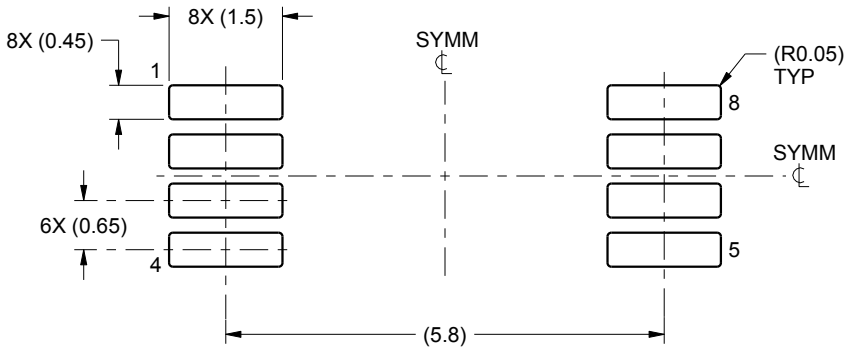
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

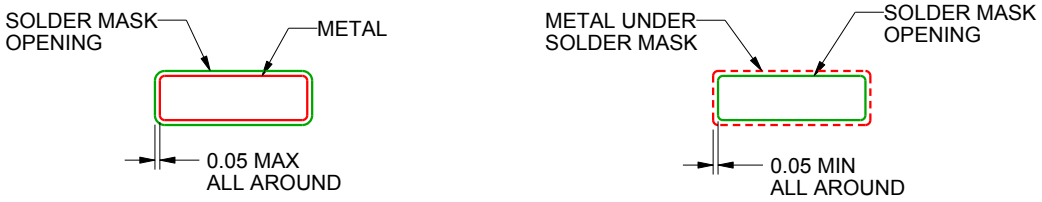


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

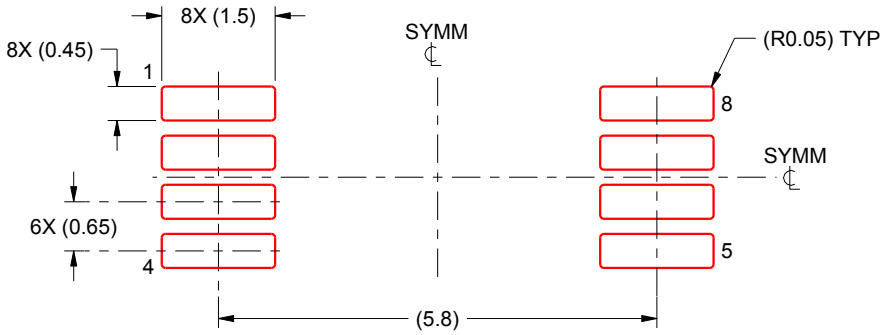


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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