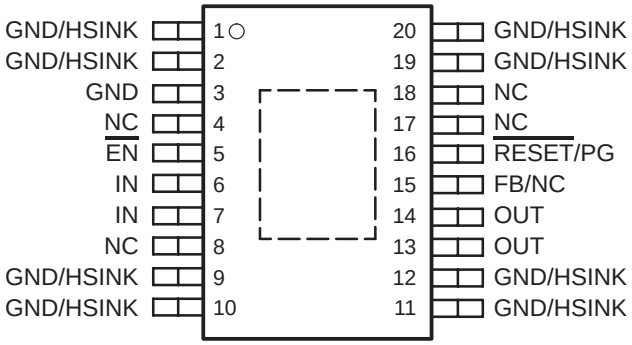
TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 with RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 with PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT LINEAR REGULATORS

SLVS230G − SEPTEMBER 1999 − REVISED JANUARY 2004

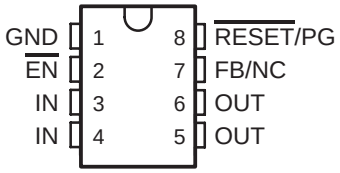
- **Open Drain Power-On Reset With 200 ms Delay (TPS777xx)**
- **Open Drain Power Good (TPS778xx)**
- **750-mA Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 3.3-V Fixed Output and Adjustable Versions**
- **Dropout Voltage to 260 mV (Typ) at 750 mA (TPS77x33)**
- **Ultralow 85 μA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package**
- **Thermal Shutdown Protection**

PWP PACKAGE
(TOP VIEW)



NC − No internal connection

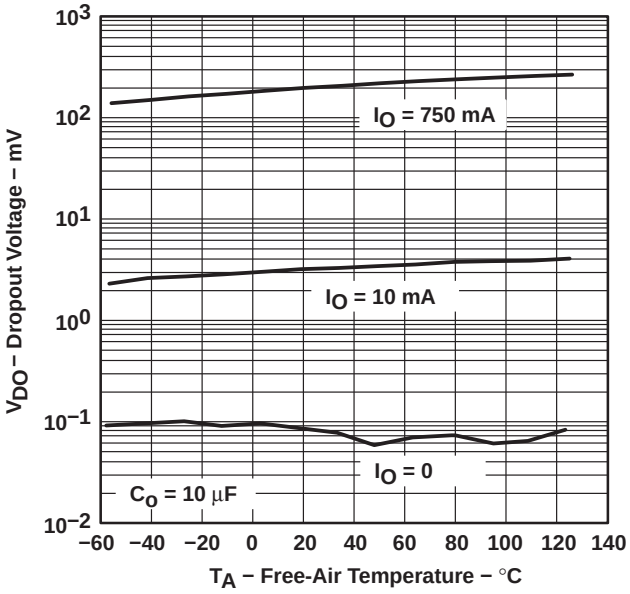
D PACKAGE
(TOP VIEW)



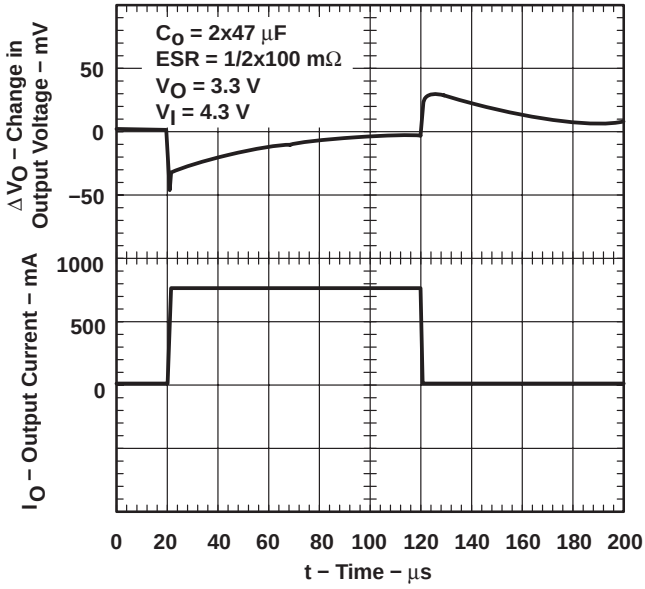
description

TPS777xx and TPS778xx are designed to have a fast transient response and be stable with a 10 μF low ESR capacitor. This combination provides high performance at a reasonable cost.

TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS77x33
LOAD TRANSIENT RESPONSE



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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 260 mV at an output current of 750 mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 750 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μA at T_J = 25°C.

The $\overline{RESET}$ output of the TPS777xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS777xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

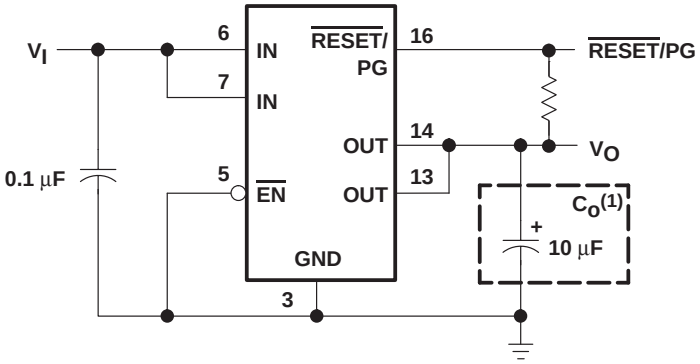
Power good (PG) of the TPS778xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS777xx and TPS778xx are offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V for the TPS77701 option and 1.2 V to 5.5 V for the TPS77801 option). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS777xx and TPS778xx families are available in 8-pin SOIC and 20-pin PWP packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES			
	TYP	TSSOP (PWP)		SOIC (D)	
−40°C to 125°C	3.3	TPS77733PWP	TPS77833PWP	TPS77733D	TPS77833D
	2.5	TPS77725PWP	TPS77825PWP	TPS77725D	TPS77825D
	1.8	TPS77718PWP	TPS77818PWP	TPS77718D	TPS77818D
	1.5	TPS77715PWP	TPS77815PWP	TPS77715D	TPS77815D
	Adjustable 1.5 V to 5.5 V	TPS77701PWP	—	TPS77701D	—
	Adjustable 1.2 V to 5.5 V	—	TPS77801PWP	—	TPS77801D

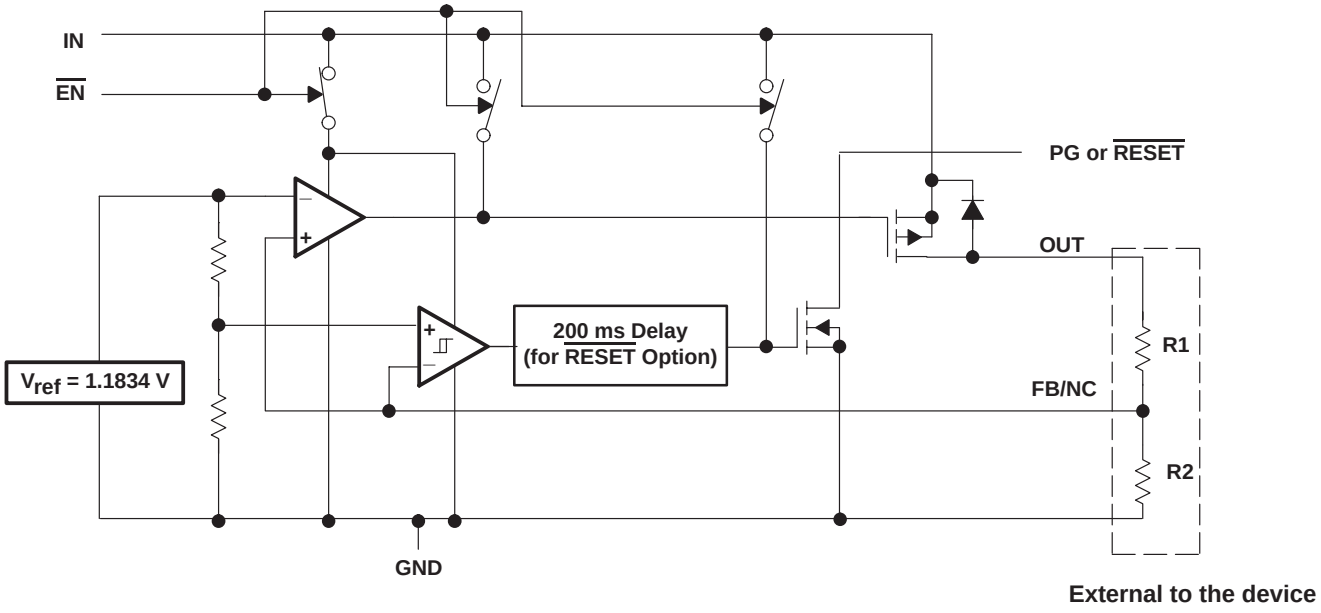
The TPS77x01 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS77701DR).



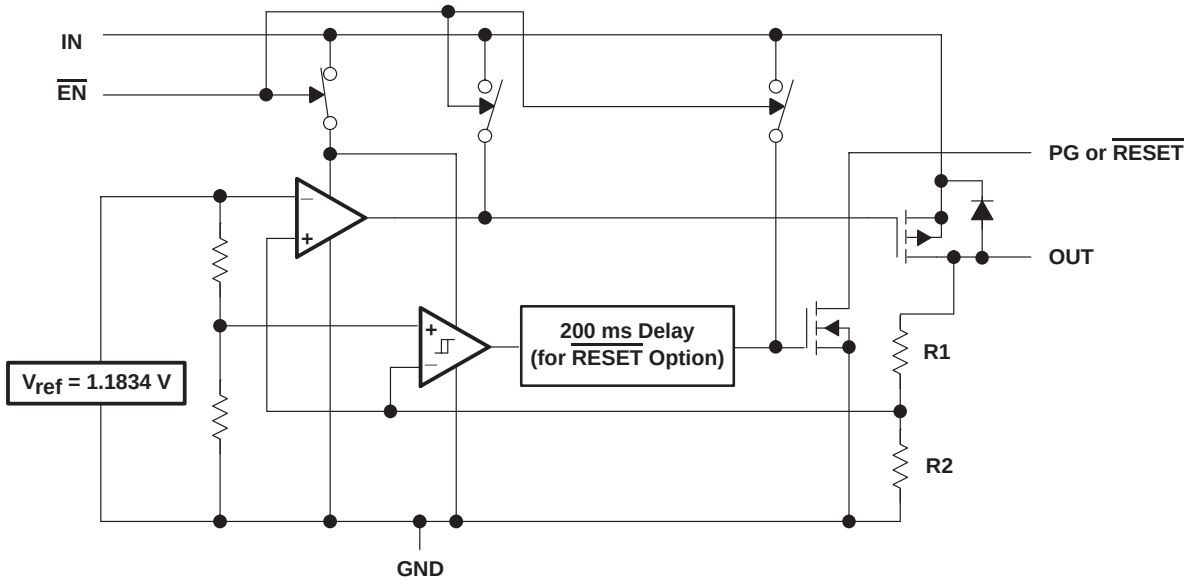
(1) See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



Terminal Functions

SOIC Package (TPS777xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
$\overline{\text{RESET}}$	8	O	$\overline{\text{RESET}}$ output

TSSOP Package (TPS777xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
$\overline{\text{RESET}}$	16	O	$\overline{\text{RESET}}$ output

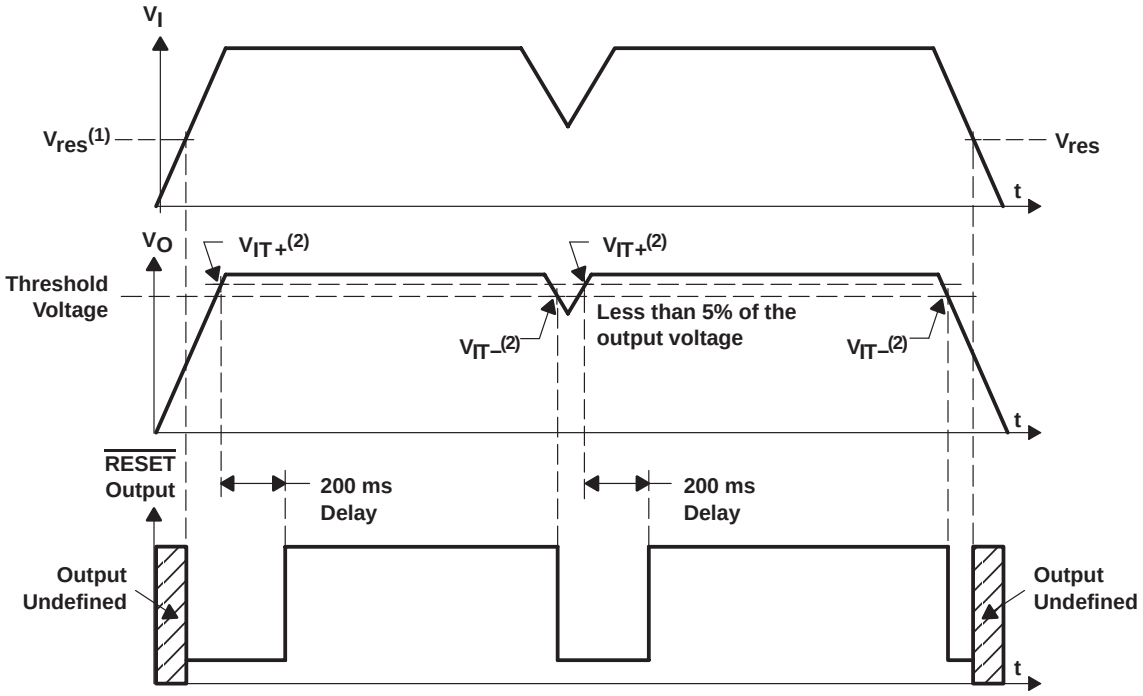
SOIC Package (TPS778xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
PG	8	O	PG output

TSSOP Package (TPS778xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	PG output

TPS777xx RESET timing diagram



(1) V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT} −Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)(1)

Input voltage range(2), V_I . . . . . −0.3 V to 13.5 V
Voltage range at $\overline{EN}$ . . . . . −0.3 V to 16.5 V
Maximum $\overline{RESET}$ voltage (TPS777xx) . . . . . 16.5 V
Maximum PG voltage (TPS778xx) . . . . . 16.5 V
Peak output current . . . . . Internally limited
Output voltage, V_O (OUT, FB) . . . . . 7 V
Continuous total power dissipation . . . . . See dissipation rating tables
Operating junction temperature range, T_J . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
ESD rating, HBM . . . . . 2 kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 − FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 − FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP§	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP¶	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

(1) This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5 in × 5 in PCB, 1 oz. copper, 2 in × 2 in coverage (4 in^2).
(2) This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5 in × 2 in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I(1)		2.7	10	V
Output voltage range, V_O	TPS77701	1.5	5.5	V
	TPS77801	1.2	5.5	
Operating junction temperature, T_J		−40	125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater.

electrical characteristics over recommended operating temperature range (TJ = −40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_o = 10 μF (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10 μA to 750 mA load)		TPS77701	1.5 V ≤ V_O ≤ 5.5 V,	T_J = 25°C		V_O		V
			1.5 V ≤ V_O ≤ 5.5 V,		0.98V_O		1.02V_O	
		TPS77801	1.2 V ≤ V_O ≤ 5.5 V,	T_J = 25°C		V_O		
			1.2 V ≤ V_O ≤ 5.5 V,		0.98V_O		1.02V_O	
		TPS77x15	T_J = 25°C,	2.7 V < V_{IN} < 10 V		1.5		
			T_J = −40°C to 125°C,	2.7 V < V_{IN} < 10 V	1.470		1.530	
		TPS77x18	T_J = 25°C,	2.8 V < V_{IN} < 10 V		1.8		
			T_J = −40°C to 125°C,	2.8 V < V_{IN} < 10 V	1.764		1.836	
		TPS77x25	T_J = 25°C,	3.5 V < V_{IN} < 10 V		2.5		
			T_J = −40°C to 125°C,	3.5 V < V_{IN} < 10 V	2.450		2.550	
		TPS77x33	T_J = 25°C,	4.3 V < V_{IN} < 10 V		3.3		
			T_J = −40°C to 125°C,	4.3 V < V_{IN} < 10 V	3.234		3.366	
Quiescent current (GND current)			10 μA < I_O < 750 mA,	T_J = 25°C		85		μA
			I_O = 750 mA				125	
Output voltage line regulation ($\Delta V_O/V_O$)			V_O + 1 V < V_I ≤ 10 V,	T_J = 25°C		0.01		%/V
Load regulation						3		mV
Output noise voltage (TPS77x18)			BW = 200 Hz to 100 kHz, C_o = 10 μF, T_J = 25°C, I_C = 750 μA			54		μVrms
Output current limit			V_O = 0 V		1.2	1.7	2	A
Thermal shutdown junction temperature						150		°C
Standby current			$\overline{EN}$ = V_I,	T_J = 25°C, 2.7 V < V_I < 10 V		1		μA
			$\overline{EN}$ = V_I,	2.7 V < V_I < 10 V			10	μA
FB input current		TPS77x01	FB = 1.5 V			2		nA
High level enable input voltage					1.7			V
Low level enable input voltage							0.9	V
Power supply ripple rejection			f = 1 KHz, T_J = 25°C	C_o = 10 μF,		60		dB
Reset (TPS777xx)	Minimum input voltage for valid $\overline{RESET}$		$I_{O(RESET)}$ = 300 μA			1.1		V
	Trip threshold voltage		V_O decreasing		92		98	%V_O
	Hysteresis voltage		Measured at V_O			0.5		%V_O
	Output low voltage		V_I = 2.7 V,	$I_{O(RESET)}$ = 1 mA		0.15	0.4	V
	Leakage current		$V_{(RESET)}$ = 5 V				1	μA
	RESET time-out delay					200		ms

electrical characteristics over recommended operating temperature range (TJ = −40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_o = 10 μF (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
PG (TPS778xx)	Minimum input voltage for valid PG		$I_{O(PG)}$ = 300 μA			1.1		V
	Trip threshold voltage		V_O decreasing		92		98	%V_O
	Hysteresis voltage		Measured at V_O			0.5		%V_O
	Output low voltage		V_I = 2.7 V,	$I_{O(PG)}$ = 1 mA		0.15	0.4	V
	Leakage current		$V_{(PG)}$ = 5 V				1	μA
Input current ($\overline{EN}$)			$\overline{EN}$ = 0 V		−1	0	1	μA
			$\overline{EN}$ = V_I		−1		1	
Dropout voltage (1)		TPS77733	I_O = 750 mA,	T_J = 25°C		260		mV
			I_O = 750 mA,				427	
		TPS77833	I_O = 750 mA,	T_J = 25°C		260		
			I_O = 750 mA,				427	

(1) IN voltage equals V_O(typ) − 100 mV; TPS77x01 output voltage set to 3.3 V nominal with external resistor divider. TPS77x15, TPS77x18, and TPS77x25 dropout voltage limited by input voltage range limitations (i.e., TPS77x33 input voltage needs to drop to 3.2 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output spectral noise density	vs Frequency	10
Z_o	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Input voltage	12
		vs Free-air temperature	13
	Input voltage (min)	vs Output voltage	14
	Line transient response		15, 17
	Load transient response		16, 18
V_O	Output voltage	vs Time	19
	Equivalent series resistance (ESR)	vs Output current	21 − 24

TYPICAL CHARACTERISTICS

TPS77x33
OUTPUT VOLTAGE vs OUTPUT CURRENT

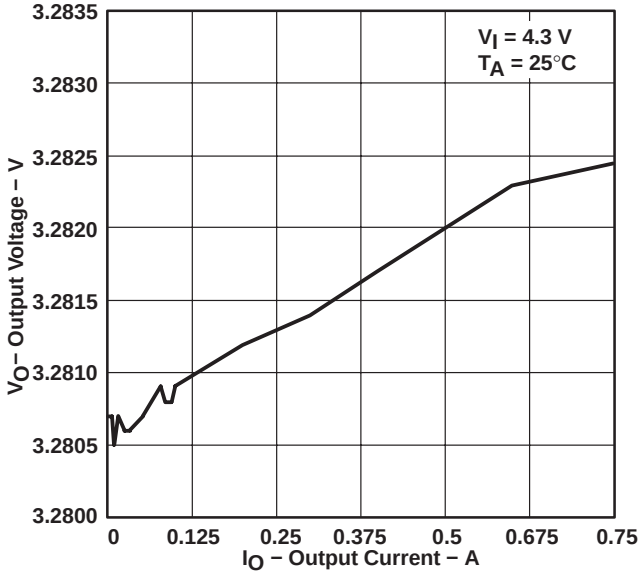


Figure 2

TPS77x15
OUTPUT VOLTAGE vs OUTPUT CURRENT

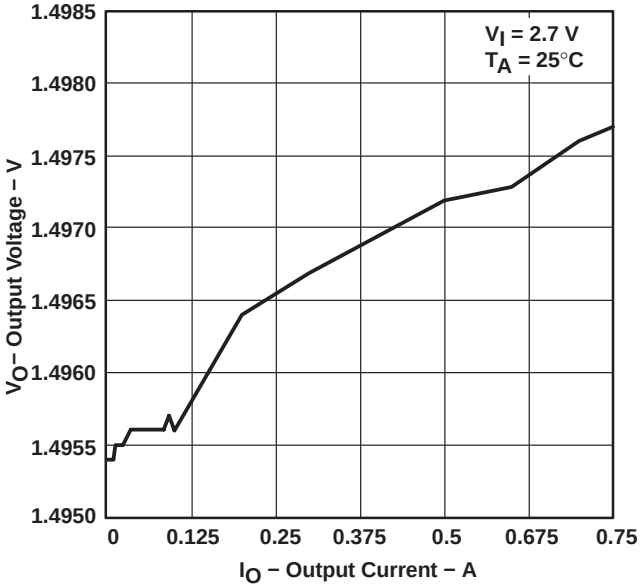


Figure 3

TPS77x25
OUTPUT VOLTAGE vs OUTPUT CURRENT

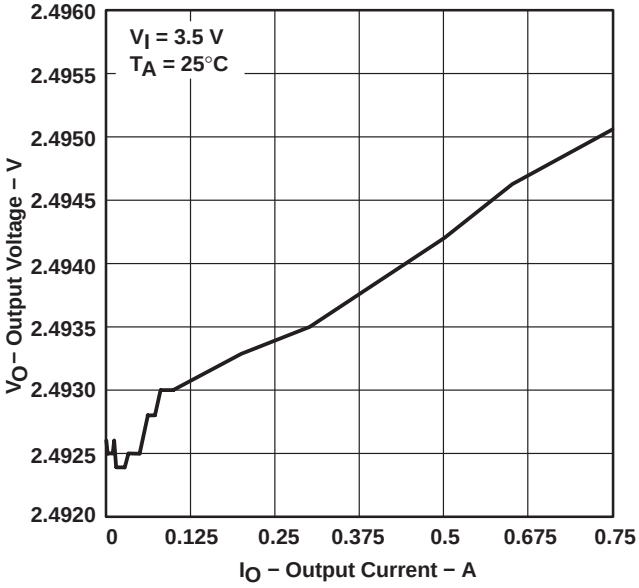


Figure 4

TPS77x33
OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

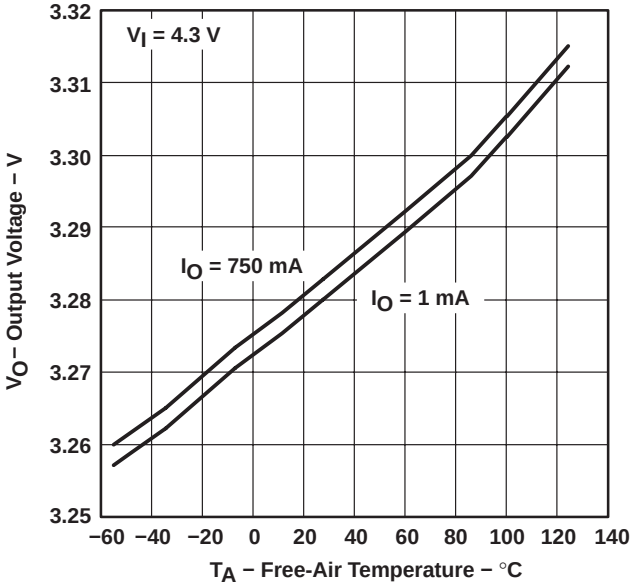


Figure 5

TYPICAL CHARACTERISTICS

TPS77x15
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

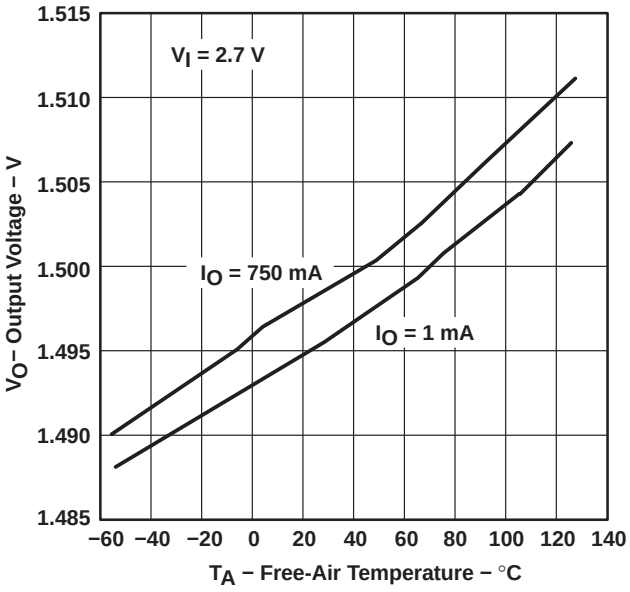


Figure 6

TPS77x25
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

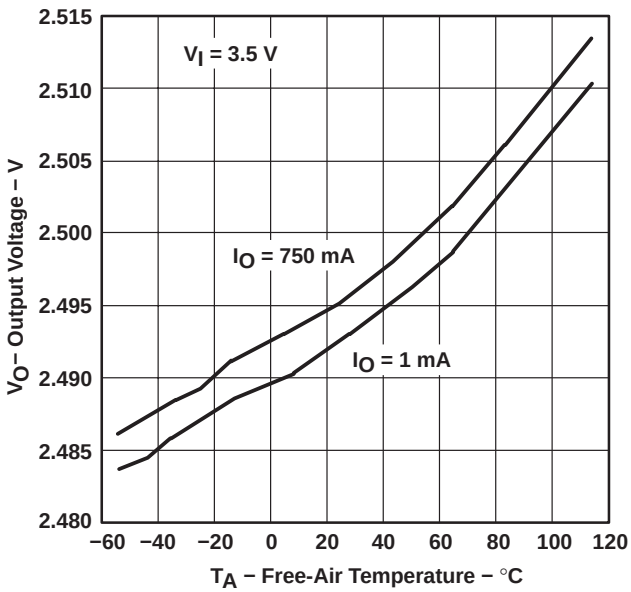


Figure 7

TPS77xxx
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

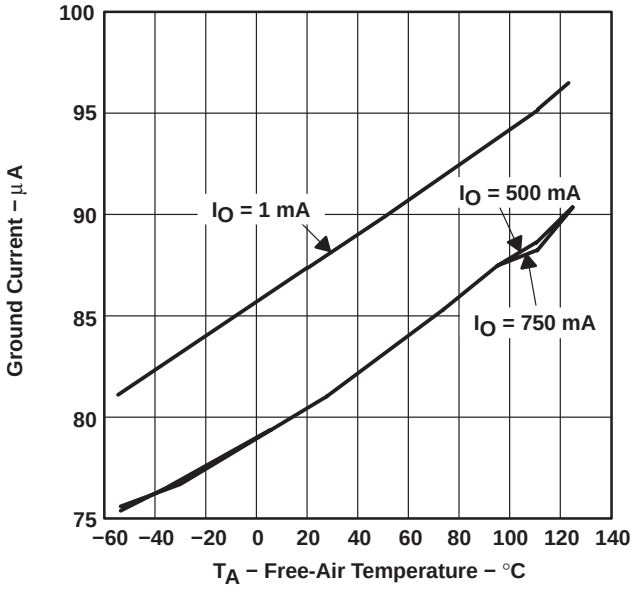


Figure 8

TPS77x33
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

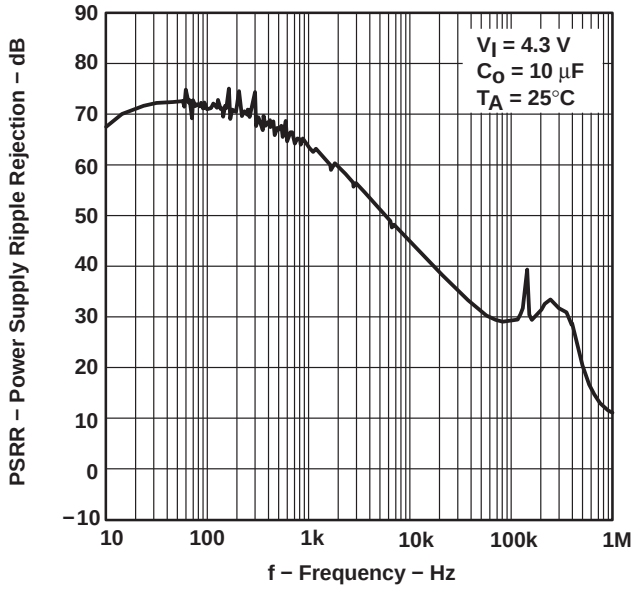


Figure 9

TYPICAL CHARACTERISTICS

TPS77x33
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

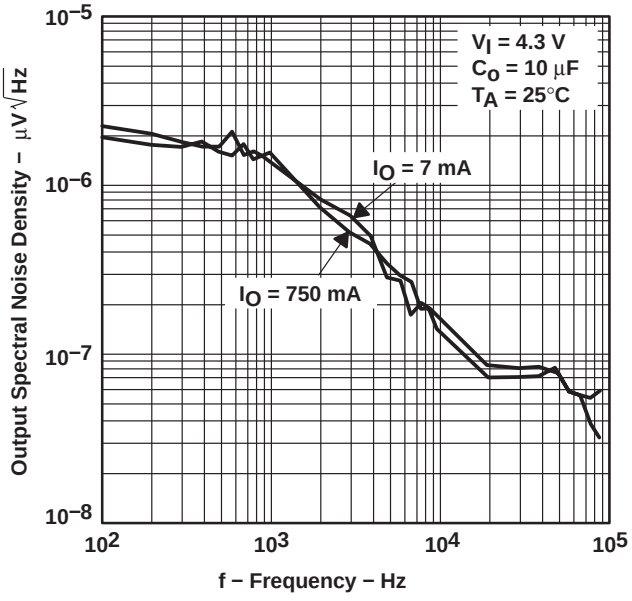


Figure 10

TPS77x33
OUTPUT IMPEDANCE
vs
FREQUENCY

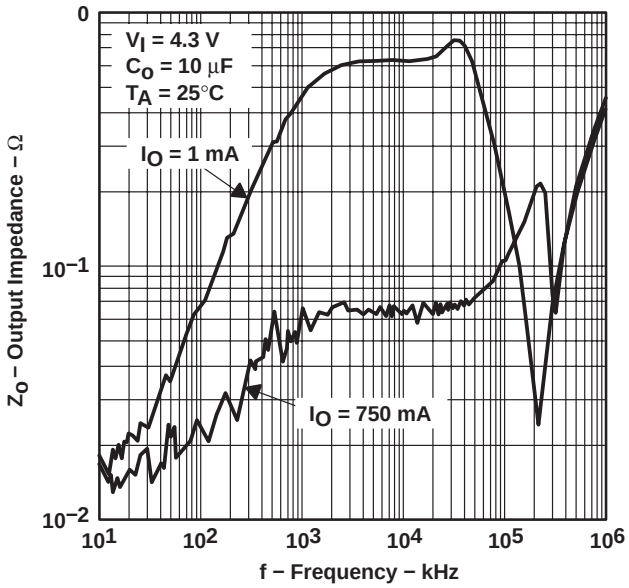


Figure 11

TPS77x01
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

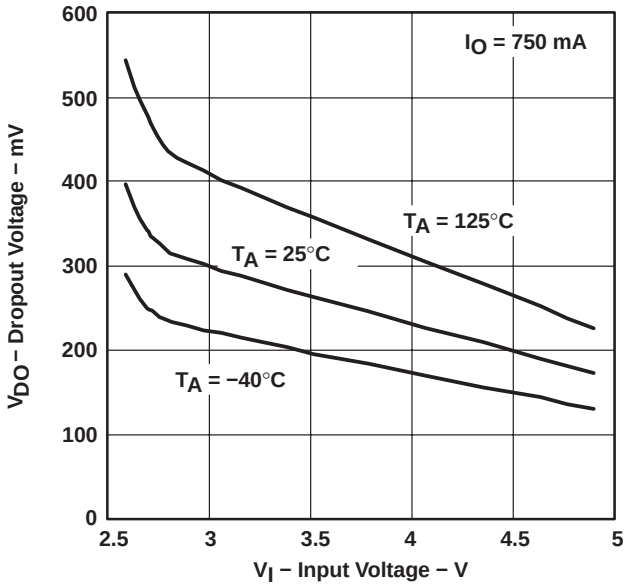


Figure 12

TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

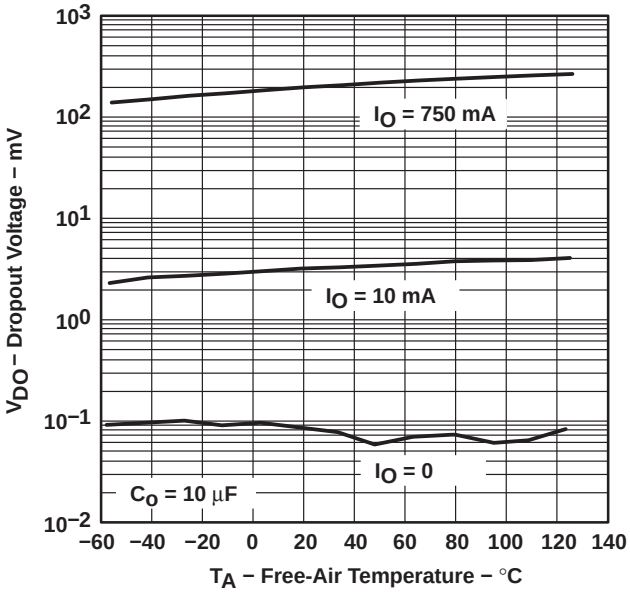


Figure 13

TYPICAL CHARACTERISTICS

**INPUT VOLTAGE (MIN)
vs
OUTPUT VOLTAGE**

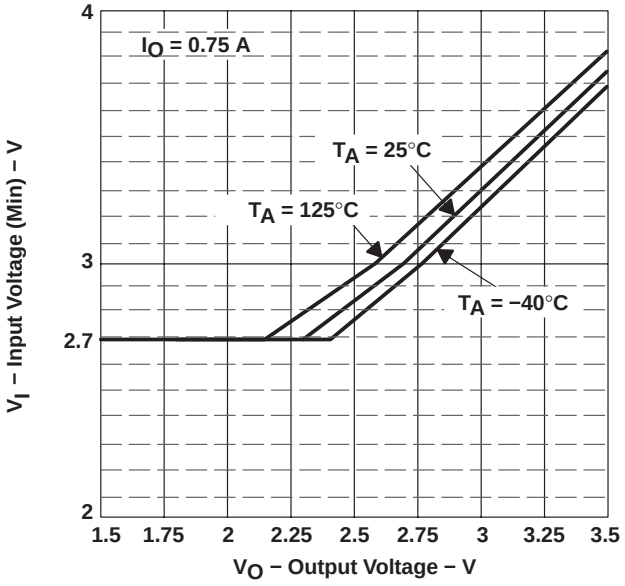


Figure 14

**TPS77x15
LINE TRANSIENT RESPONSE**

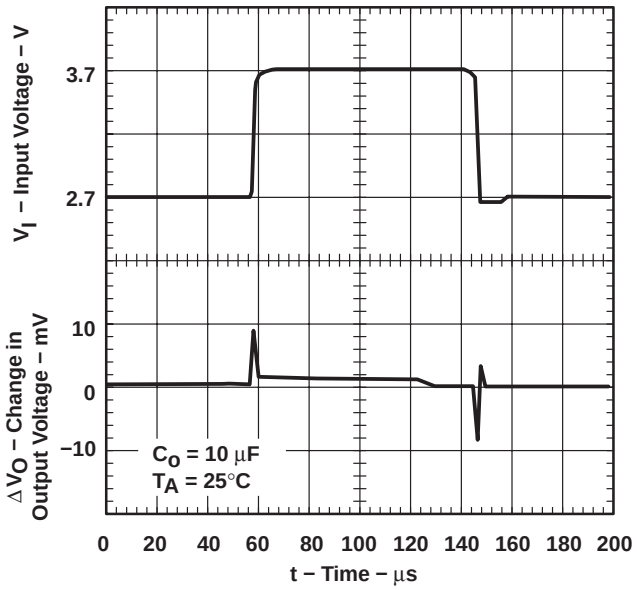


Figure 15

**TPS77x15
LOAD TRANSIENT RESPONSE**

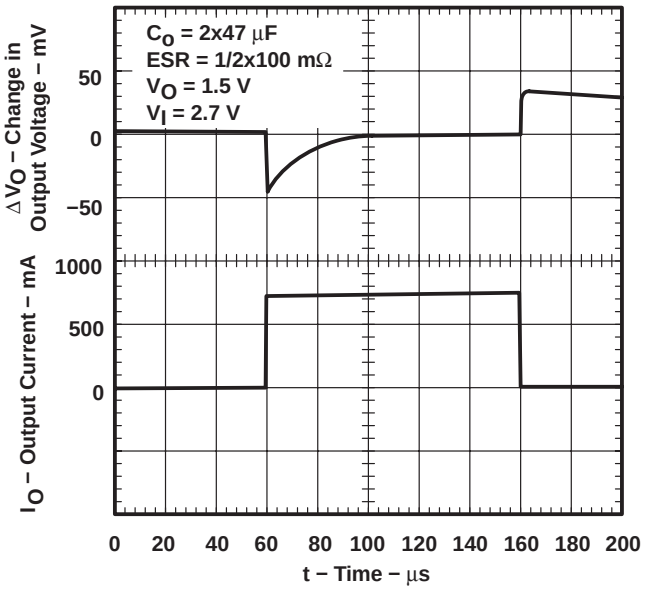


Figure 16

**TPS77x33
LINE TRANSIENT RESPONSE**

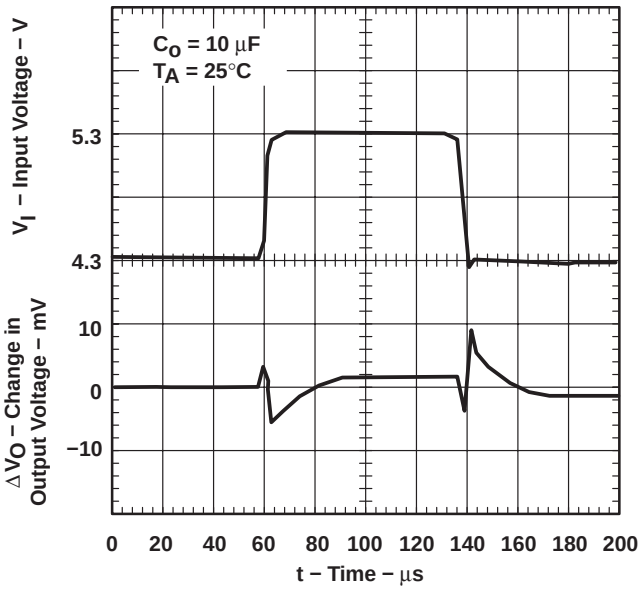


Figure 17

TYPICAL CHARACTERISTICS

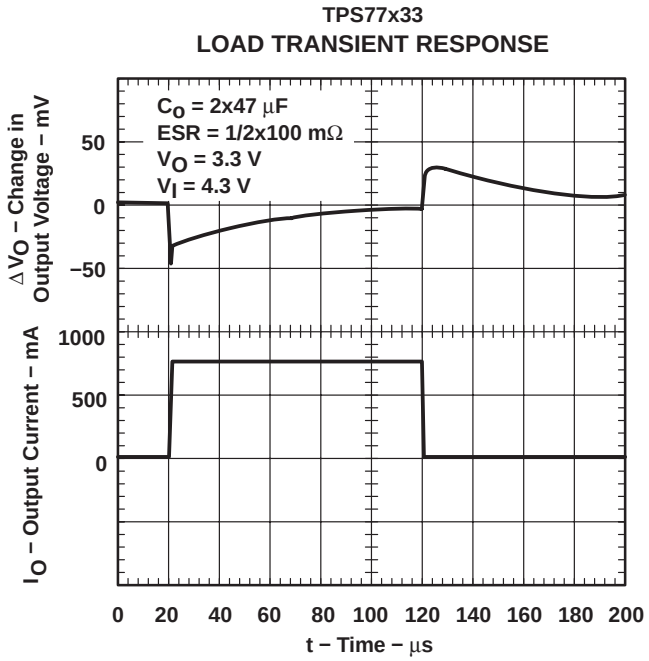


Figure 18

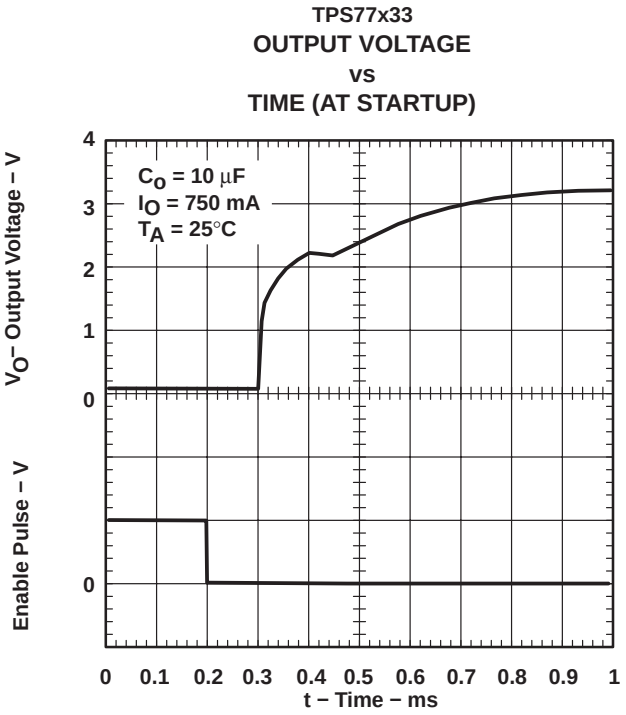


Figure 19

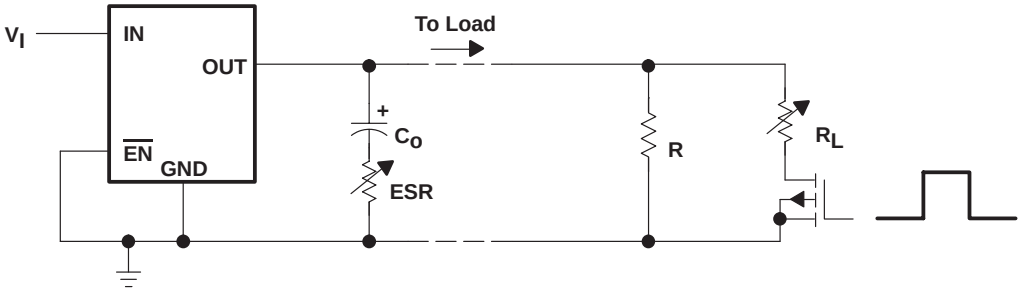


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

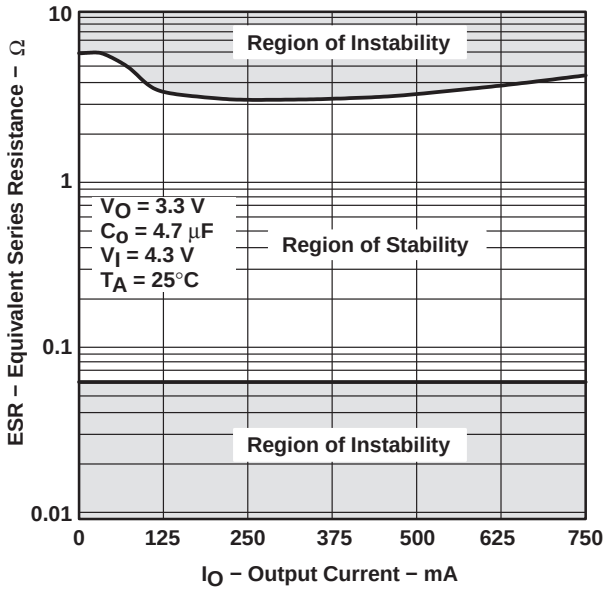


Figure 21

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

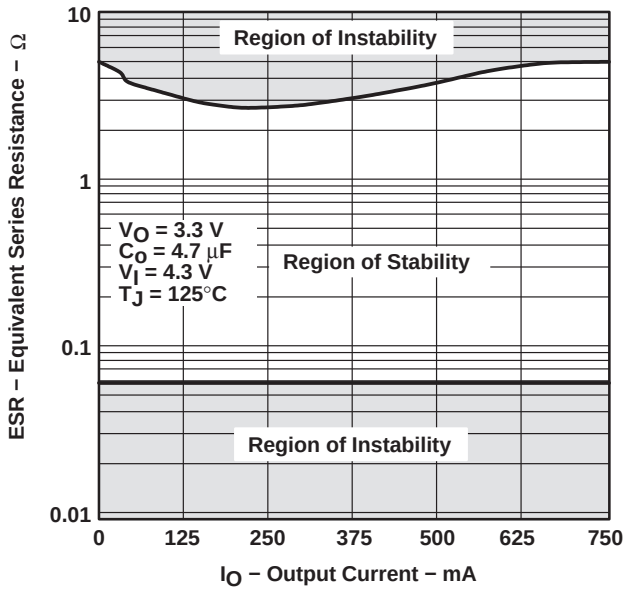


Figure 22

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

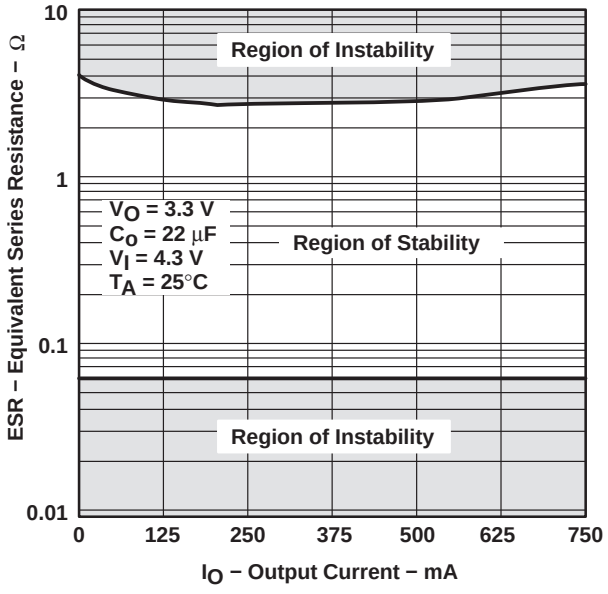


Figure 23

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

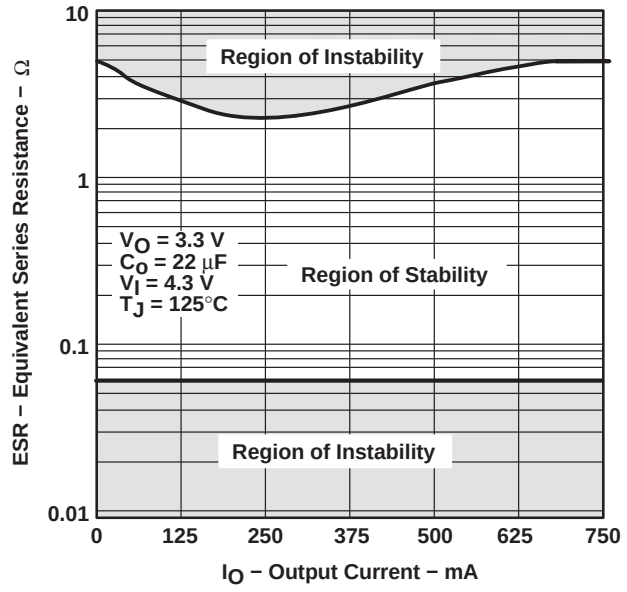


Figure 24

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS777xx and TPS778xx families include four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS77x01 (adjustable from 1.5 V to 5.5 V for TPS77701 option and 1.2 V to 5.5 V for TPS77801 option).

device operation

The TPS777xx and TPS778xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS777xx and TPS778xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS777xx and TPS778xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS777xx and TPS778xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

minimum load requirements

The TPS777xx and TPS778xx families are stable even at zero load; no minimum load is required for operation.

FB—pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option . The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS777xx or TPS778xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS777xx and TPS778xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF and the ESR (equivalent series resistance) must be between 50 mΩ and 1.5 Ω. Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

APPLICATION INFORMATION

external capacitor requirements (continued)

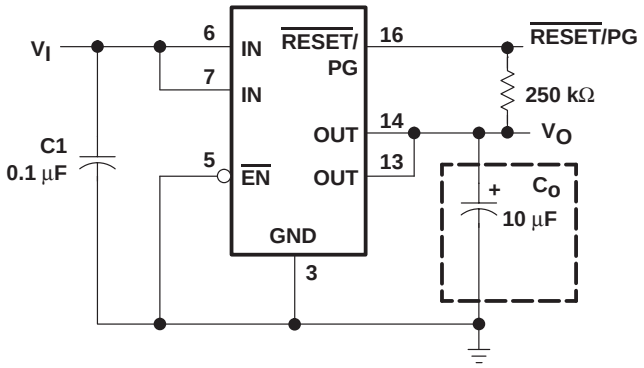


Figure 25. Typical Application Circuit (Fixed Versions)

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

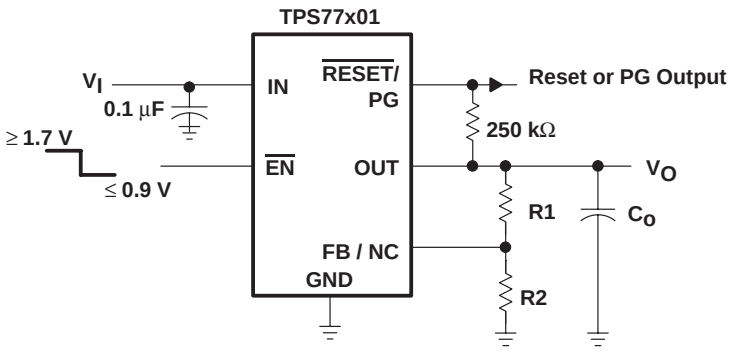
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 10-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 110 kΩ to set the divider current at approximately 10 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	121	110	kΩ
3.3 V	196	110	kΩ
3.6 V	226	110	kΩ
4.75 V	332	110	kΩ

Figure 26. TPS77x01 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

reset indicator

The TPS777xx features a RESET output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the RESET output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. RESET can be used to drive power-on reset circuitry or as a low-battery indicator. RESET does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

power-good indicator

The TPS778xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS777xx and TPS778xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS777xx and TPS778xx also feature internal current limiting and thermal protection. During normal operation, the TPS777xx and TPS778xx limit output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

APPLICATION INFORMATION

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, and is calculated as $\frac{1}{\text{derating factor}}$ from the dissipation rating tables.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS77701D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77701
TPS77701D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77701
TPS77701DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77701
TPS77701DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77701
TPS77701PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77701
TPS77701PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77701
TPS77701PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77701
TPS77701PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77701
TPS77715D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77715
TPS77715D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77715
TPS77715DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77715
TPS77715DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77715
TPS77715PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77715
TPS77715PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77715
TPS77715PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77715
TPS77718D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77718
TPS77718D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77718
TPS77718DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77718
TPS77718DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77718
TPS77718PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77718
TPS77718PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77718
TPS77718PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77718
TPS77718PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77718
TPS77718PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77718
TPS77725D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77725
TPS77725D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77725
TPS77725PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77725
TPS77725PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77725
TPS77725PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77725

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS77725PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77725
TPS77733D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77733
TPS77733D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77733
TPS77733DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77733
TPS77733DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77733
TPS77733PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77733
TPS77733PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77733
TPS77733PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77733
TPS77733PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77733
TPS77801D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77801
TPS77801D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77801
TPS77801DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77801
TPS77801DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77801
TPS77801DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77801
TPS77801PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77801
TPS77801PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77801
TPS77801PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77801
TPS77801PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77801
TPS77801PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77801
TPS77801PWPRG4	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77801
TPS77815D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77815
TPS77815D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77815
TPS77815DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77815
TPS77815DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77815
TPS77815PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77815
TPS77815PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77815
TPS77815PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77815
TPS77815PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77815
TPS77815PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77815
TPS77818D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77818
TPS77818D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77818

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS77818PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77818
TPS77818PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77818
TPS77818PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77818
TPS77818PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77818
TPS77818PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77818
TPS77825D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77825
TPS77825D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77825
TPS77825DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77825
TPS77825DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77825
TPS77825PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77825
TPS77825PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77825
TPS77825PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77825
TPS77825PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77825
TPS77833D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77833
TPS77833D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77833
TPS77833DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77833
TPS77833DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77833
TPS77833PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77833
TPS77833PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77833
TPS77833PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77833
TPS77833PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77833

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

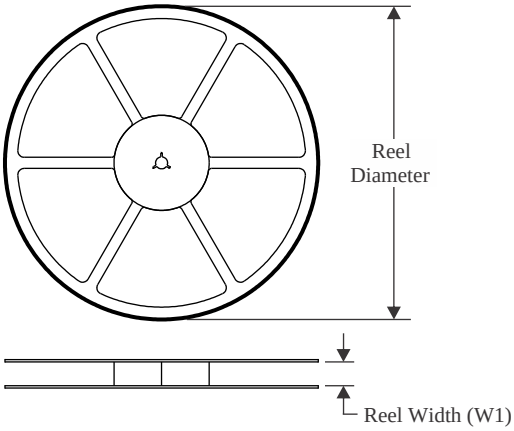
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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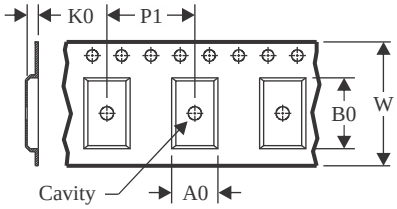
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

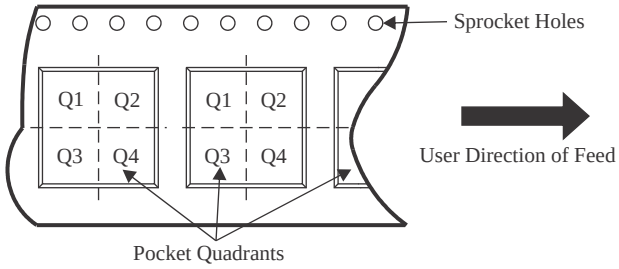


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

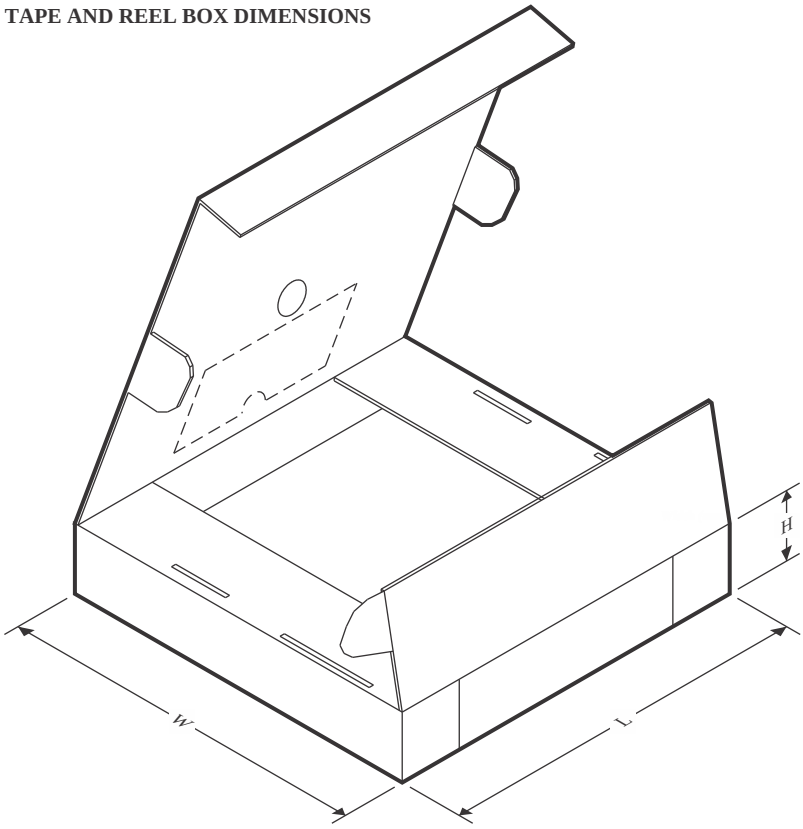


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77701DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77701PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TPS77715DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77718DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77718PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77725PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77733DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77733PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77801DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77801PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77815DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77815PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77818PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77825DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77825PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77833PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

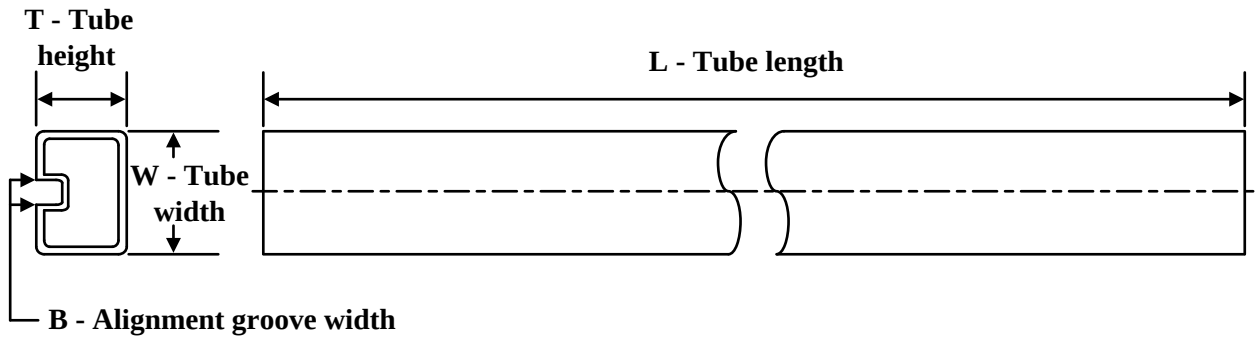
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77701DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77701PWPR	HTSSOP	PWP	20	2000	353.0	353.0	32.0
TPS77715DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77718DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77718PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77725PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77733DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77733PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77801DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77801PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77815DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77815PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77818PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77825DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77825PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77833DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77833PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS77701D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77701D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77701PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77701PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77715D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77715D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77715PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77715PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77715PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77718D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77718D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77718PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77718PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77718PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77725D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77725D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77725PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77725PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77733D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77733D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77733PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77733PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77801D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77801D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77801DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS77801PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77801PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77801PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77815D	D	SOIC	8	75	505.46	6.76	3810	4

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS77815D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77815PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77815PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77815PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77818D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77818D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77818PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77818PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77818PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77825D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77825D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77825PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77825PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77833D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77833D.A	D	SOIC	8	75	505.46	6.76	3810	4
TPS77833PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77833PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5

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