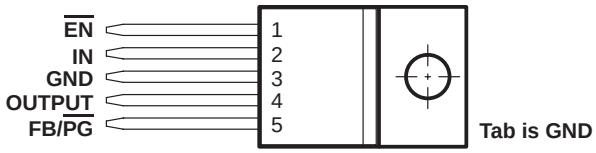
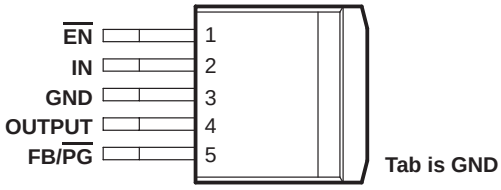
- 5-A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, and 3.3-V Fixed-Output and Adjustable Versions
- Open Drain Power-Good ($\overline{PG}$) Status Output (Fixed Options Only)
- Dropout Voltage Typically 250 mV at 5 A (TPS75533)
- Low 125 μA Typical Quiescent Current
- Fast Transient Response
- 3% Tolerance Over Specified Conditions for Fixed-Output Versions
- Available in 5-Pin TO−220 and TO−263 Surface-Mount Packages
- Thermal Shutdown Protection

TO−220 (KC) PACKAGE
(TOP VIEW)



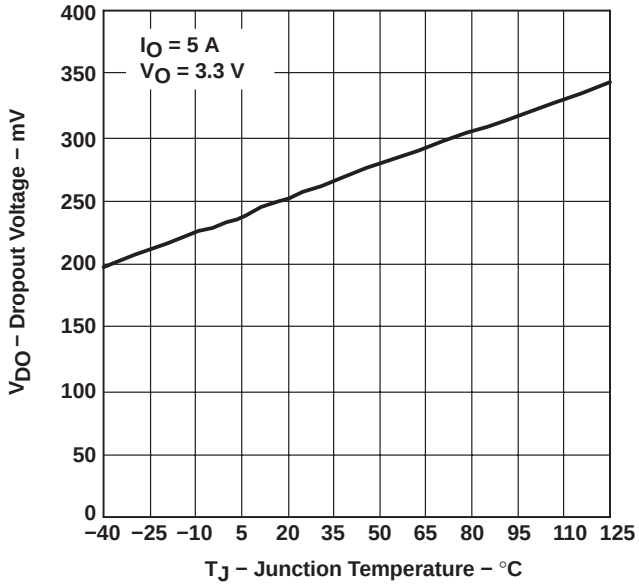
TO−263 (KTT) PACKAGE
(TOP VIEW)



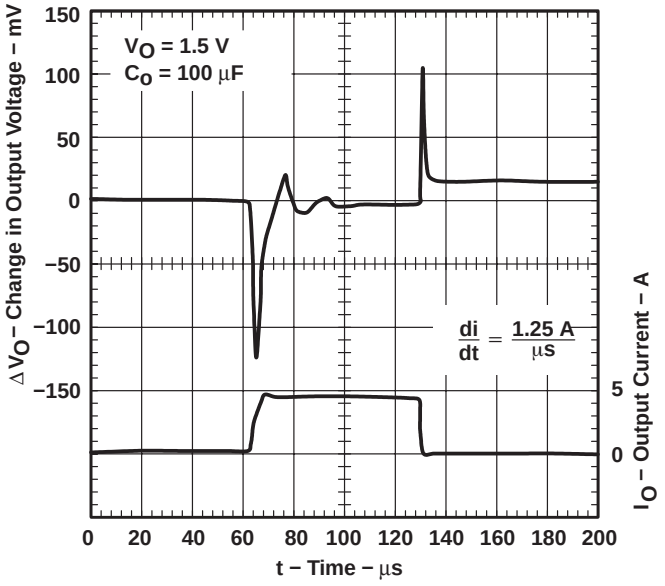
description

The TPS755xx family of 5-A low dropout (LDO) regulators contains four fixed voltage option regulators with integrated power-good ($\overline{PG}$) and an adjustable voltage option regulator. These devices are capable of supplying 5 A of output current with a dropout of 250 mV (TPS75533). Therefore, the device is capable of performing a 3.3-V to 2.5-V conversion. Quiescent current is 125 μA at full load and drops down to less than 1 μA when the device is disabled. The TPS755xx is designed to have fast transient response for large load current changes.

TPS75533
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



TPS75515
LOAD TRANSIENT RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 250 mV at an output current of 5 A for the TPS75533) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 125 μA over the full range of output current). These two key specifications yield a significant improvement in operating life for battery-powered systems.

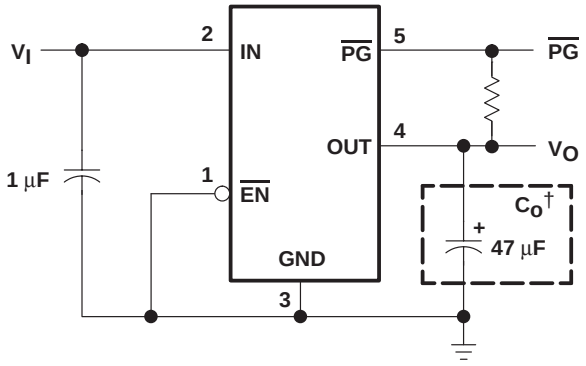
The device is enabled when $\overline{EN}$ is connected to a low-level voltage. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μA at T_J = 25°C. The power-good terminal ($\overline{PG}$) is an active low, open drain output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS755xx is offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.22 V to 5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS755xx family is available in a 5-pin TO−220 (KC) and TO−263 (KTT) packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (TYP)	TO−220 (KC)	TO−263(KTT)
−40°C to 125°C	3.3 V	TPS75533KC	TPS75533KTT
	2.5 V	TPS75525KC	TPS75525KTT
	1.8 V	TPS75518KC	TPS75518KTT
	1.5 V	TPS75515KC	TPS75515KTT
	Adjustable 1.22 V to 5 V	TPS75501KC	TPS75501KTT

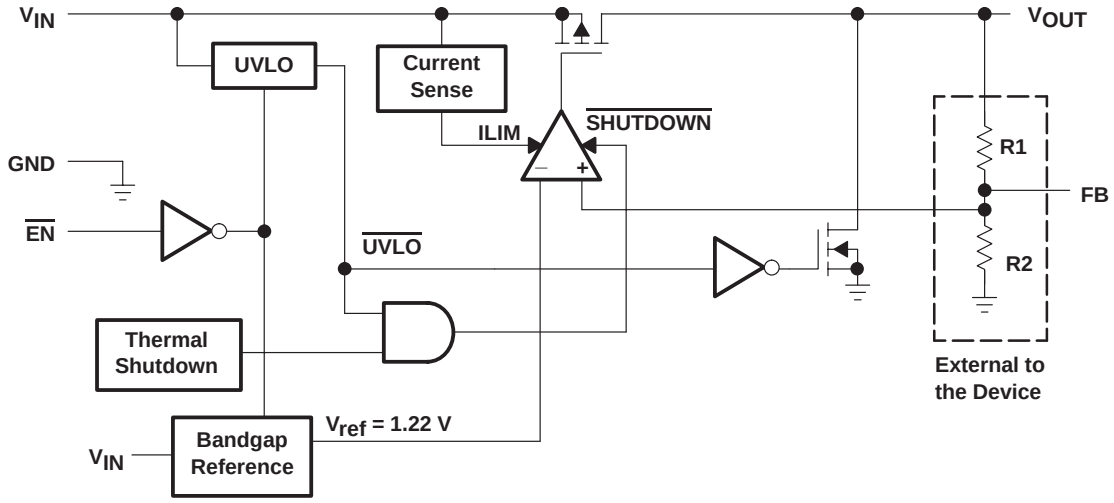
NOTE: The TPS75501 is programmable using an external resistor divider (see application information). The KTT package is available taped and reeled. Add an R suffix to the device type (e.g., TPS75501KTTR) to indicate tape and reel.



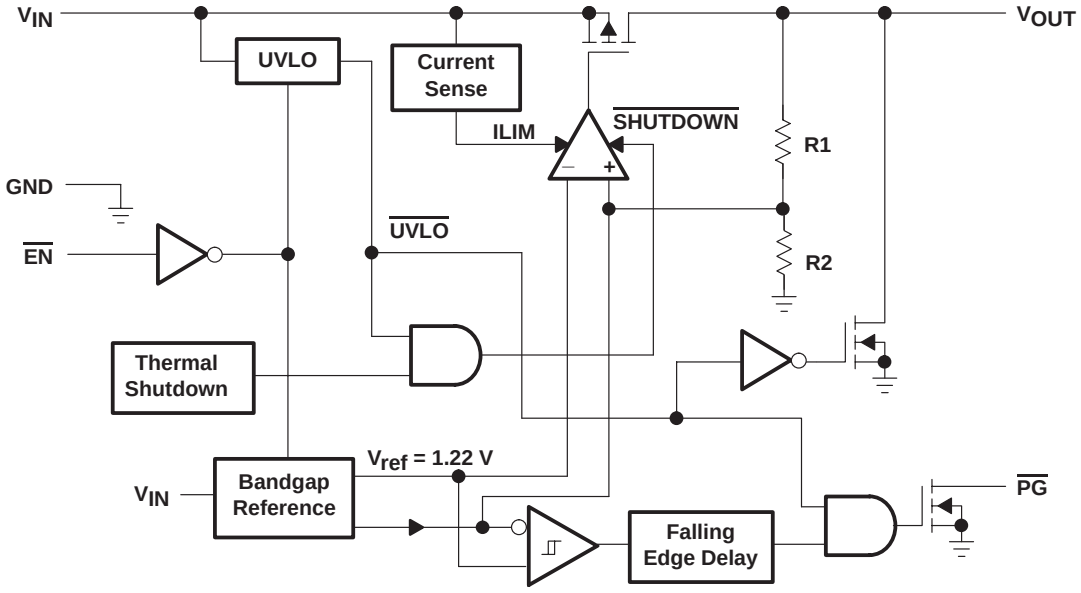
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (For Fixed Output Options)

functional block diagram—adjustable version



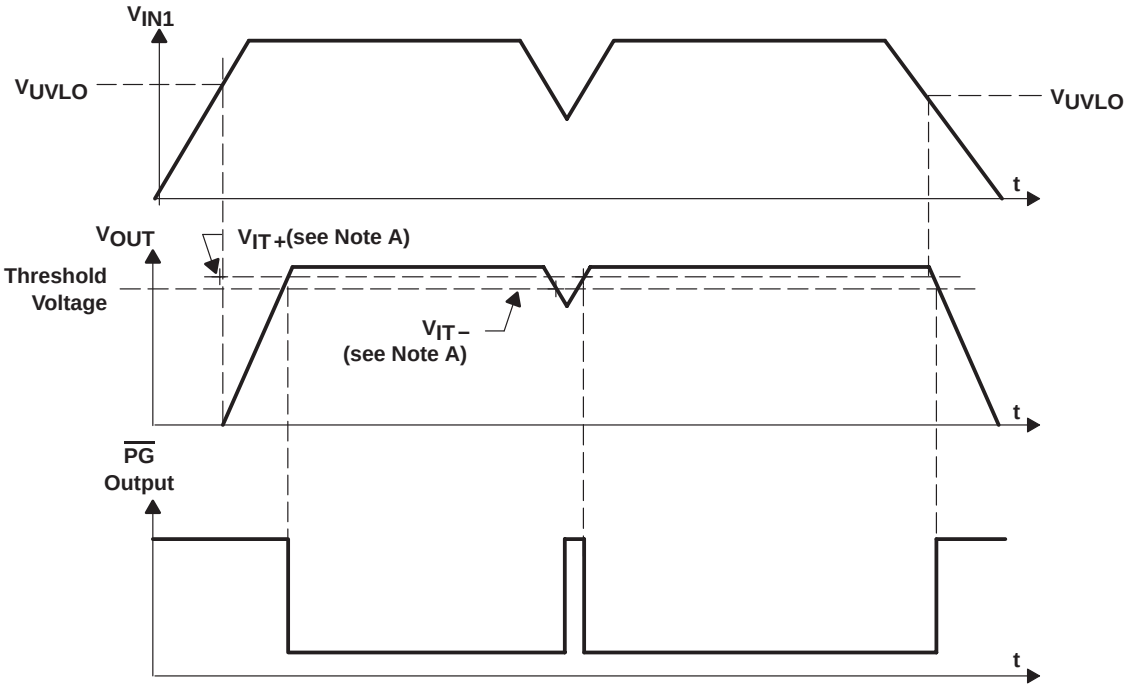
functional block diagram—fixed version



Terminal Functions (TPS755xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	1	I	Enable input
FB/$\overline{PG}$	5	I	Feedback input voltage for adjustable device/$\overline{PG}$ output for fixed options
GND	3		Regulator ground
IN	2	I	Input voltage
OUTPUT	4	O	Regulated output voltage

TPS755xx $\overline{PG}$ timing diagram



NOTE A: V_{IT} −Trip voltage is typically 9% lower than the output voltage (91%V_O). V_{IT-} to V_{IT+} is the hysteresis voltage.

detailed description

The TPS755xx family includes four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS75501 (adjustable from 1.22 V to 5 V). The bandgap voltage is typically 1.22 V.

pin functions

enable ($\overline{EN}$)

The $\overline{EN}$ terminal is an input which enables or shuts down the device. If $\overline{EN}$ is a logic high, the device will be in shutdown mode. When $\overline{EN}$ goes to logic low, the device will be enabled.

power-good ($\overline{PG}$)

The $\overline{PG}$ terminal for the fixed voltage option devices is an open drain, active low output that indicates the status of V_O (output of the LDO). When V_O reaches approximately 91% of the regulated voltage, $\overline{PG}$ will go to a low impedance state. It will go to a high-impedance state when V_O falls below approximately 89% (i.e. over load condition) of the regulated voltage. The open drain output of the $\overline{PG}$ terminal requires a pullup resistor.

feedback (FB)

FB is an input terminal used for the adjustable-output option and must be connected to the output terminal either directly, in order to generate the minimum output voltage of 1.22 V, or through an external feedback resistor divider for other output voltages. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

detailed description (continued)

input voltage (IN)

The V_{IN} terminal is an input to the regulator.

output voltage (OUTPUT)

The V_{OUTPUT} terminal is an output to the regulator.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . . . −0.3 V to 6 V
Voltage range at $\overline{EN}$ . . . . . −0.3 V to 6 V
Maximum $\overline{PG}$ voltage (fixed options only) . . . . . 6 V
Peak output current . . . . . Internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Tables
Output voltage, V_O (OUTPUT, FB) . . . . . 5.5 V
Operating junction temperature range, T_J . . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
ESD rating, HBM . . . . . 2 kV
ESD rating, CDM . . . . . 500 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)§
TO−220	2	58.7¶
TO−263	2	38.7#

§ For both packages, the $R_{\theta JA}$ values were computed using JEDEC high K board (2S2P) with 1 ounce internal copper plane and ground plane. There was no air flow across the packages.
¶ $R_{\theta JA}$ was computed assuming a vertical, free standing TO-220 package with pins soldered to the board. There is no heatsink attached to the package.
# $R_{\theta JA}$ was computed assuming a horizontally mounted TO-263 package with pins soldered to the board. There is no copper pad underneath the package.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I‖	2.8	5.5	V
Output voltage range, V_O	1.22	5	V
Output current, I_O	0	5	A
Operating virtual junction temperature, T_J	−40	125	°C

‖ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

electrical characteristics over recommended operating junction temperature range (T_J = −40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 100 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (see Note 2)	Adjustable voltage	1.22 V ≤ V_O ≤ 5.5 V,	T_J = 25°C		V_O		V
		1.22 V ≤ V_O ≤ 5.5 V		0.97 V_O		1.03 V_O	
		1.22 V ≤ V_O ≤ 5.5 V, (see Note 1)	T_J = 0 to 125°C	0.98 V_O		1.02 V_O	
	1.5 V Output	T_J = 25°C,	2.8 V < V_I < 5.5 V		1.5		V
		2.8 V ≤ V_I ≤ 5.5 V		1.455		1.545	
	1.8 V Output	T_J = 25°C,	2.8 V < V_I < 5.5 V		1.8		V
		2.8 V ≤ V_I ≤ 5.5 V		1.746		1.854	
	2.5 V Output	T_J = 25°C,	3.5 V < V_I < 5.5 V		2.5		V
		3.5 V ≤ V_I ≤ 5.5 V		2.425		2.575	
	3.3 V Output	T_J = 25°C,	4.3 V < V_I < 5.5 V		3.3		V
		4.3 V ≤ V_I ≤ 5.5 V		3.201		3.399	
Quiescent current (GND current) (see Notes 2 and 3)		T_J = 25°C			125		μA
						200	
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 3)		V_O + 1 V ≤ V_I ≤ 5.5 V,	T_J = 25°C		0.04		%/V
		V_O + 1 V ≤ V_I < 5.5 V				0.1	
Load regulation (see Note 2)					0.35		%/V
Output noise voltage	TPS75515	BW = 300 Hz to 50 kHz, T_J = 25°C, V_I = 2.8 V			35		μVrms
Output current limit		V_O = 0 V		5.5	10	14	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I,	T_J = 25°C		0.1		μA
		$\overline{EN}$ = V_I				10	μA
FB input current	TPS75501	FB = 1.5 V		−1		1	μA
Power supply ripple rejection	TPS75515	f = 100 Hz, V_I = 2.8 V,	T_J = 25°C, I_O = 5 A		60		dB
Minimum input voltage for valid $\overline{PG}$		$I_{O(PG)}$ = 300 μA,	$V_{(PG)}$ ≤ 0.8 V		0		V
$\overline{PG}$ trip threshold voltage	Fixed options only	V_O decreasing		89		93	$\%V_O$
$\overline{PG}$ hysteresis voltage	Fixed options only	Measured at V_O			0.5		$\%V_O$
$\overline{PG}$ output low voltage	Fixed options only	V_I = 2.8 V,	$I_{O(PG)}$ = 1 mA		0.15	0.4	V
$\overline{PG}$ leakage current	Fixed options only	$V_{(PG)}$ = 5 V				1	μA

NOTES: 1. The adjustable option operates with a 2% tolerance over T_J = 0 to 125 °C.
2. I_O = 1 mA to 5 A
3. If $V_O \leq$ 2.5 V then V_{Imin} = 2.8 V, V_{Imax} = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.8\ V\right)}{100} \times 1000$$

If V_O > 2.5 V then $V_{Imin} = V_O$ + 1 V, V_{Imax} = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

electrical characteristics over recommended operating junction temperature range (T_J = −40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 100 μF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Input current ($\overline{EN}$)		$\overline{EN} = V_I$			−1		1	μA
		$\overline{EN}$ = 0 V			−1	0	1	μA
High level $\overline{EN}$ input voltage					2			V
Low level $\overline{EN}$ input voltage							0.7	V
V_O	Dropout voltage, (3.3 V output) (see Note 4)	I_O = 5 A,	V_I = 3.2 V,	T_J = 25°C		250		mV
		I_O = 5 A,	V_I = 3.2 V				500	mV
	Discharge transistor current	V_O = 1.5 V,	T_J = 25°C		10	25		mA
V_I	UVLO	T_J = 25°C,	V_I rising		2.2		2.75	V
	UVLO hysteresis	T_J = 25°C,	V_I falling			100		mV

NOTE 4: IN voltage equals V_O(typ) − 100 mV; TPS75515, TPS75518, and TPS75525 dropout voltage limited by input voltage range limitations (i.e., TPS75533 input voltage is set to 3.2 V for the purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3
		vs Junction temperature	4, 5
	Ground current	vs Junction temperature	6
	Power supply ripple rejection	vs Frequency	7
	Output spectral noise density	vs Frequency	8
z_o	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Input voltage	10
		vs Junction temperature	11
V_I	Minimum required input voltage	vs Output voltage	12
	Line transient response		13, 15
	Load transient response		14, 16
V_O	Output voltage and enable voltage	vs Time (start-up)	17
	Equivalent series resistance	vs Output current	19, 20

TYPICAL CHARACTERISTICS

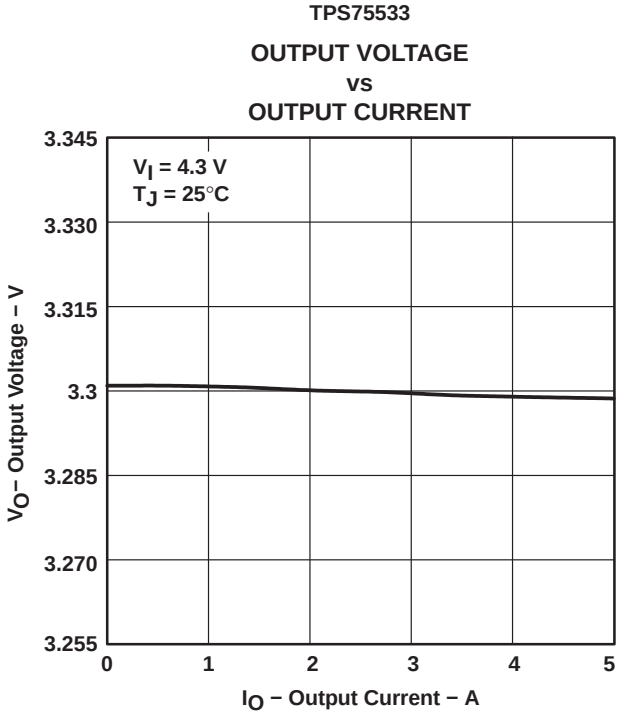


Figure 2

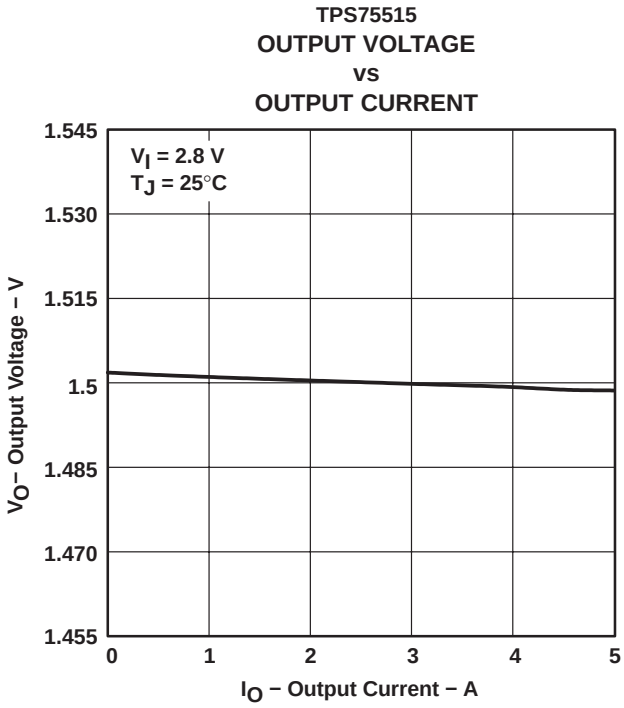


Figure 3

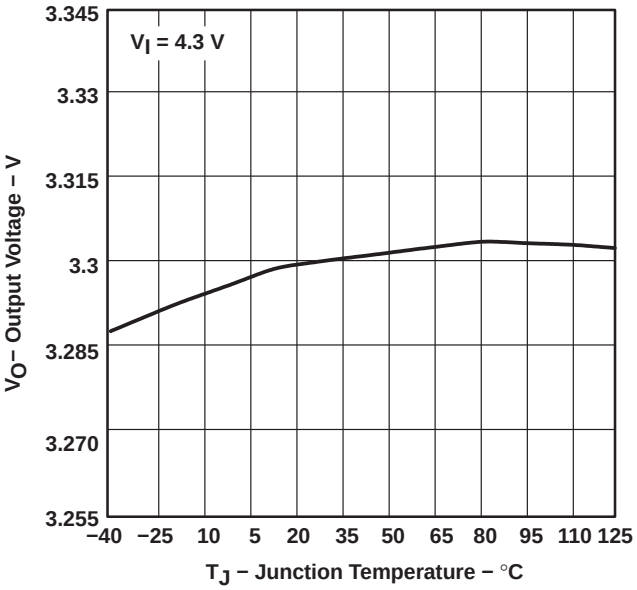


Figure 4

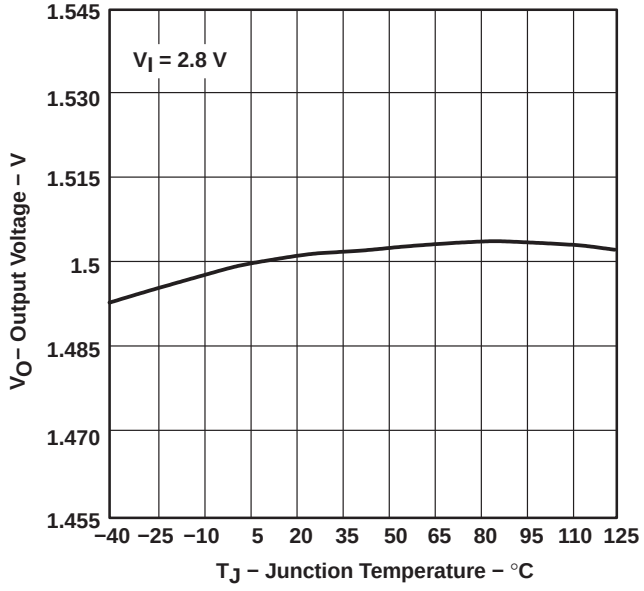


Figure 5

TYPICAL CHARACTERISTICS

TPS755xx
GROUND CURRENT
vs
JUNCTION TEMPERATURE

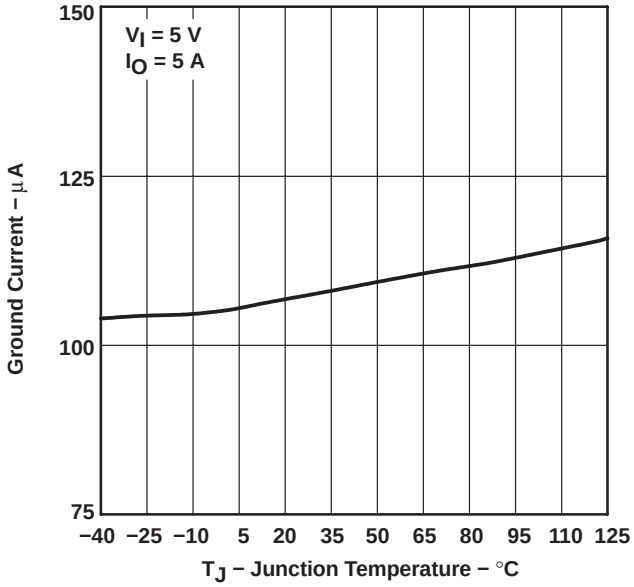


Figure 6

TPS75733
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

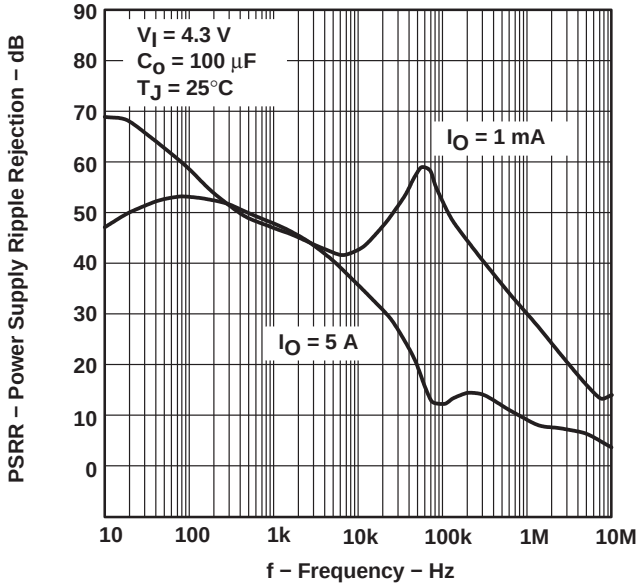


Figure 7

TPS75533
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

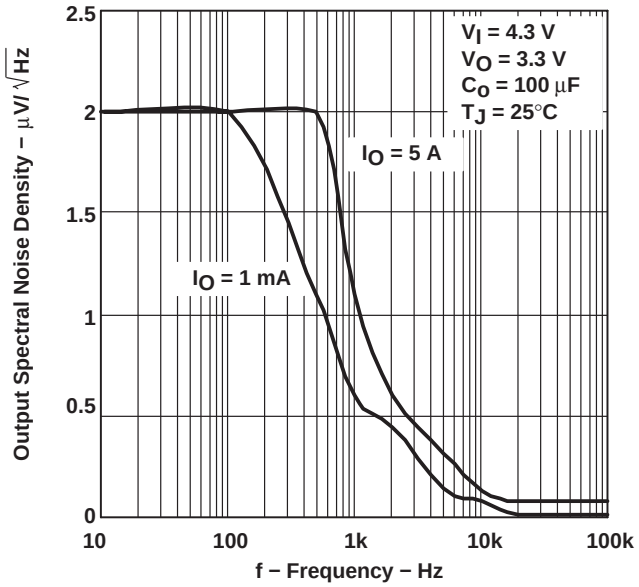


Figure 8

TPS75533
OUTPUT IMPEDANCE
vs
FREQUENCY

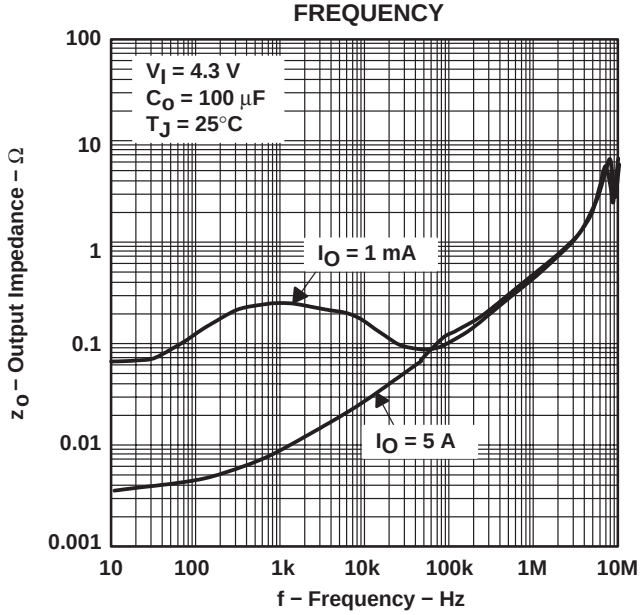


Figure 9

TYPICAL CHARACTERISTICS

TPS75501
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

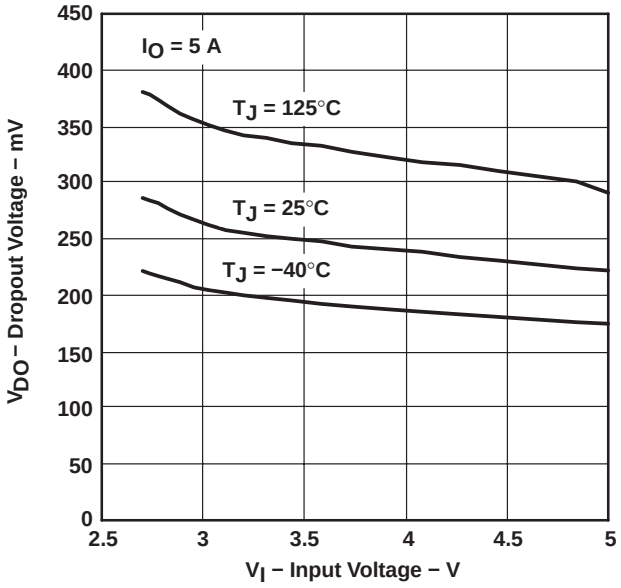


Figure 10

TPS75533
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

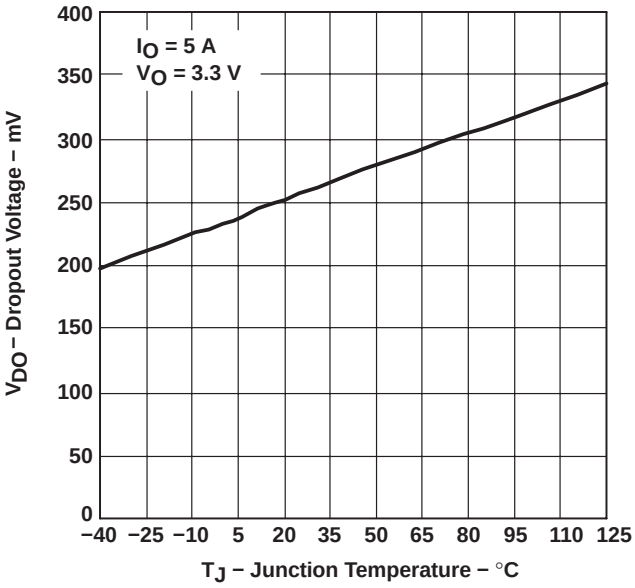


Figure 11

MINIMUM REQUIRED INPUT VOLTAGE
vs
OUTPUT VOLTAGE

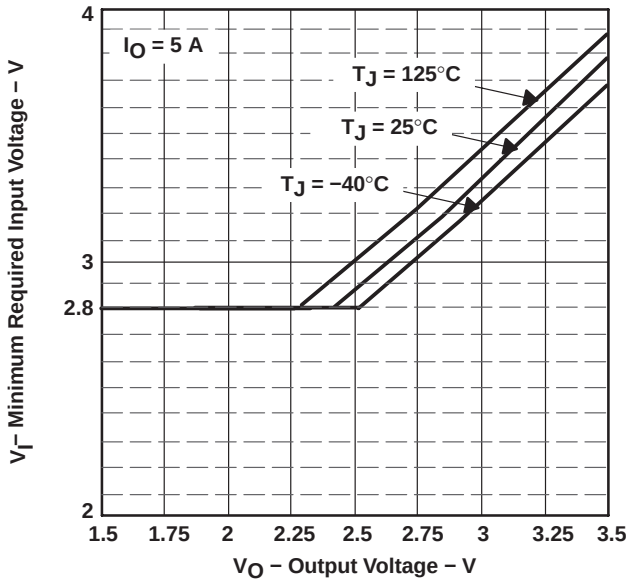


Figure 12

TPS75515
LINE TRANSIENT RESPONSE

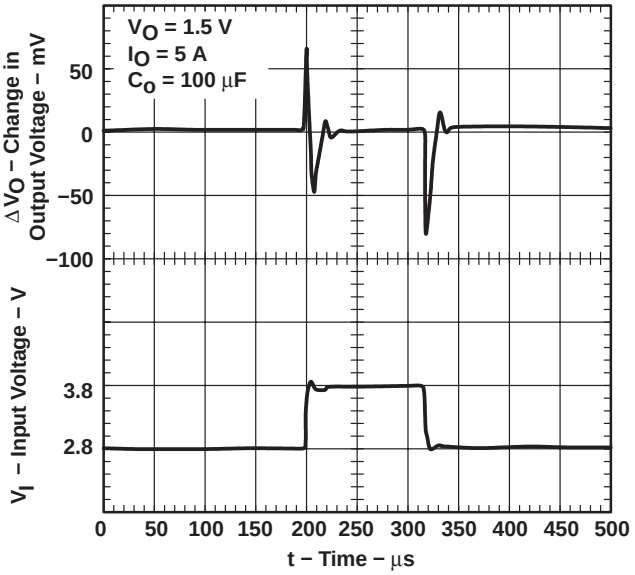


Figure 13

TYPICAL CHARACTERISTICS

TPS75515
LOAD TRANSIENT RESPONSE

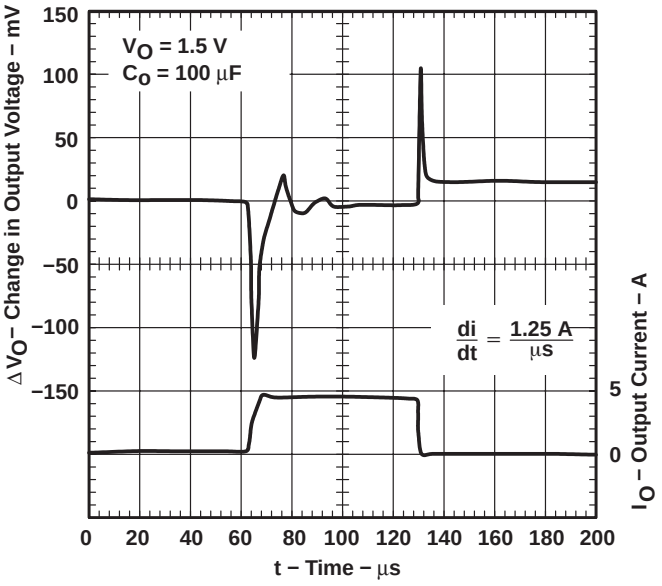


Figure 14

TPS75533
LINE TRANSIENT RESPONSE

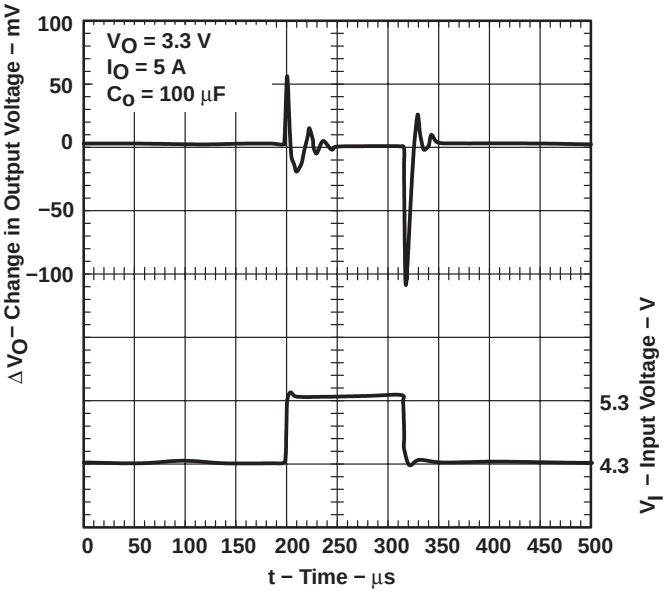


Figure 15

TPS75533
LOAD TRANSIENT RESPONSE

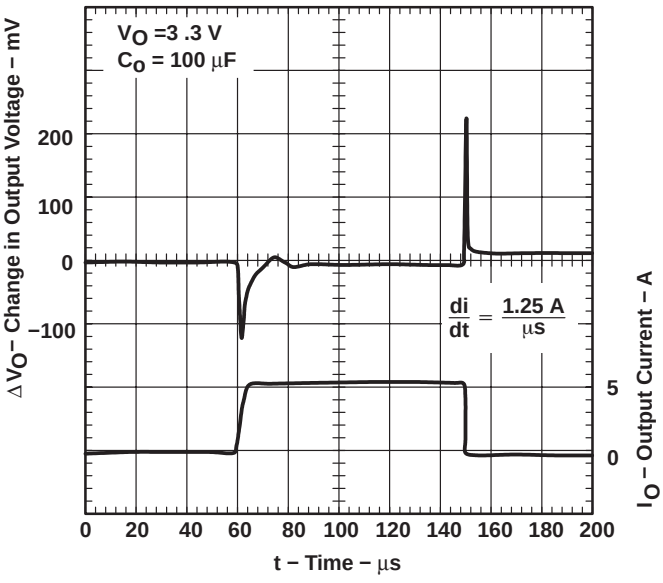


Figure 16

TPS75533
OUTPUT VOLTAGE AND ENABLE VOLTAGE
vs
TIME (START-UP)

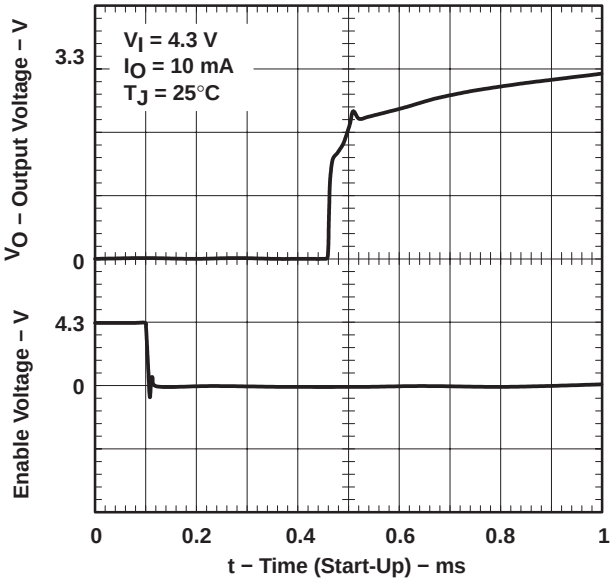


Figure 17

TYPICAL CHARACTERISTICS

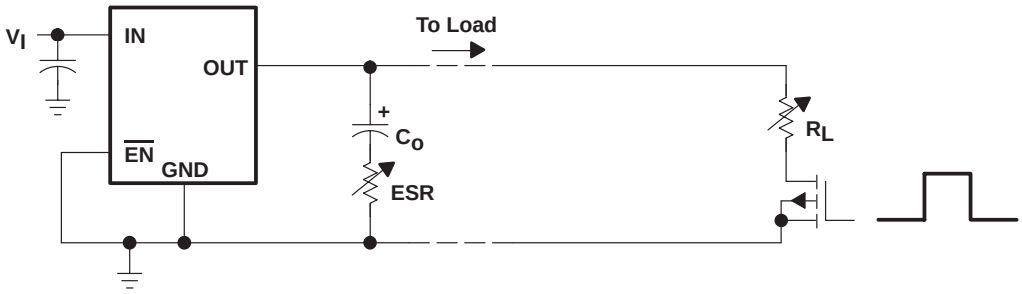


Figure 18. Test Circuit for Typical Regions of Stability (Figures 19 and 20) (Fixed Output Options)

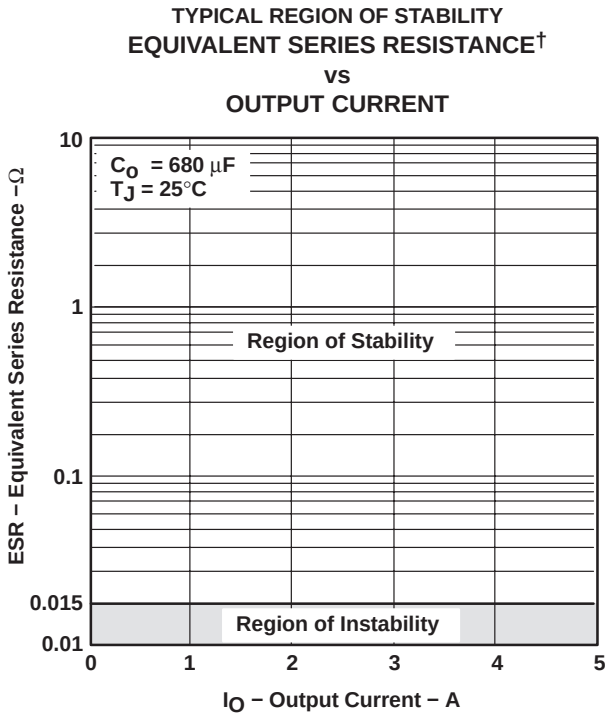


Figure 19

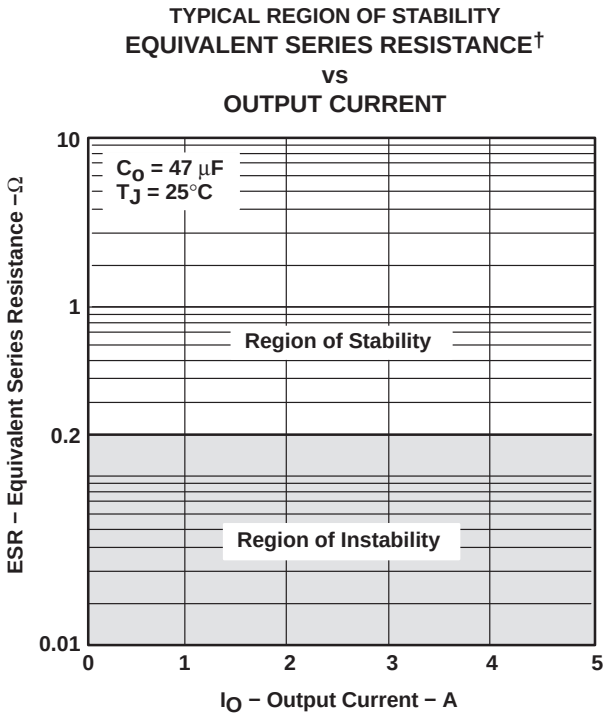


Figure 20

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D\text{max} = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \quad (1)$$

Where:

$V_{I(avg)}$ is the average input voltage.

$V_{O(avg)}$ is the average output voltage.

$I_{O(avg)}$ is the average output current.

$I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 21 illustrates these thermal resistances for (a) a TO−220 package attached to a heatsink, and (b) a TO−263 package mounted on a JEDEC High-K board.

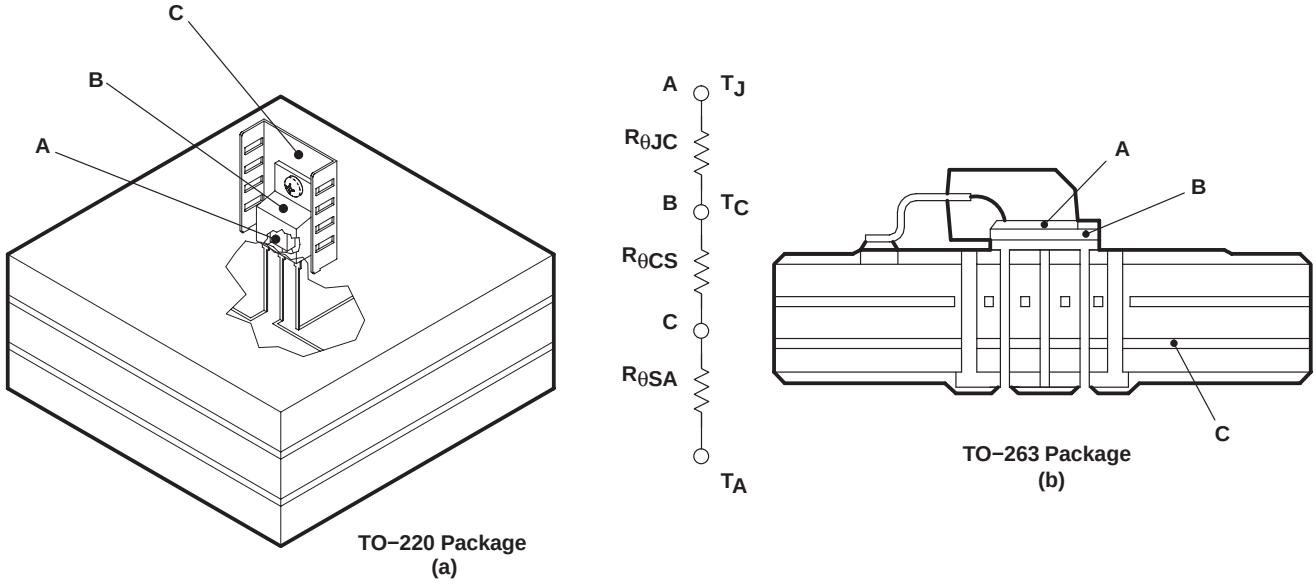


Figure 21. Thermal Resistances

THERMAL INFORMATION

Equation 2 summarizes the computation:

$$T_J = T_A + P_D\text{max} \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (2)$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's datasheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks, like the one attached to the TO−220 package in Figure 21(a), can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a TO−220 package, $R_{\theta CS}$ of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted will provide some heatsinking through the pin solder connections. Some packages, like the TO−263 and TI's TSSOP PowerPAD™ packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 2 simplifies into equation 3:

$$T_J = T_A + P_D\text{max} \times R_{\theta JA} \quad (3)$$

Rearranging equation 3 gives equation 4:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D\text{max}} \quad (4)$$

Using equation 3 and the computer model generated curves shown in Figures 22 and 25, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

TO−220 power dissipation

The TO−220 package provides an effective means of managing power dissipation in through-hole applications. The TO−220 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. A heatsink can be used with the TO−220 package to effectively lower the junction-to-ambient thermal resistance.

To illustrate, the TPS75525 in a TO−220 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 3 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\text{max} = (3.3 - 2.5)\ \text{V} \times 3\ \text{A} = 2.4\ \text{W} \quad (5)$$

Substituting $T_J\text{max}$ for T_J into equation 4 gives equation 6:

$$R_{\theta JA}\text{max} = (125 - 55)°\text{C}/2.4\ \text{W} = 29°\text{C/W} \quad (6)$$

From Figure 22, $R_{\theta JA}$ vs Heatsink Thermal Resistance, a heatsink with $R_{\theta SA}$ = 22°C/W is required to dissipate 2.4 W. The model operating environment used in the computer model to construct Figure 22 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. Since the package pins were soldered to the board, 450 mm^2 of the board was modeled as a heatsink. Figure 23 shows the side view of the operating environment used in the computer model.

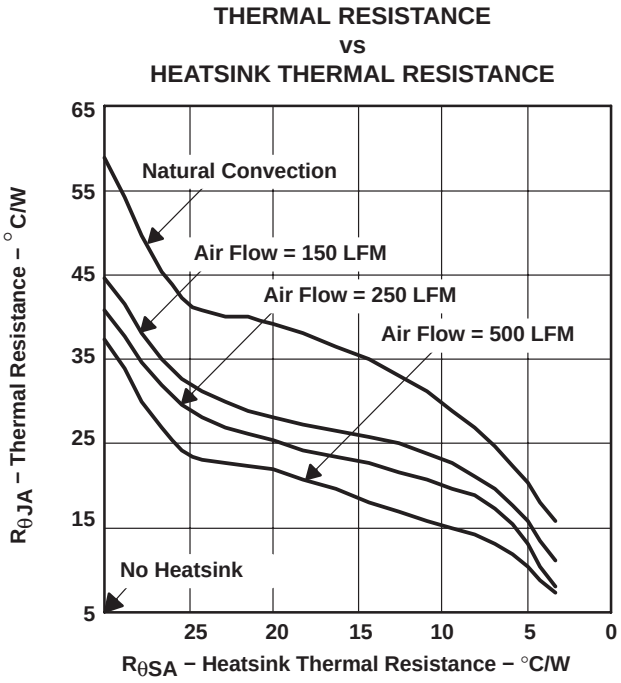


Figure 22

THERMAL INFORMATION

TO−220 power dissipation (continued)

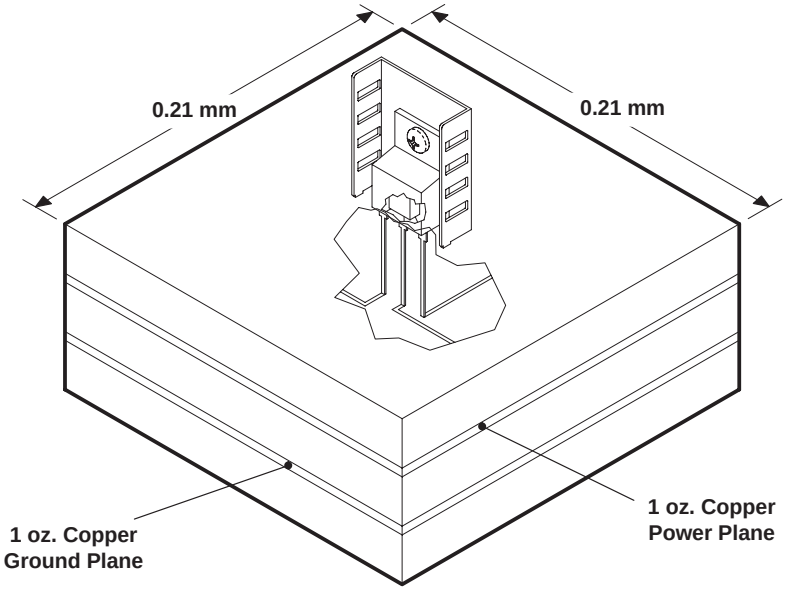


Figure 23

From the data in Figure 22 and rearranging equation 4, the maximum power dissipation for a different heatsink $R_{\theta SA}$ and a specific ambient temperature can be computed (see Figure 24).

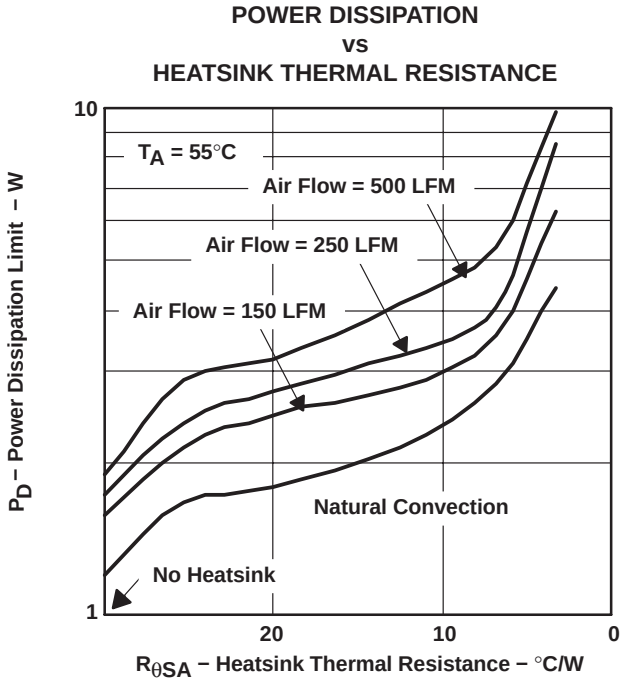


Figure 24

THERMAL INFORMATION

TO−263 power dissipation

The TO−263 package provides an effective means of managing power dissipation in surface mount applications. The TO−263 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the TO−263 package enhances the thermal performance of the package.

To illustrate, the TPS75525 in a TO−263 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 3 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\text{max} = (3.3 - 2.5)\ \text{V} \times 3\ \text{A} = 2.4\ \text{W} \quad (7)$$

Substituting $T_J$max for T_J into equation 4 gives equation 8:

$$R_{\theta JA}\text{max} = (125 - 55)°\text{C}/2.4\ \text{W} = 29°\text{C/W} \quad (8)$$

From Figure 25, $R_{\theta JA}$ vs Copper Heatsink Area, the ground plane needs to be 2 cm^2 for the part to dissipate 2.4 W. The model operating environment used in the computer model to construct Figure 25 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 26 shows the side view of the operating environment used in the computer model.

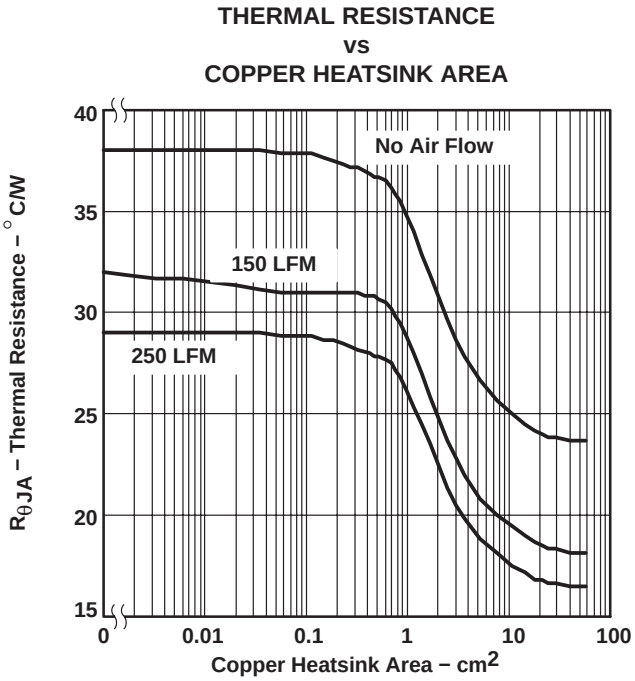


Figure 25

THERMAL INFORMATION

TO−263 power dissipation (continued)

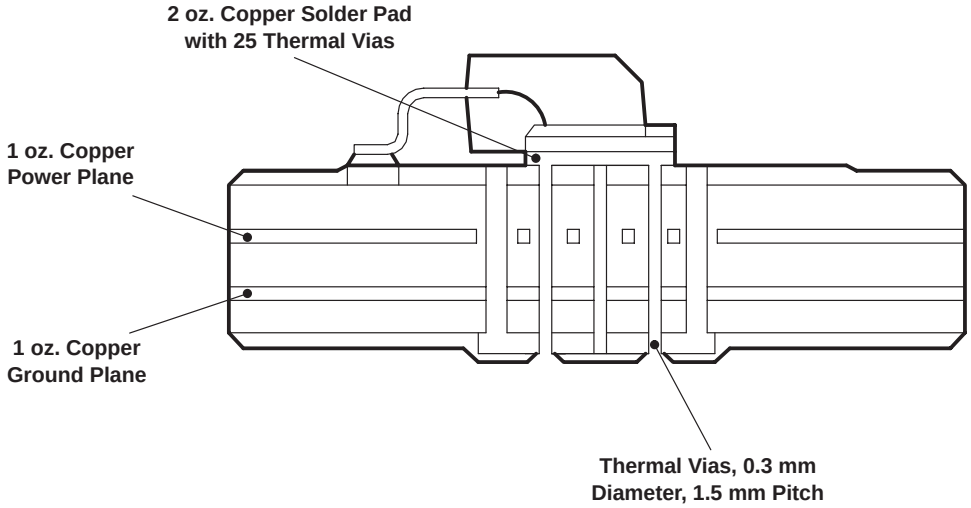


Figure 26

From the data in Figure 25 and rearranging equation 4, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (see Figure 27).

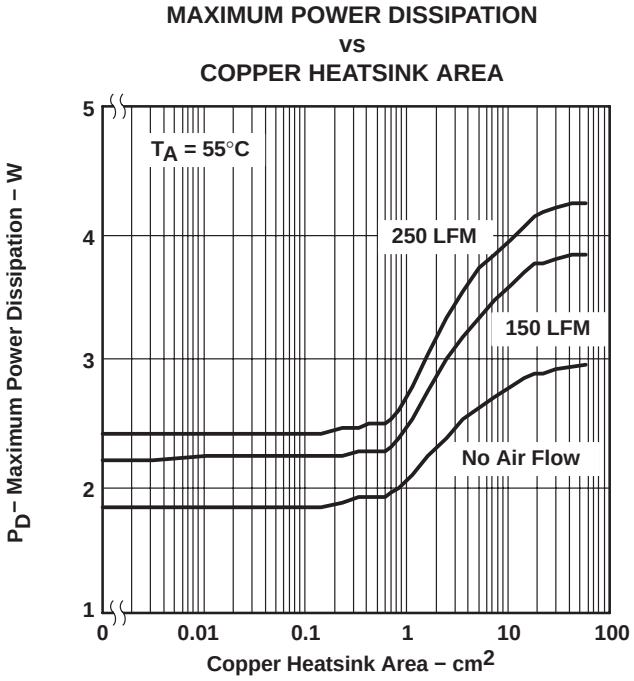


Figure 27

APPLICATION INFORMATION

programming the TPS75501 adjustable LDO regulator

The output voltage of the TPS75501 adjustable regulator is programmed using an external resistor divider as shown in Figure 28. The output voltage is calculated using:

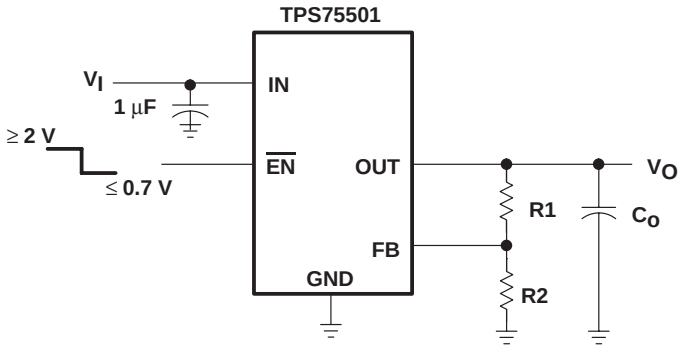
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (9)$$

Where:

V_{ref} = 1.224 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 40-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (10)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	31.6	30.1	kΩ
3.3 V	51	30.1	kΩ
3.6 V	58.3	30.1	kΩ

Figure 28. TPS75501 Adjustable LDO Regulator Programming

regulator protection

The TPS755xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS755xx also features internal current limiting and thermal protection. During normal operation, the TPS755xx limits output current to approximately 10 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

APPLICATION INFORMATION

input capacitor

For a typical application, a ceramic input bypass capacitor (0.22 μF−1 μF) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Due to the impedance of the input supply, large transient currents will cause the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device will turn off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator's input. The size of this capacitor depends on the output current, response time of the main power supply, and the main power supply's distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

output capacitor

As with most LDO regulators, the TPS755xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47 μF with an ESR (equivalent series resistance) of at least 200 mΩ. As shown in Figure 29, most capacitor and ESR combinations with a product of 47e−6 x 0.2 = 9.4e−6 or larger will be stable, provided the capacitor value is at least 47 μF. Solid tantalum electrolytic and aluminum electrolytic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information along with the ESR graphs, Figures 19, 20, and 29, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

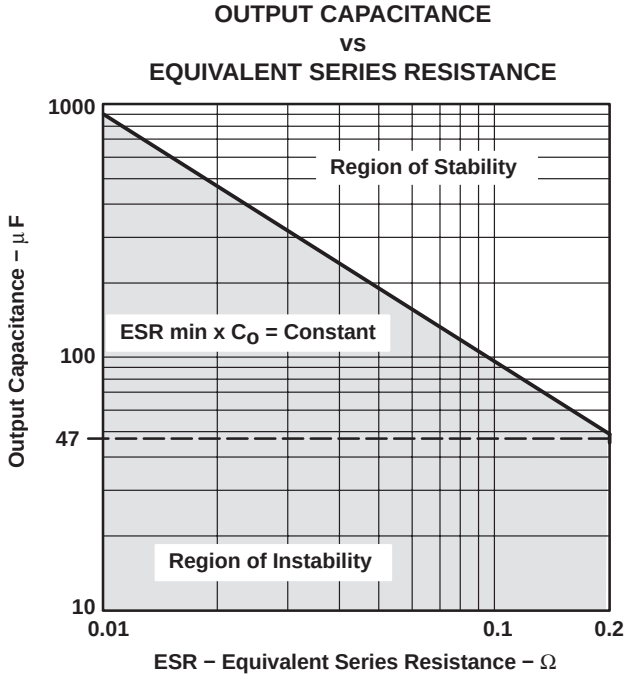


Figure 29

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS75501KC	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75501
TPS75501KC.A	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75501
TPS75501KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75501
TPS75501KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75501
TPS75501KTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75501
TPS75515KC	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75515
TPS75515KC.A	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75515
TPS75515KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75515
TPS75515KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75515
TPS75518KC	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75518
TPS75518KC.A	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75518
TPS75518KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75518
TPS75518KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75518
TPS75525KC	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75525
TPS75525KC.A	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75525
TPS75525KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75525
TPS75525KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75525
TPS75533KC	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75533
TPS75533KC.A	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75533
TPS75533KCG3	Active	Production	TO-220 (KC) | 5	50 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 125	75533
TPS75533KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75533

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS75533KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75533
TPS75533KTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	75533

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

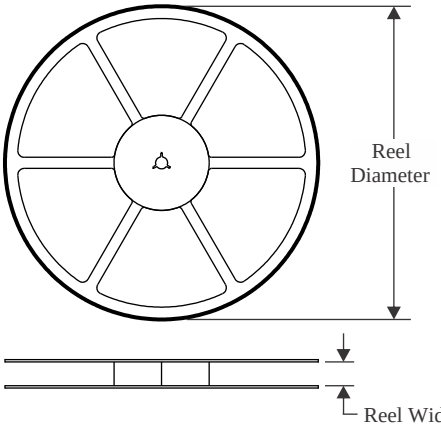
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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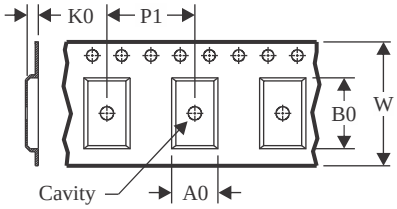
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

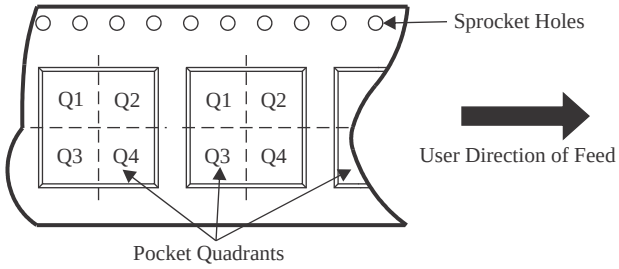


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

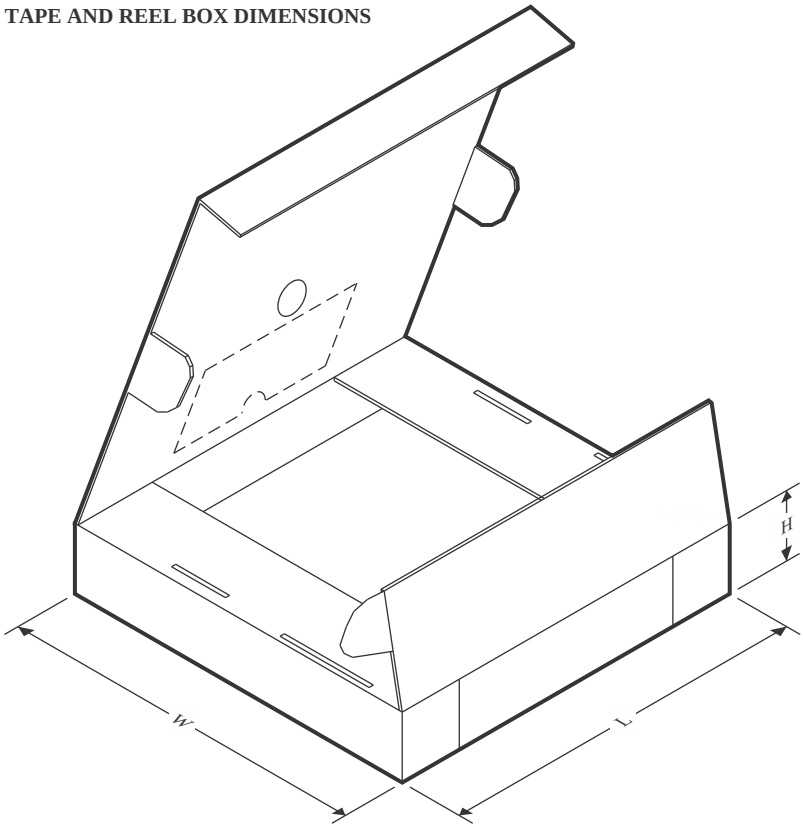
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75501KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS75515KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS75518KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS75525KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS75533KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2

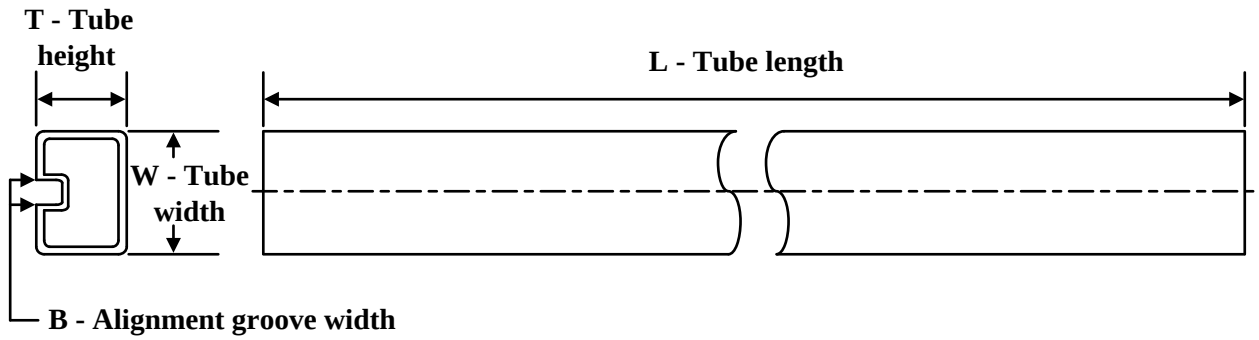
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75501KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS75515KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS75518KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS75525KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS75533KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0

TUBE



*All dimensions are nominal

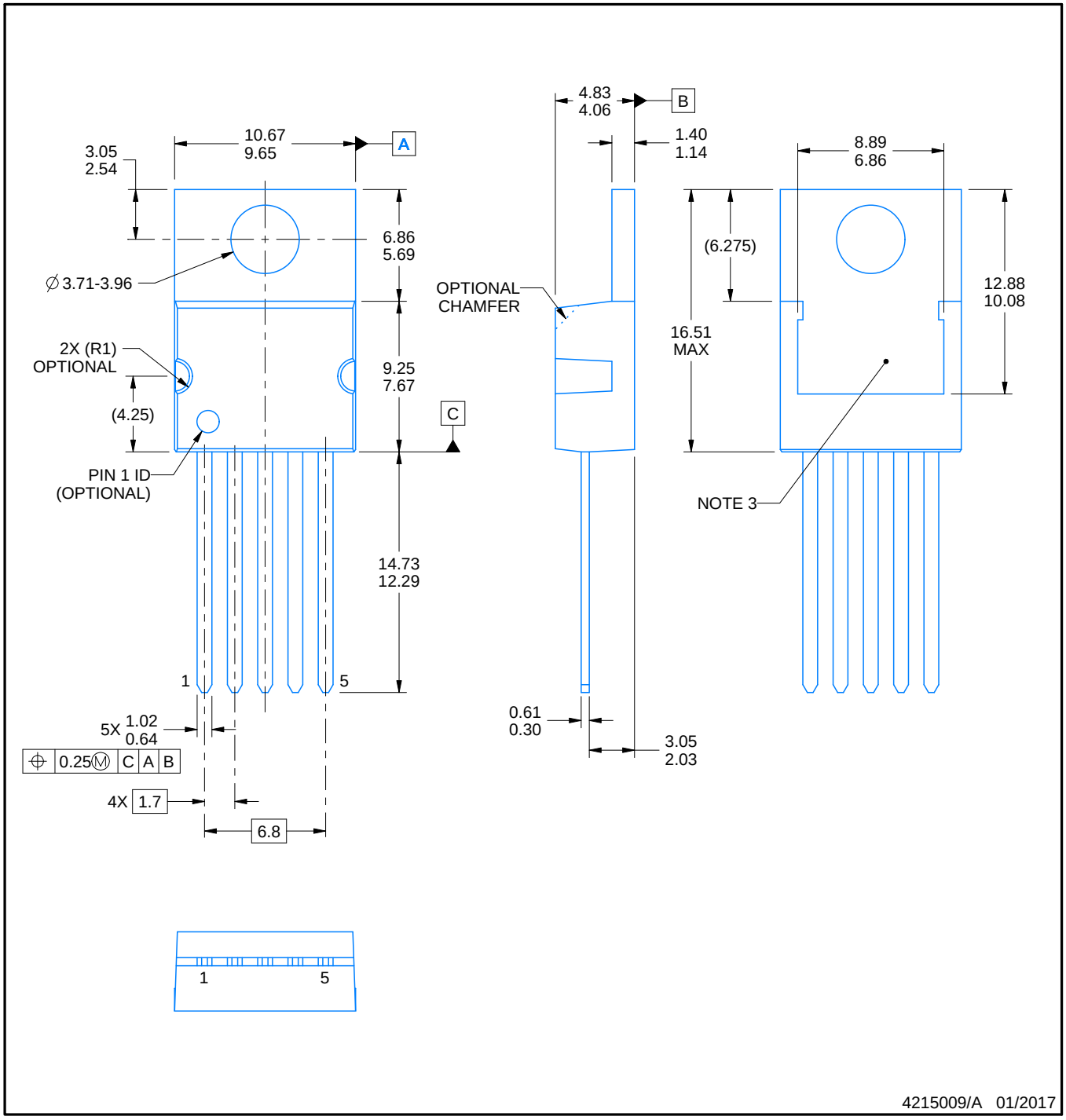
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS75501KC	KC	TO-220	5	50	546	31	11930	3.17
TPS75501KC.A	KC	TO-220	5	50	546	31	11930	3.17
TPS75515KC	KC	TO-220	5	50	546	31	11930	3.17
TPS75515KC.A	KC	TO-220	5	50	546	31	11930	3.17
TPS75518KC	KC	TO-220	5	50	546	31	11930	3.17
TPS75518KC.A	KC	TO-220	5	50	546	31	11930	3.17
TPS75525KC	KC	TO-220	5	50	546	31	11930	3.17
TPS75525KC.A	KC	TO-220	5	50	546	31	11930	3.17
TPS75533KC	KC	TO-220	5	50	546	31	11930	3.17
TPS75533KC.A	KC	TO-220	5	50	546	31	11930	3.17
TPS75533KCG3	KC	TO-220	5	50	546	31	11930	3.17

KC0005A

PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



NOTES:

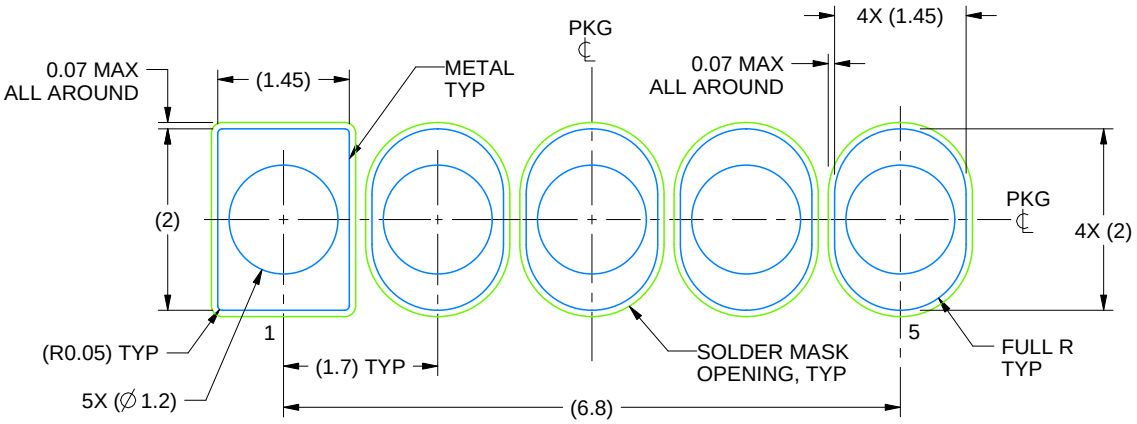
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

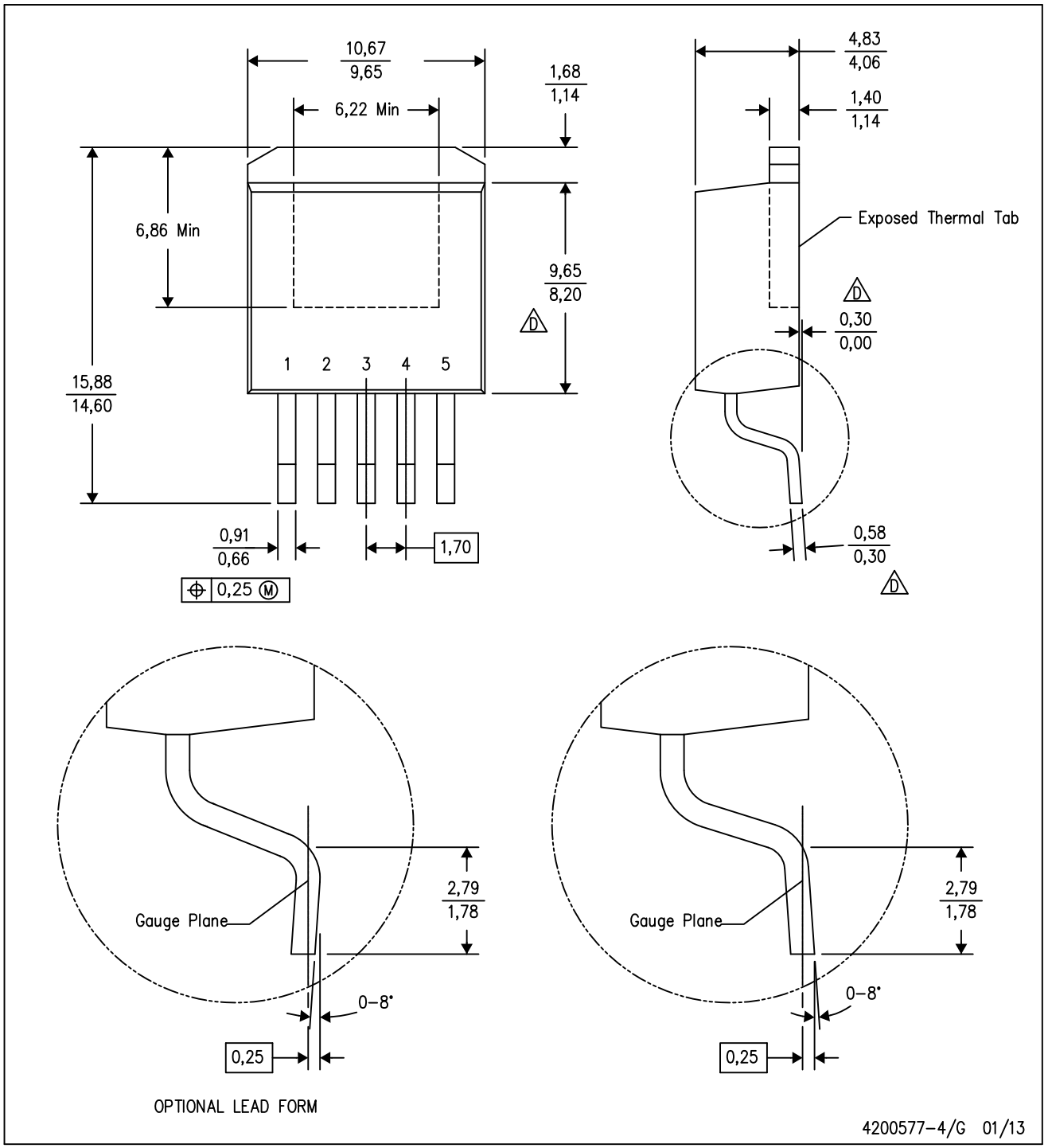
TO-220



LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

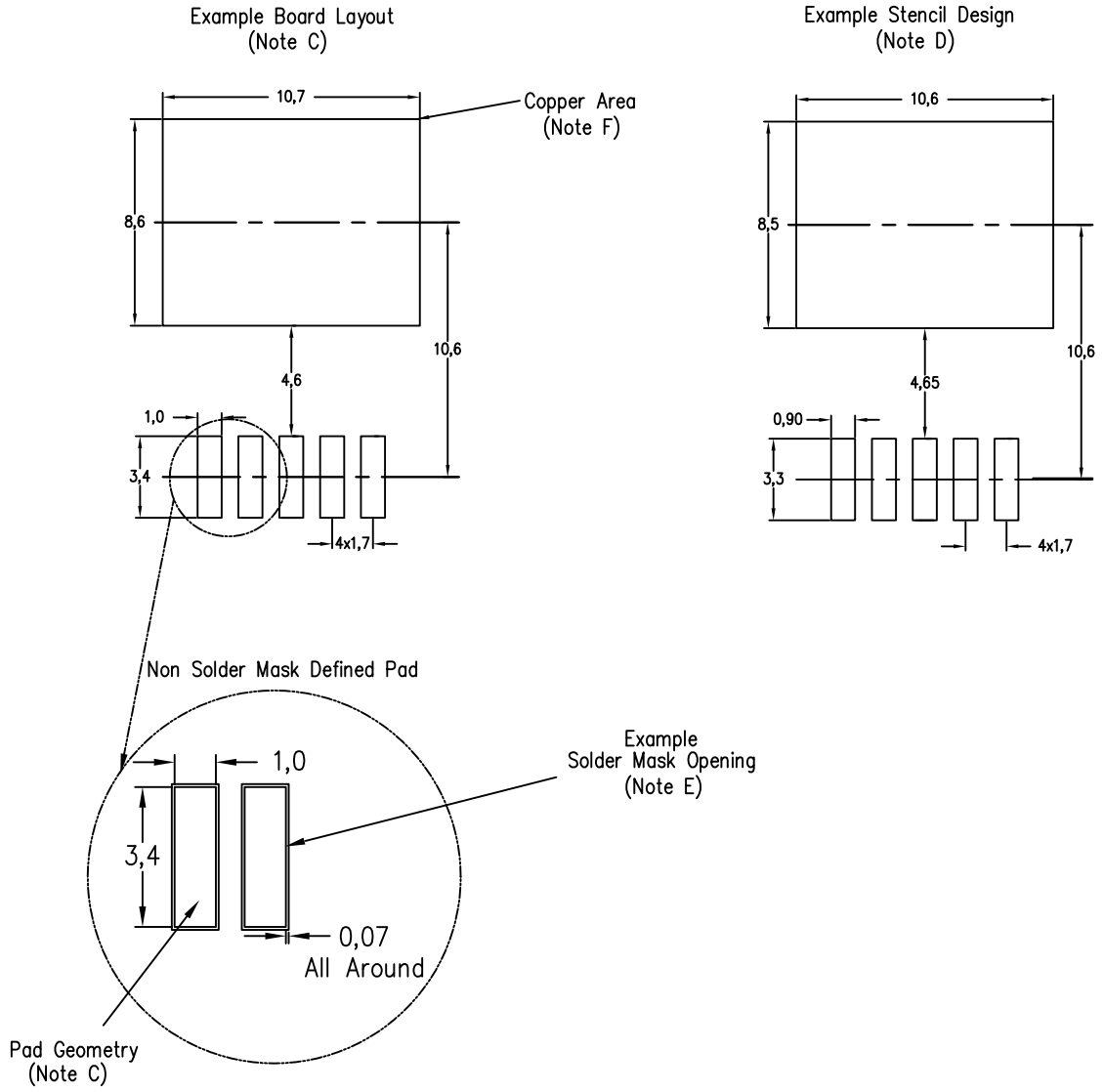
4215009/A 01/2017

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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