TPS794 250mA, Low-Dropout Linear Regulator

1 Features

- 250mA low-dropout regulator with enable
- Available in fixed and adjustable versions
- High PSRR: 60dB at 10kHz
- Fast start-up
- Excellent load, line transient response
- Very low dropout voltage: 155mV(typ) at full load
- Available in HVSSOP-8 and SOT223-6 packages

2 Applications

- TV applications
- Building automation
- Smartphones and tablets
- Connected peripherals and printers
- Home theater and entertainment applications

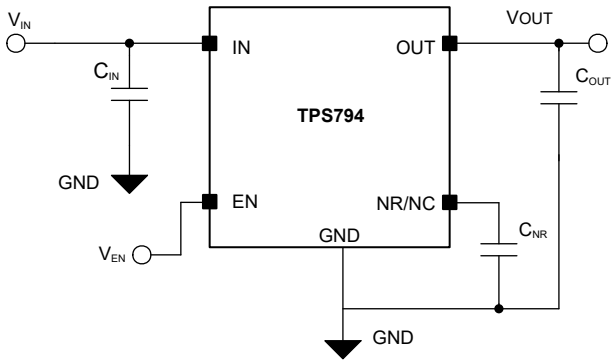
3 Description

The TPS794 low-dropout (LDO) linear voltage regulator features high power-supply rejection ratio (PSRR), low-noise, fast start-up, and excellent line and load transient responses. Each device in the family is stable with a small 2.2µF ceramic capacitor on the output. The TPS794 offers low dropout voltages, 155mV (typ) at 250mA.Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS794	DGN (HVSSOP, 8)	3mm × 4.9mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm

(1) For more information, see the *Section 11* addendum.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

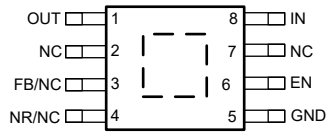


Figure 4-1. DGN Package, MSOP-8 PowerPad™ (Top View)

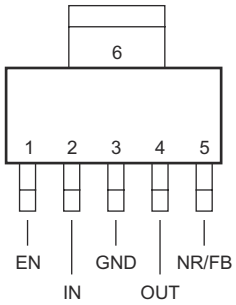


Figure 4-2. DCQ Package, 6-Pin SOT-223 (Top View, legacy chip only)

Table 4-1. Pin Functions

PIN				DESCRIPTION
NAME	DGN (HVSSOP)	DCQ (SOT-223)	TYPE	
NR/NC	4	5	Input (Legacy) / No Connect (New)	Noise Reduction pin (legacy chip only). Connecting an external capacitor to this pin filters noise generated by the internal bandgap. This configuration improves power-supply rejection and reduces output noise for the legacy chip only. No Connect pin (new chip only). This pin is not internally connected. Connect to GND for improved thermal performance or leave floating. For lower noise performance on a fixed device, consider looking at the TPS7A20.
EN	6	1	Input	The EN pin is an input that enables or shuts down the device. When EN is a logic high, the device is enabled. When the device is a logic low, the device is in shutdown mode.
FB	3	5	Input	Feedback input voltage for the adjustable device.
GND	5, PAD	3, 6	Ground	Regulator ground
IN	8	2	Input	Unregulated input to the device.
NC	2, 7		No Connect	This pin is not internally connected. Connect to GND for improved thermal performance or leave floating.
OUT	1	4	Output	Output of the regulator.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN} , V_{EN}, V_{OUT} (Legacy Chip)	–0.3	6	V
	V_{IN} , V_{EN} (New Chip)	–0.3	6.5	V
	V_{OUT} (New Chip)	–0.3	V_{IN} + 0.3 (2)	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.5 V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, V all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		2.7		5.5	V
V_{EN}	Enable voltage		0		5.5	V
V_{OUT}	Output voltage		V_{FB}		5	V
I_{OUT}	Output current		0		250	mA
C_{IN}	Input capacitor	Input capacitor	1			µF
C_{OUT}	Output capacitor		1.0(1) (2)	2.2		µF
C_{NR}	Noise reduction capacitor(3)		0	10	100	nF
C_{FF}	Feed-forward capacitor (Legacy Chip)			15		pF
	Feed-forward capacitor (New Chip)(4)			10	100	nF
R_2	Lower feedback resistor (Legacy Chip)			30.1		kΩ
F_{EN}	Enable toggle frequency (New Chip)				10	kHz
T_J	Operating junction temperature		–40		125	°C

(1) If C_{FF} is not used the minimum recommended C_{OUT} = 2.2µF.
(2) The minimum effective capacitance is 0.47 µF for the new chip.
(3) Legacy Chip only. The New Chip does not have a Noise Reduction pin. For more information please refer to Pin Functions table.
(4) Feed-forward capacitor is optional and not required for stability.

5.4 Thermal Information

THERMAL METRIC (1)		TPS794		UNIT
		DGN (MSOP-8)	DGN (MSOP-8) (2)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.6	51.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.1	82.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.2	25.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	6.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.2	25.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.2	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Packaging application note.
(2) New Chip.

5.5 Electrical Characteristics

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		5.5	V
I_{OUT}	Continuous output current			0		250	mA
V_{OUT}	Output voltage range	TPS79401	0µA < I_{OUT} < 250mA	1.225		5.5 – $V_{DROPOUT}$	V
	Accuracy	TPS79401	0µA < I_{OUT} < 250mA, V_{OUT}+1V ≤ V_{IN} < 5.5V	0.97(V_{OUT})	V_{OUT}	1.03(V_{OUT})	V
		Fixed V_{OUT}	0µA < I_{OUT} < 250mA, V_{OUT}+1V ≤ V_{IN} < 5.5V	-3		3	%

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5.5 Electrical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	Quiescent current (GND current)	0µA ≤ I_O ≤ 250mA (Legacy Chip)			170	220	µA
		0µA ≤ I_O ≤ 250mA(New Chip)			250	1000	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0µA ≤ I_{OUT} ≤ 250mA			10		mV
$\Delta V_{OUT}/\Delta VIN$	Line regulation	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V			0.05	0.12	%/V
Vn[2]	Output noise voltage (TPS79428)	BW = 100Hz to 100kHz, I_{OUT} =250mA	C_{NR} = 0.001µF		55		μV_{RMS}
	Output noise voltage (TPS79428)	BW = 100Hz to 100kHz, I_{OUT} =250mA	C_{NR} = 0.0047µF		36		μV_{RMS}
	Output noise voltage (TPS79428)	BW = 100Hz to 100kHz, I_{OUT} =250mA	C_{NR} = 0.01 µF		33		μV_{RMS}
	Output noise voltage (TPS79428)	BW = 100Hz to 100kHz, I_{OUT} =250mA	C_{NR} = 0.1µF		32		μV_{RMS}
	Output noise voltage (TPS79418)	BW = 100Hz to 100kHz, I_{OUT} =250mA	(New Chip)		71		μV_{RMS}
t_{STR}	Time, start-up (TPS79428)	R_L = 14 Ω, C_{OUT} = 1µF	C_{NR} = 0.001µF		50		µs
	Time, start-up (TPS79428)		C_{NR} = 0.0047µF		50		
	Time, start-up (TPS79428)		C_{NR} = 0.01µF		50		
	Time, start-up (TPS79428)		(New Chip)		500		
I_{CL}	Output current limit	V_{OUT} = 0V(Legacy Chip)			925		mA
I_{CL}	Output current limit	V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{OUT} = 0.9 x $V_{OUT(NOM)}$ (New Chip only)		320		460	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V (New Chip)			175		mA
I_{SHDN}	Shutdown current	V_{EN} = 0V, 2.7V < V_I < 5.5V(Legacy Chip)[3]			0.07	1	µA
		V_{EN} = 0V, 2.7V < V_I < 5.5V(New Chip)[3]			0.01	1	
$V_{EN(HI)}$	High-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		1.7		V_{IN}	V
$V_{EN(HI)}$	High-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V (New Chip)		0.85		V_{IN}	V
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V		0		0.7	V
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V ≤ V_{IN} ≤ 5.5V (New Chip)		0		0.425	V
I_{EN}	Enable pin current	V_{EN} = 0 V		–1		1	µA

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5.5 Electrical Characteristics (continued)

over recommended operating temperature range, T_J = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{O(typ)}$ + 1V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (Legacy Chip) (unless otherwise noted). All typical values at T_J= 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{FB}	Feedback pin current (TPS79401)	V_{FB} = 1.225V (Legacy Chip)				1	µA
		V_{FB} = 1.225V (New Chip)				0.05	
V_{REF}	Internal reference (TPS79401)			1.201	1.225	1.25	V
PSRR	Power-supply rejection ratio (TPS79428)	f = 100Hz	I_{OUT} = 250mA (Legacy Chip)		65		dB
			I_{OUT} = 250mA (New Chip)		64		
		f = 10kHz	I_{OUT} = 250mA (Legacy Chip)		60		
			I_{OUT} = 250mA (New Chip)		49		
		f = 100kHz	I_{OUT} = 250mA (Legacy Chip)		40		
			I_{OUT} = 250mA (New Chip)		39		
V_{DO} (4)	Dropout voltage (TPS79428)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 250mA			155	210	mV
	Dropout voltage (TPS79430)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 250mA			155	210	
	Dropout voltage (TPS79433)	V_{IN}= V_{OUT} - 0.1V, I_{OUT} = 250mA			145	200	
V_{UVLO}	UVLO threshold	V_{IN} rising (Legacy Chip)		2.25		2.65	V
		VIN rising (New Chip)		1.32		1.6	
$V_{UVLO(HYST)}$	UVLO hysteresis	T_J = 25°C, V_{CC} rising (Legacy Chip)			100		mV
		T_J = 25°C, V_{CC} rising (New Chip)			130		

(1) Minimum VIN is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) New Chip does not have a Noise Reduction pin.
(3) For adjustable versions, this parameters applies only after V_{IN} is applied; then V_{EN} transitions high to low.
(4) Dropout is not measured for the TPS79418 and TPS79425 since minimum V_{IN} = 2.7 V.

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6 Typical Characteristics

over recommended operating temperature range, TJ = –40°C to +125°C V_{EN} = V_{IN}, V_{IN} = $V_{OUT(typ)}$ + 1V I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF (legacy chip) (unless otherwise noted); all typical values at TJ= 25°C

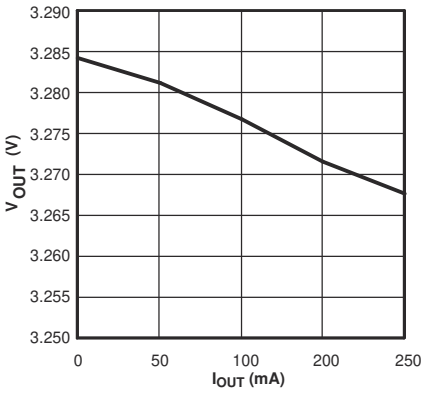


Figure 6-1. TPS794 Output Voltage vs Output Current

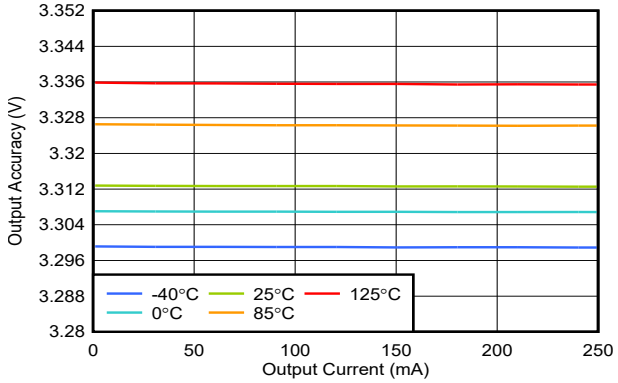


Figure 6-2. TPS794 Output Voltage vs Output Current

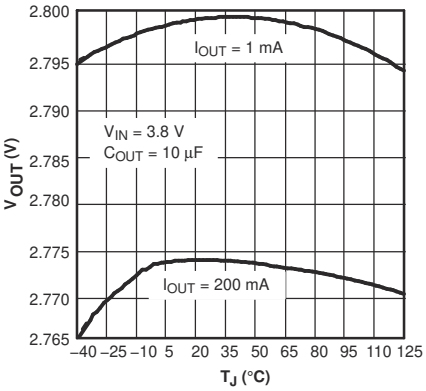


Figure 6-3. TPS794 Output Voltage vs Junction Temperature

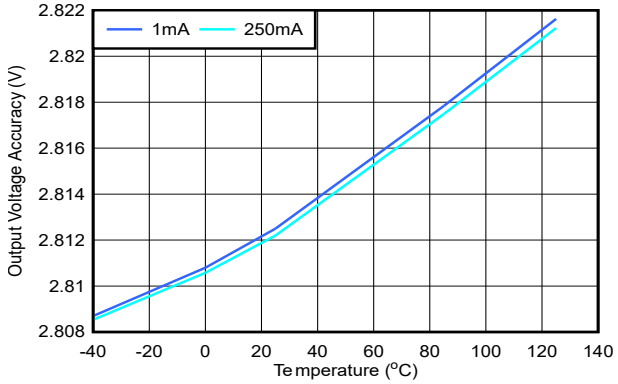


Figure 6-4. TPS794 Output Voltage vs Junction Temperature

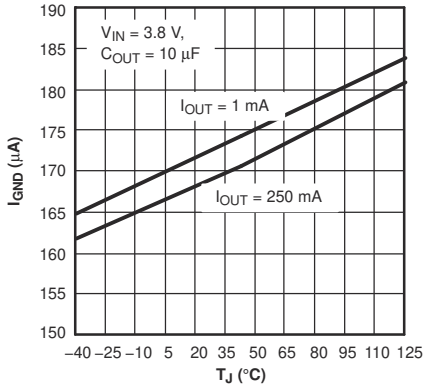


Figure 6-5. TPS794 Ground Current vs Junction Temperature

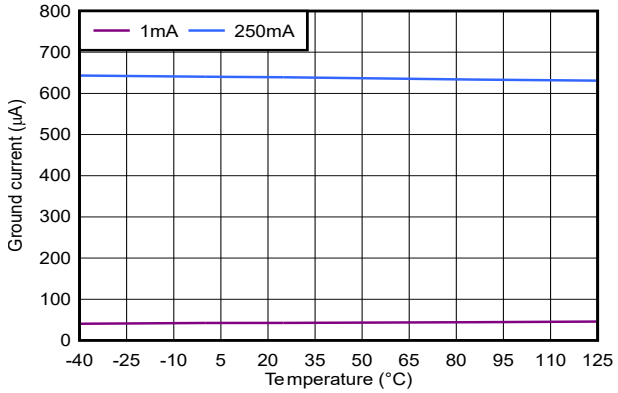


Figure 6-6. TPS794 Ground Current vs Junction Temperature

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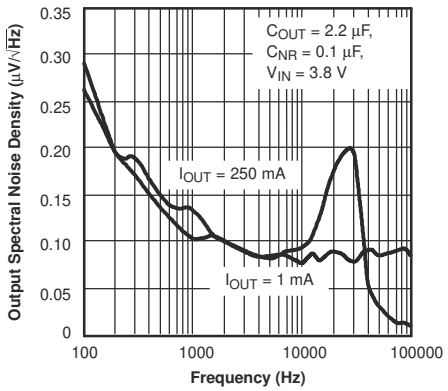
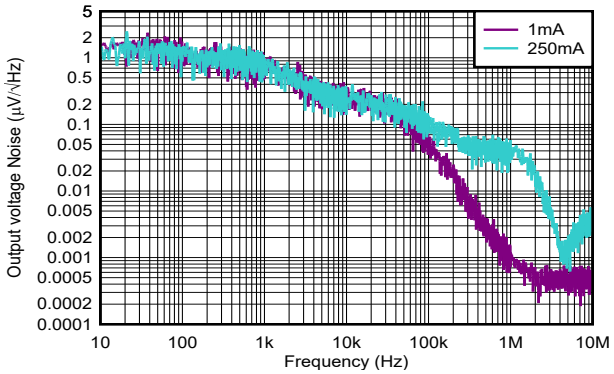


Figure 6-7. TPS794 Output Spectral Noise Density vs Frequency



C_{OUT} = 2.2μF

Figure 6-8. TPS794 Output Spectral Noise Density vs Frequency

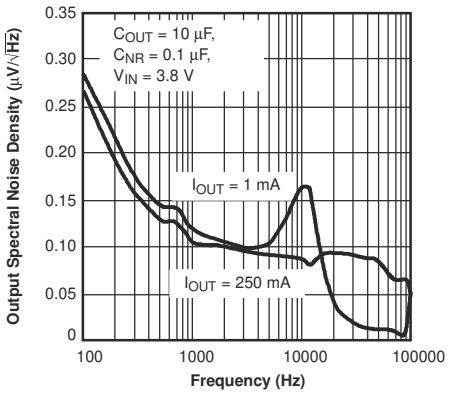
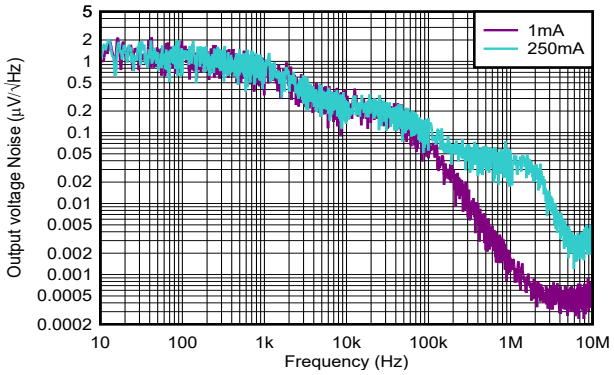


Figure 6-9. TPS794 Output Spectral Noise Density vs Frequency



C_{OUT} = 10μF

Figure 6-10. TPS794 Output Spectral Noise Density vs Frequency

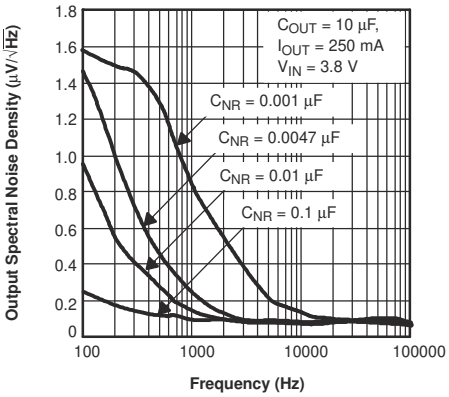


Figure 6-11. TPS79428 Output Spectral Noise Density vs Frequency

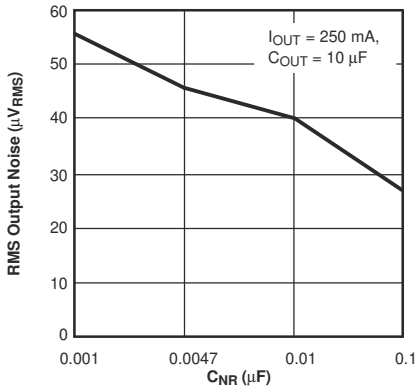


Figure 6-12. TPS79428 Root Mean Squared Output Noise vs C_{NR}

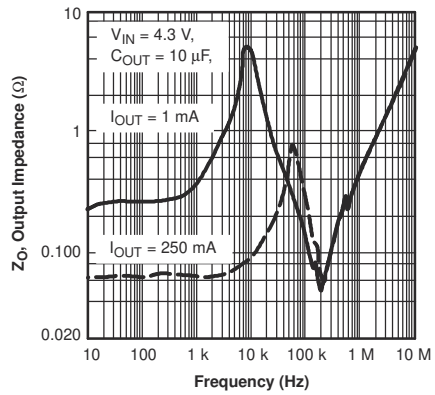


Figure 6-13. TPS794 Output Impedance vs Frequency

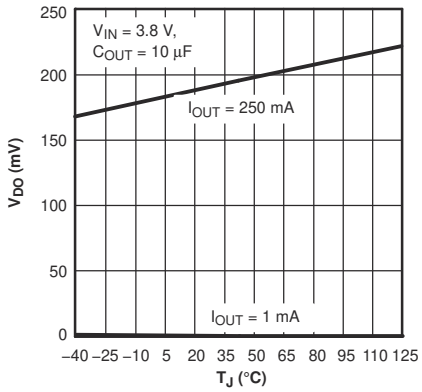


Figure 6-14. TPS794 Dropout Voltage vs Junction Temperature

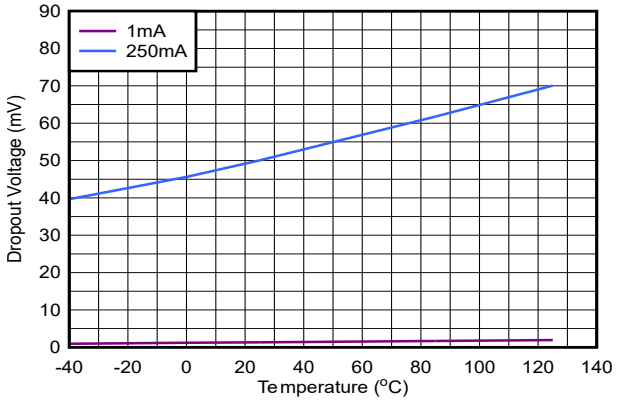


Figure 6-15. TPS794 Dropout Voltage vs Junction Temperature

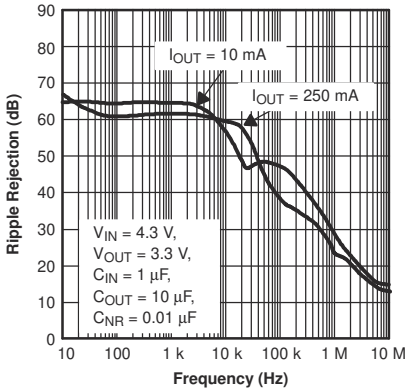
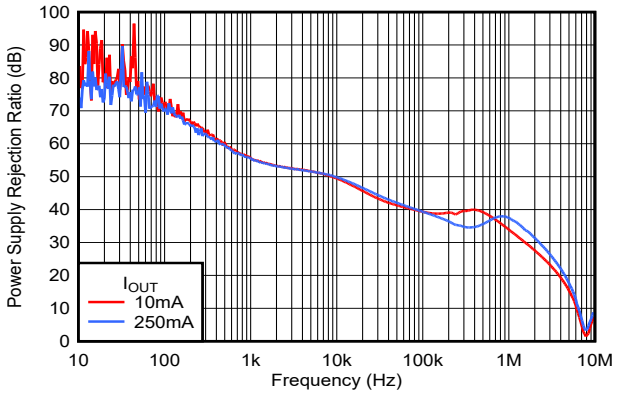


Figure 6-16. TPS794 Ripple Rejection vs Frequency



C_{OUT} = 10µF

Figure 6-17. TPS794 Ripple Rejection vs Frequency

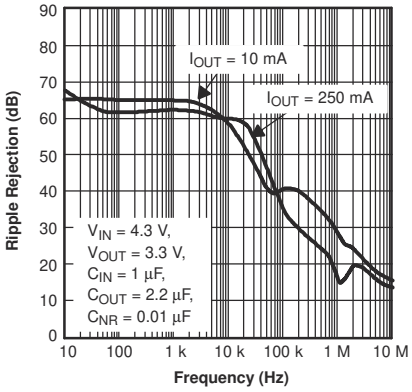
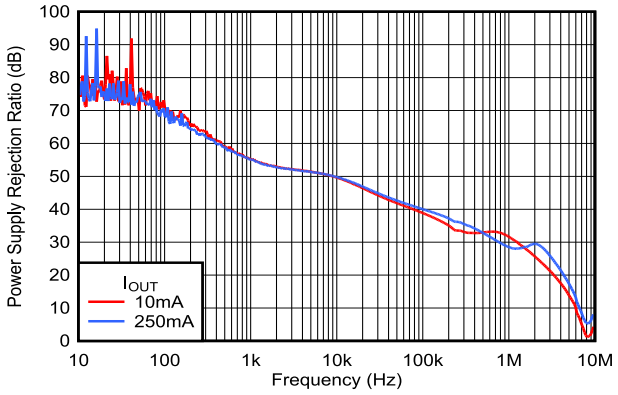


Figure 6-18. TPS794 Ripple Rejection vs Frequency

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C_{OUT} = 2.2µF

Figure 6-19. TPS794 Ripple Rejection vs Frequency

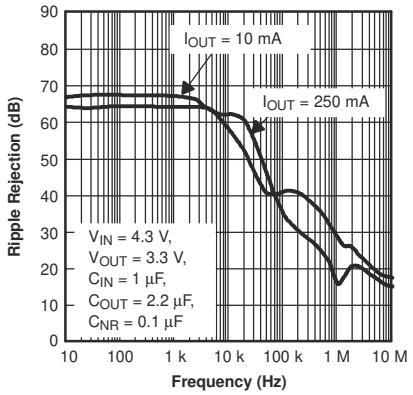


Figure 6-20. TPS794 Ripple Rejection vs Frequency

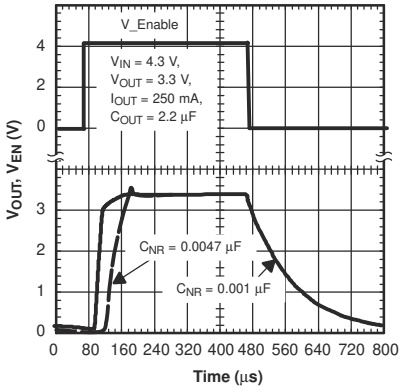


Figure 6-21. TPS794 Output Voltage, Enable Voltage vs Time (Start-up)

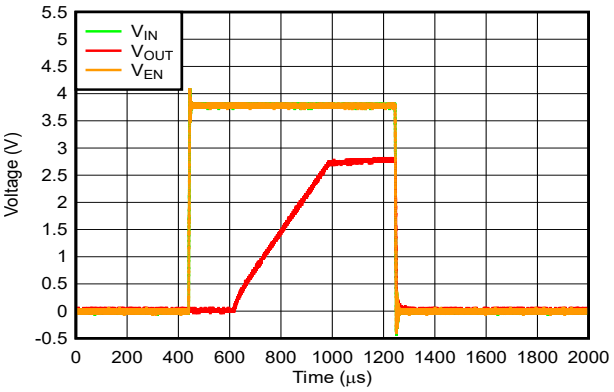


Figure 6-22. TPS794 Output Voltage, Enable Voltage vs Time (Start-up)

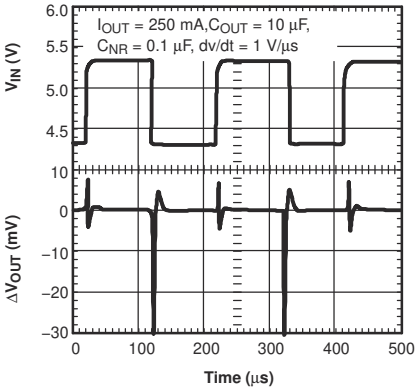
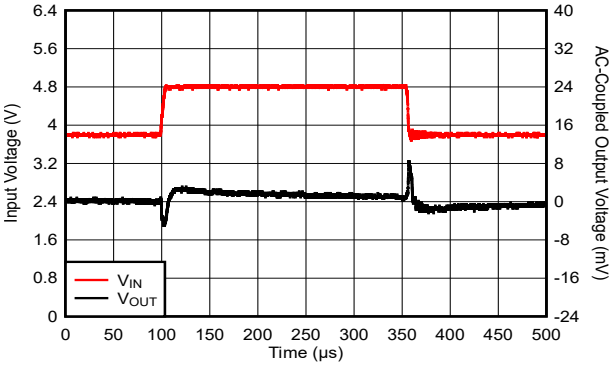


Figure 6-23. TPS794 Line Transient Response



I_{OUT} = 250mA, C_{OUT} = 10µF, dv/dt = 1V/µs

Figure 6-24. TPS794 Line Transient Response

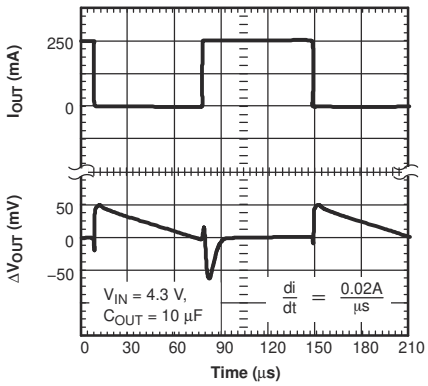
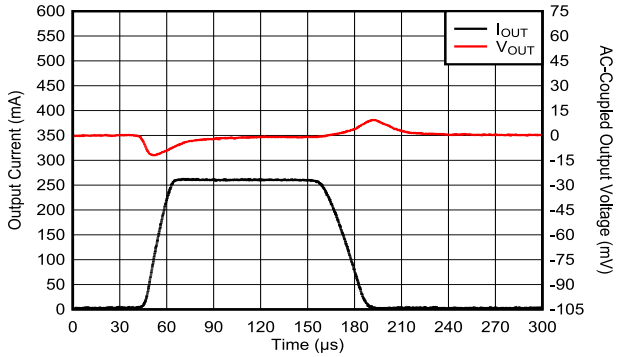


Figure 6-25. TPS794 Load Transient Response



C_{OUT} = 10µF, di/dt = 20mA/µs

Figure 6-26. TPS794 Load Transient Response

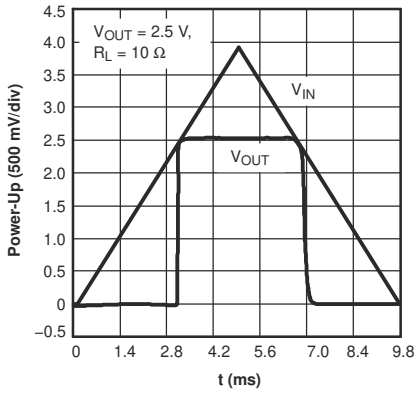


Figure 6-27. TPS794 Power-up/Power-down

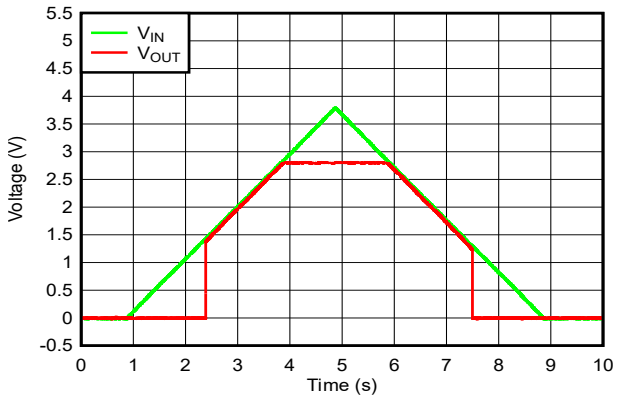


Figure 6-28. TPS794 POWER-UP/POWER-DOWN

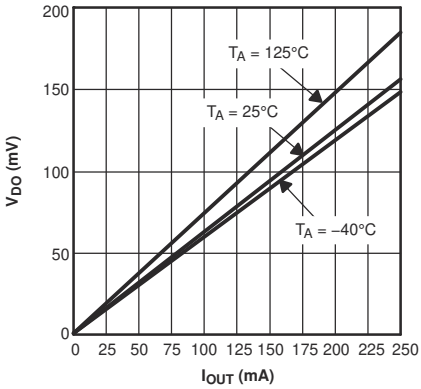


Figure 6-29. TPS794 Dropout Voltage vs Output Current

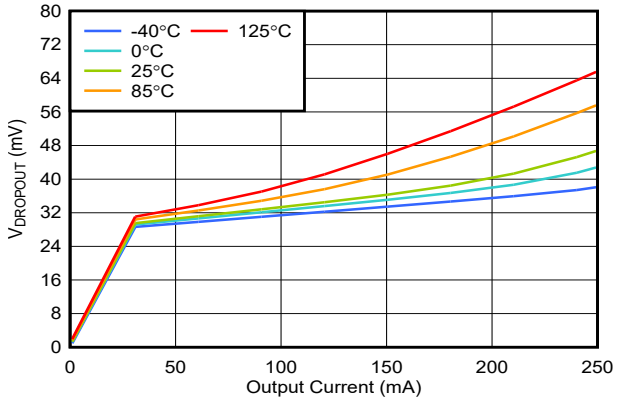


Figure 6-30. TPS794 Dropout Voltage vs Output Current

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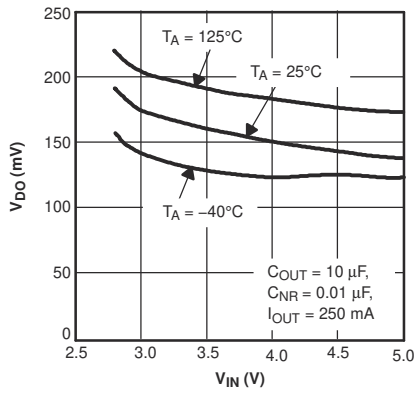


Figure 6-31. TPS794 Dropout Voltage vs Input Voltage

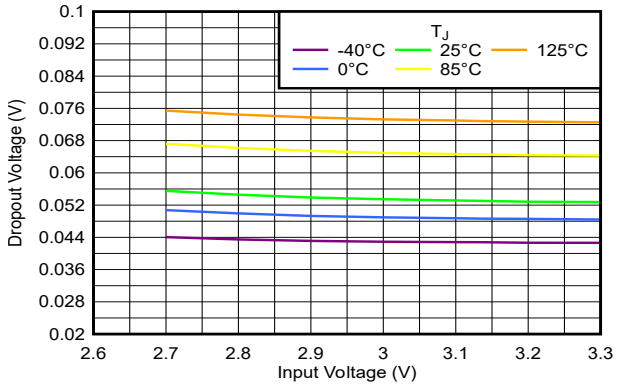


Figure 6-32. TPS794 Dropout Voltage vs Input Voltage

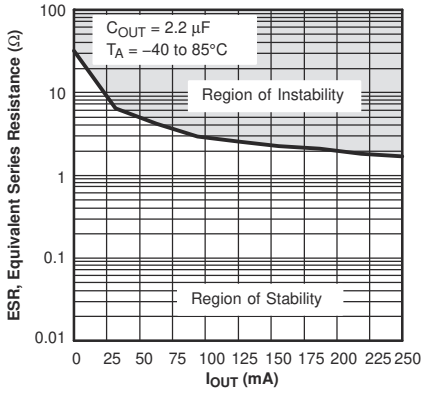


Figure 6-33. TPS794 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

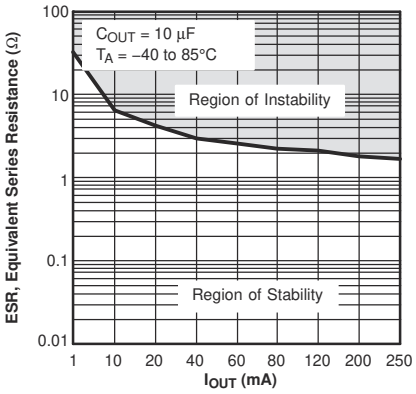


Figure 6-34. TPS794 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

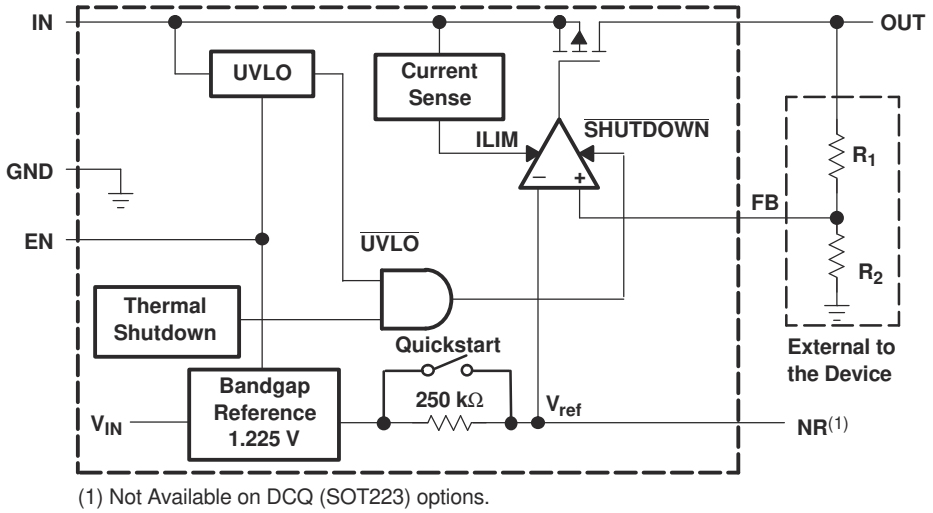
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7 Detailed Description

7.1 Overview

The TPS794 family of LDO regulators has been optimized for use in noise-sensitive. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current, and enable-input to reduce supply currents to less than 1μA when the regulator is turned off.

7.2 Functional Block Diagrams



(1) Not Available on DCQ (SOT223) options.

Figure 7-1. TPS794 Block Diagram (Adjustable Version, Legacy Chip)

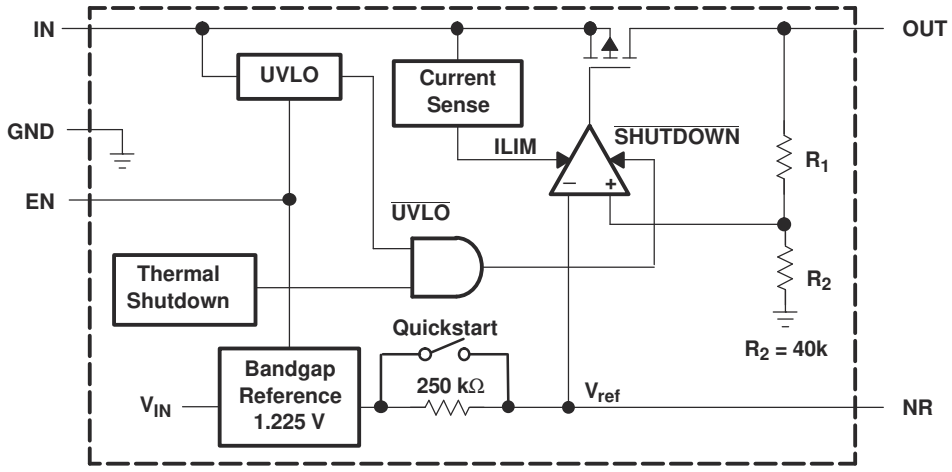


Figure 7-2. TPS794 Block Diagram (Fixed Version, Legacy Chip)

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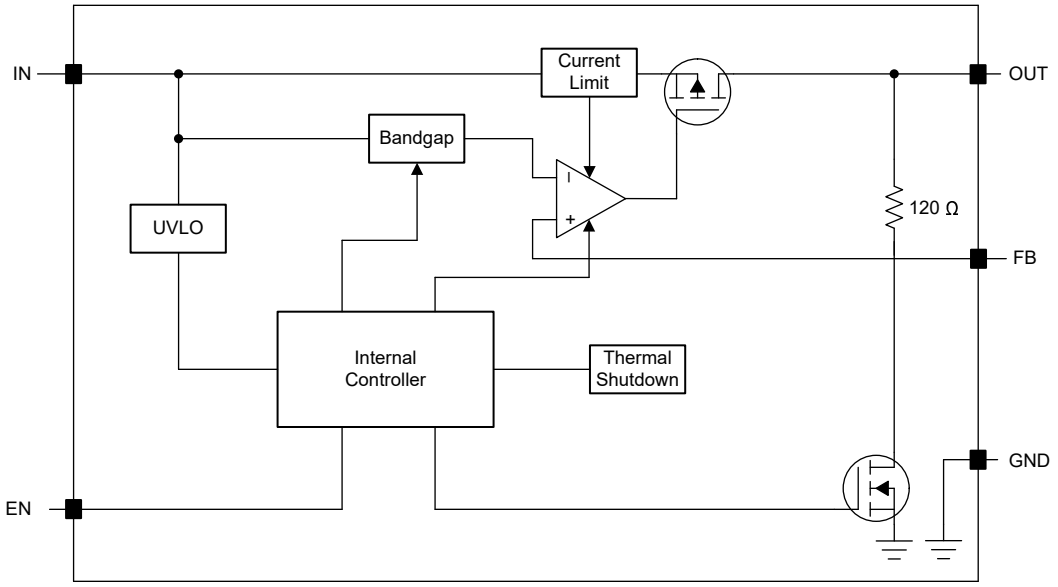


Figure 7-3. TPS794 Block Diagram (Adjustable Version, New Chip)

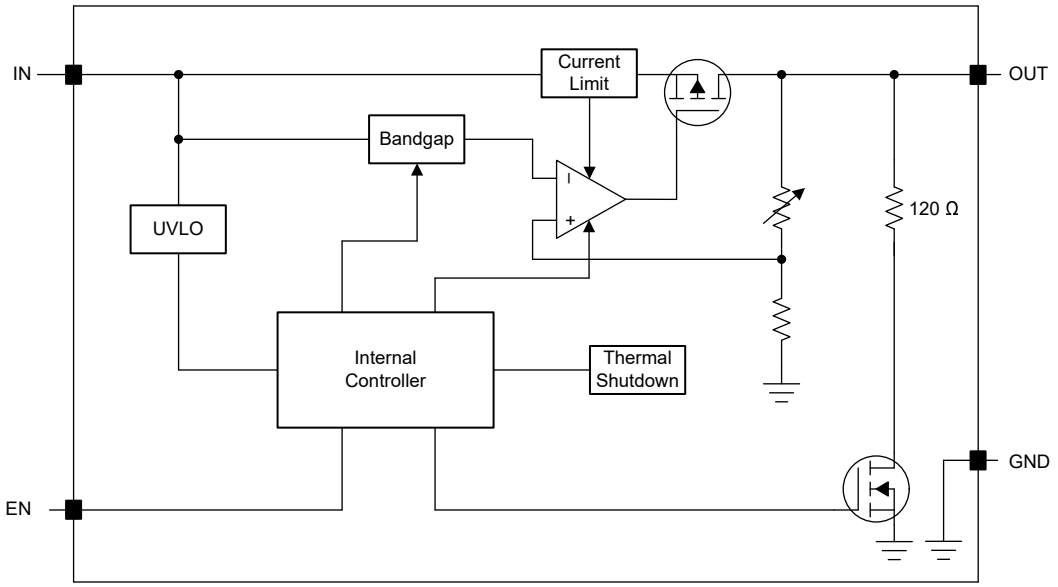


Figure 7-4. TPS794 Block Diagram (Fixed Version, New Chip)

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS794 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit verifies that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$. Turn off the device by forcing the EN pin to drop below the maximum EN pin low-level input voltage (see *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

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7.3.3 Active Discharge (new chip)

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit to discharge the output voltage after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device especially when a large output capacitor is used. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.3.4 Foldback Current Limit

The legacy chip of TPS794 features internal current limiting and thermal protection. During normal operation, the TPS794 limits output current to 925mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 7-5 shows a diagram of the foldback current limit.

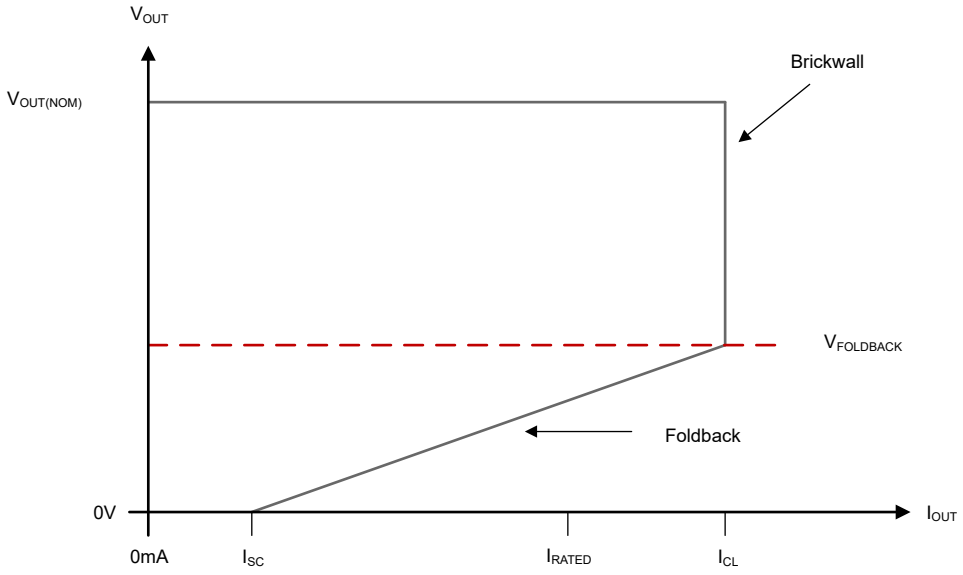


Figure 7-5. Foldback Current Limit

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7.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit the junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS794 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS794 into thermal shutdown degrades device reliability.

7.3.6 Reverse Current

The TPS794 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

As with most modern LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

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Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3V$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. Example Circuit for Reverse Current Protection Using a Schottky Diode shows one approach of protecting the device.

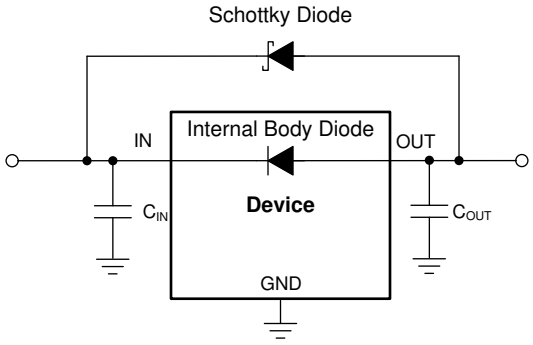


Figure 7-6. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 7-1 shows the conditions that lead to the different modes of operation.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$

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Table 7-1. Device Functional Mode Comparison (continued)

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$[1]

(1) Approximate value for thermal shutdown.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS794 has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current, and an enable input to reduce supply currents.

8.1.1 Adjustable Operation

The output voltage of the TPS794 adjustable regulator is programmed using an external resistor divider as shown in TPS794 Adjustable LDO Regulator Programming. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

- V_{REF} = 1.2246V typ (the internal reference voltage)

Resistors R_1 and R_2 must be chosen for approximately 40µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values must be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to select
R_2 = 30.1 kΩ to set the divider current at 40µA,
C_1 = 15pF for stability, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

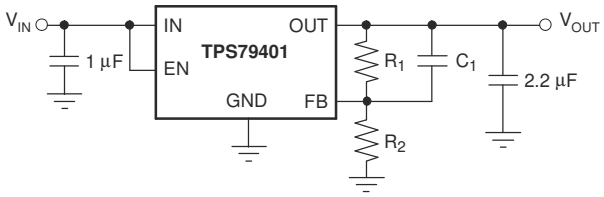
To improve the stability of the adjustable version, place a small compensation capacitor between OUT and FB.

The approximate value of this capacitor can be calculated as Equation 3:

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within TPS794 Adjustable LDO Regulator Programming. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2µF instead of 1µF.

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OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.8 V	14.0 kΩ	30.1 kΩ	22 pF
3.6 V	61.9 kΩ	30.1 kΩ	15 pF

Figure 8-1. TPS794 Adjustable LDO Regulator Programming

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8.1.2 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Start-Up Into Dropout, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

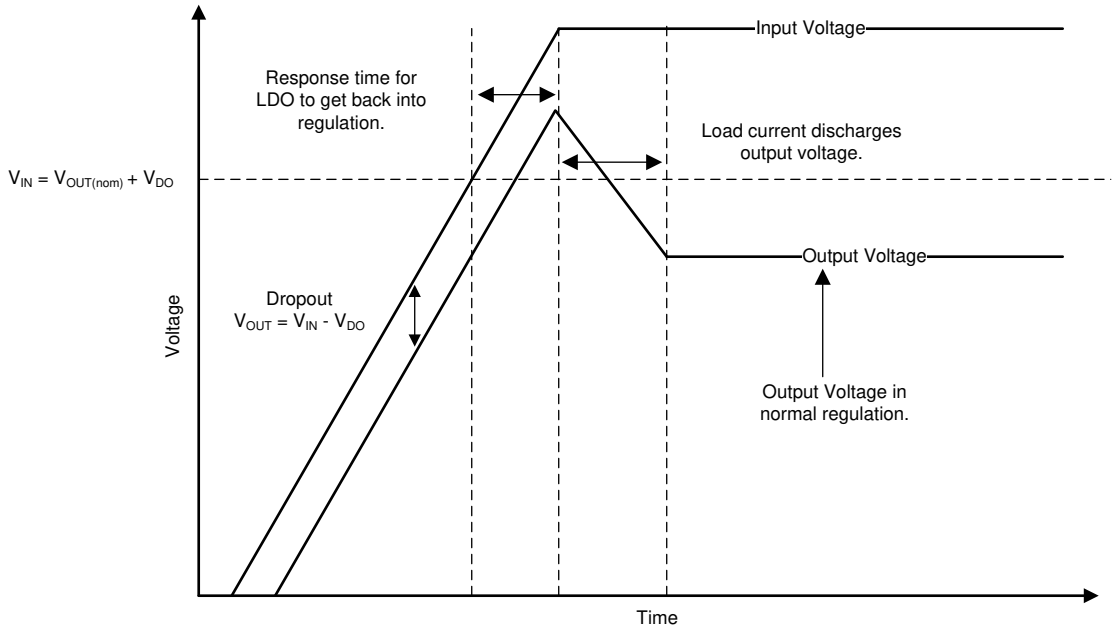


Figure 8-2. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. Line Transients From Dropout illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

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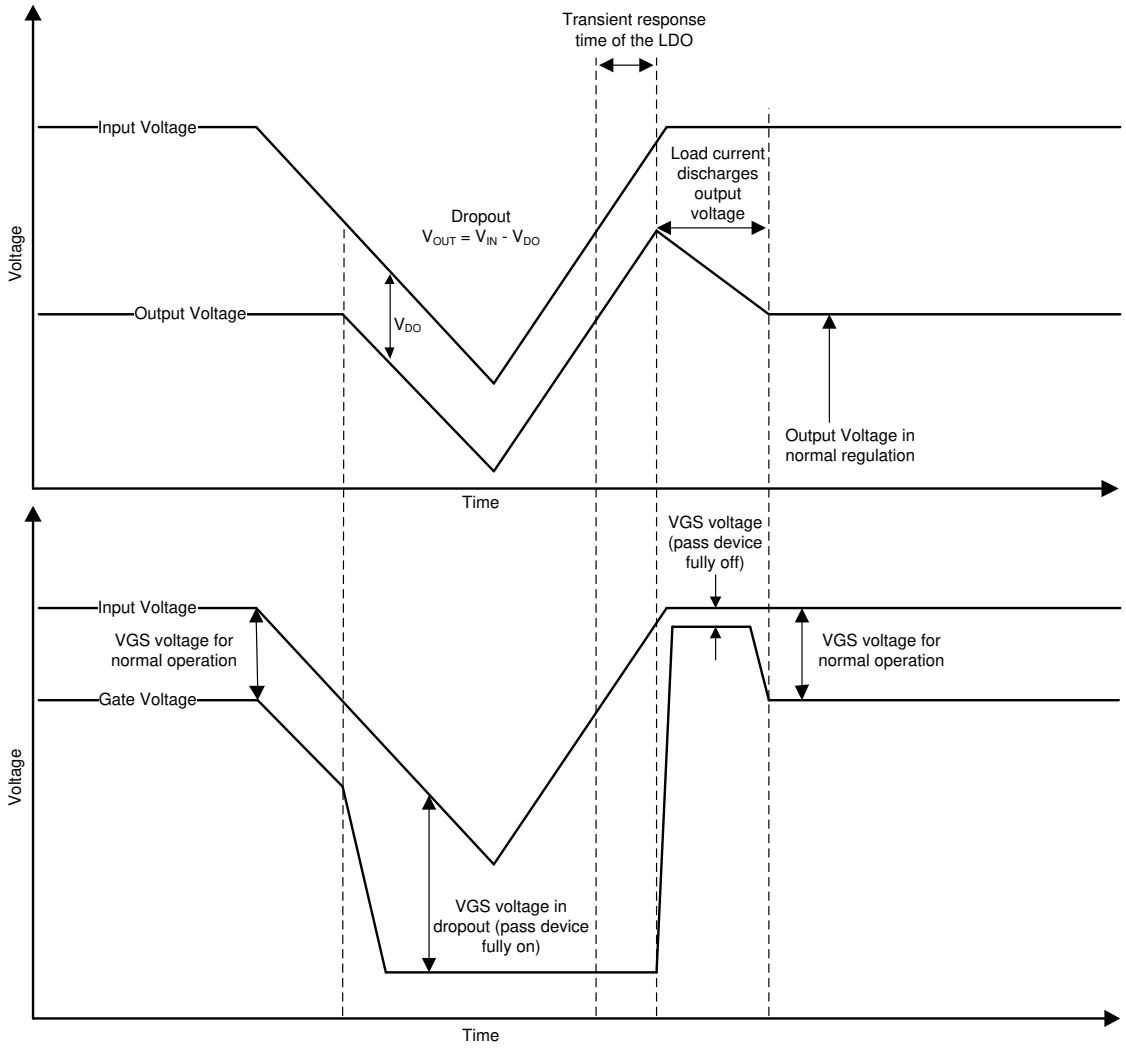


Figure 8-3. Line Transients From Dropout

8.2 Typical Application

A typical application circuit is shown in Figure 8-4.

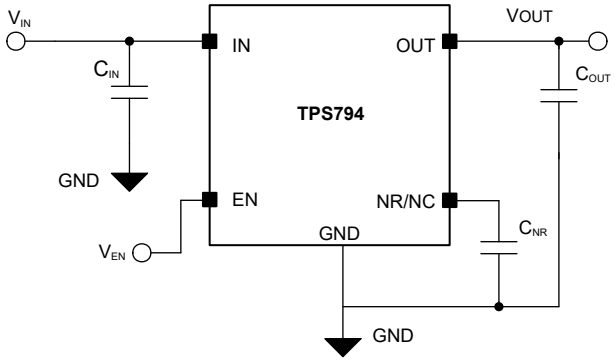


Figure 8-4. Typical Application Circuit

8.2.1 Detailed Design Procedure

Pick the desired output voltage option. An input capacitor of 1µF is used as the battery is connected to the input through a via and a short 10mil (0.01in) trace. An output capacitor of 10µF is used to provide optimal response time for the load transient. Verify that the maximum junction temperature is not exceed by referring to Maximum Ambient Temperature vs Power Dissipation.

8.2.1.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors must be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

8.2.1.2 Input and Output Capacitor Requirements

A 1µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS794, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS794 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1µF. Any
1µF or larger ceramic capacitor is suitable.

8.2.1.3 Noise Reduction and Feed-Forward Capacitor Requirements

The internal voltage reference is a key source of noise in an LDO regulator. The legacy chip of TPS794 has an NR pin which is connected to the voltage reference through a 250kΩ internal resistor. The 250kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor must be no more than 0.1µF to verify that the capacitor is fully charged during the quickstart time provided by the internal switch shown in the *Functional Block Diagrams*.

A feed-forward capacitor is recommended when using the adjustable version, to improve the stability of the device. Please refer to the Recommended Operating conditions table for C_{FF} values.

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8.2.2 Application Curves

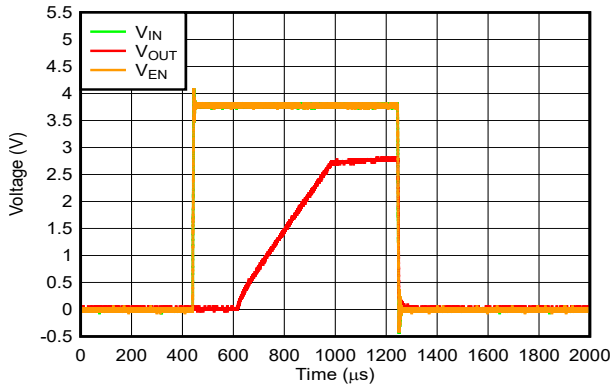


Figure 8-5. TPS794 Output Voltage, Enable Voltage vs Time (Start-Up)

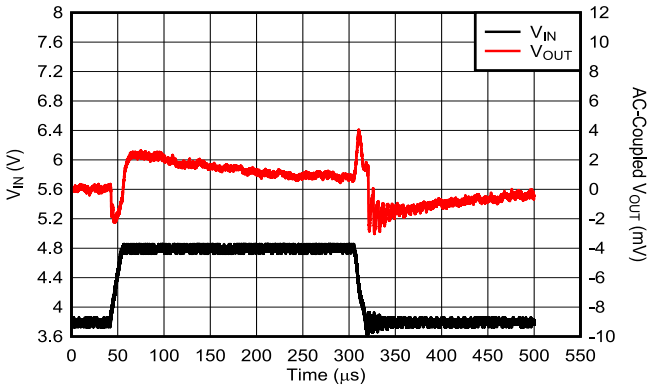


Figure 8-6. TPS794 Line Transient Response

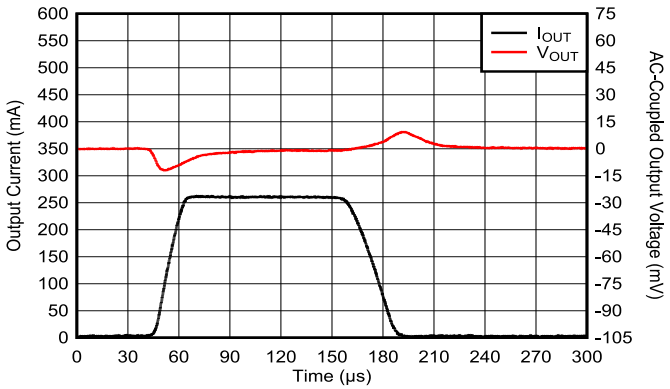


Figure 8-7. TPS794 Load Transient Response

8.3 Layout

8.3.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the ground pin of the device.

8.3.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}).

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package.
- T_A is the ambient temperature.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

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Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 5.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{5}$$

where

- P_D is the power dissipation shown by Equation 4.
- T_T is the temperature at the center-top of the IC package.
- T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface*.

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

8.3.3 Thermal Information

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power the regulator dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_D$max) consumed by a linear regulator is computed as shown in Equation 6:

$$P_D\,\text{max} = \left(V_{IN(avg)} - V_{OUT(avg)}\right) \times I_{OUT(avg)} + V_{I(avg)} \times I_Q \tag{6}$$

where:

- $V_{IN(avg)}$ is the average input voltage
- $V_{OUT(avg)}$ is the average output voltage
- $I_{OUT(avg)}$ is the average output current
- I_Q is the quiescent current

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)}$ x I_Q can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\Theta JC}$), the case to heatsink ($R_{\Theta CS}$), and the heatsink to ambient ($R_{\Theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 8-8 illustrates these thermal resistances for a SOT223 package mounted in a JEDEC low-K board.

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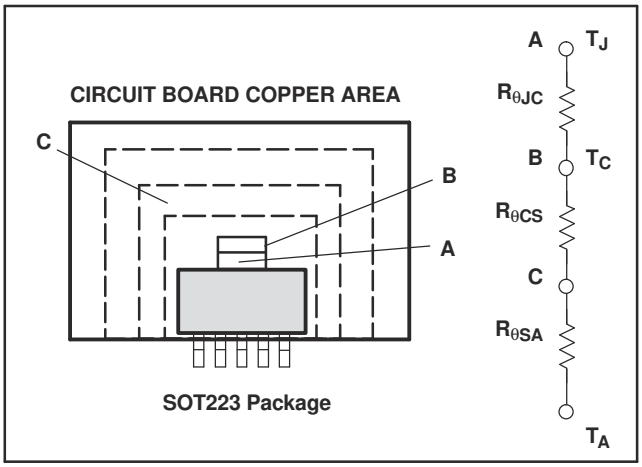


Figure 8-8. Thermal Resistances

Equation 7 summarizes the computation:

$$T_J = T_A + P_D max \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \quad (7)$$

The $R_{\Theta JC}$ is specific to each regulator as determined by the package, lead frame, and die size provided in the data sheet of the regulator. The $R_{\Theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\Theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\Theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\Theta CS}$ of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve the thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of the thermal performance of an integrated circuit in different operating environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, and more). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\Theta JA}$). This $R_{\Theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 7 simplifies into Equation 8:

$$T_J = T_A + P_D max \times R_{\theta JA} \quad (8)$$

Rearranging Equation 8 gives Equation 9:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \quad (9)$$

Using Equation 9 and the computer model generated curves shown in Figure 8-9, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

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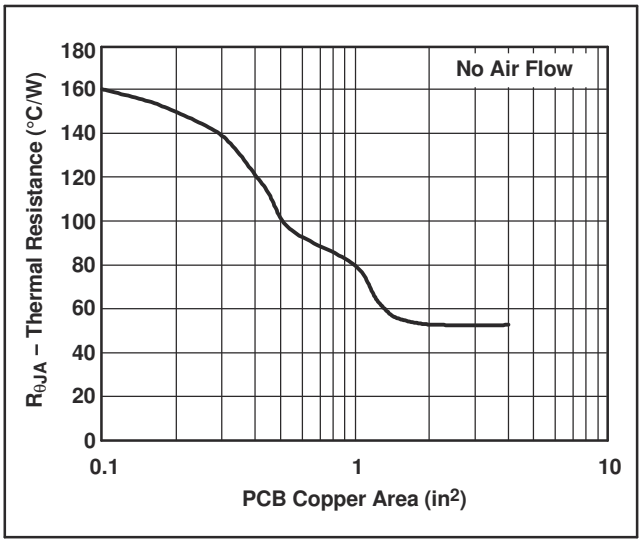


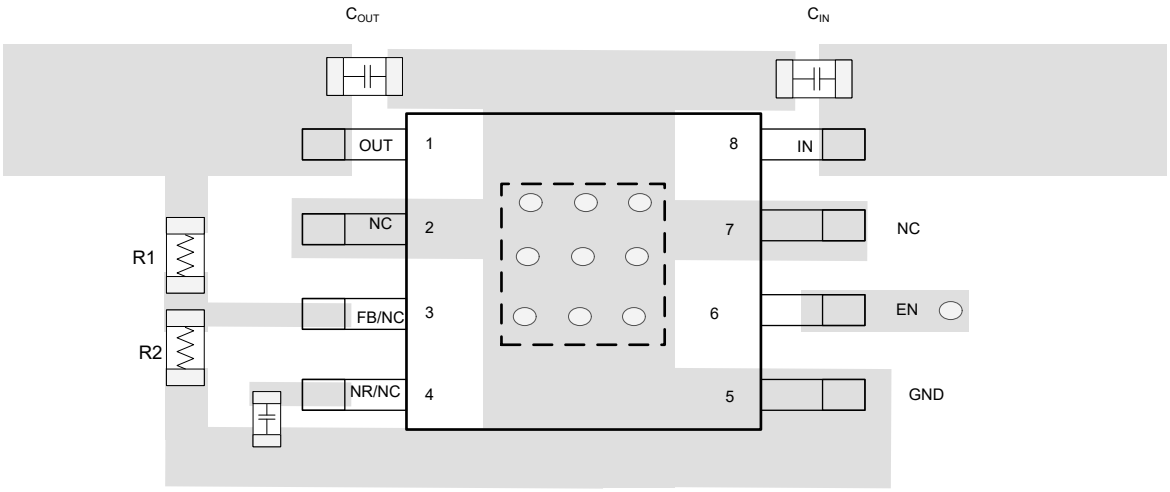
Figure 8-9. SOT223 Thermal Resistance vs PCB Copper Area

8.3.3.1 Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version must be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Note SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI web site (www.ti.com).

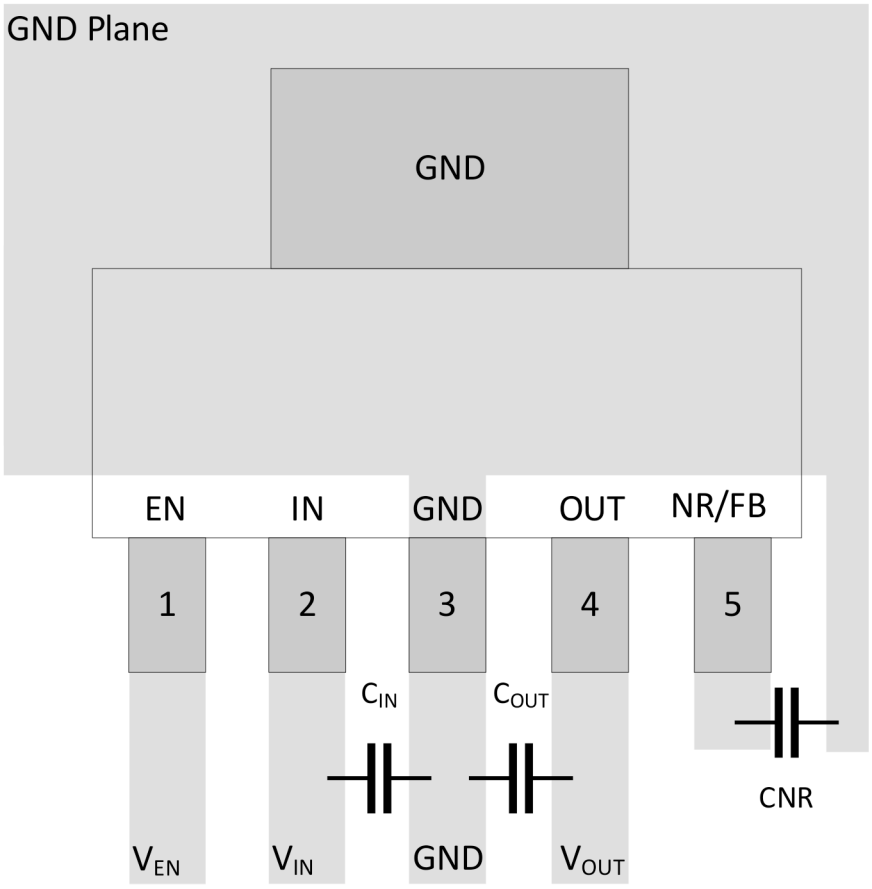
8.3.4 Layout Example



Notes:
- Not to scale
- Connect NC pins to GND for better thermal performance, or leave floating
- R_1 and R_2 only needed for adjustable operation
- NR capacitor can be left connected for new chip
- ○ Denotes a via to a connection made on another layer
- Add as many thermal vias as possible under thermal pad and nearby GND plane for better thermal performance

Figure 8-10. Layout Example (DGN Package)

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Notes:

Not to scale
Legacy chip only
Representative of the fixed output voltage options
Add as many thermal vias as possible under thermal pad and nearby GND plane for better thermal performance

Figure 8-11. Layout Example (DCQ Package)

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Available Options

PRODUCT(1)	DESCRIPTION(2)
TPS794**xx** ***yyy z*** **M3**	**xx** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **yyy** is package designator. **z** is package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 1.3V to 5.0V in 100mV increments are available; minimum order quantities can apply. Contact factory for details and availability.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2005) to Revision F (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added new silicon (M3) devices to the document	1
• Adding nomenclature distinguishing between new and legacy chip information throughout the document	1
• Adding portfolio device bullet to the *Features* section	1
• Changed MSOP to HVSSOP throughout document	1
• Added the *Applications* section	1
• Updated Pin Description table to include new chip and legacy chip descriptions	3
• Added description to look at TPS7A20 for lower noise performance	3
• Added NR/NC pin	3
• Added the *Recommended Operating Conditions* table	4
• Added the *Thermal Information* table	4
• Added the *ESD Ratings* table	4
• Updated the *Electrical Characteristics* table to include new chip and legacy chip specifications	4
• Added the *Device Functional Modes* section	18
• Added the *Application and Implementation* section	20
• Added the *Layout* section	25
• Added the *Device and Documentation Support* section	30
• Added the *Mechanical, Packaging and Orderable Information* section	32

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79401DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 85	PS79401
TPS79401DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79401
TPS79401DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79401
TPS79401DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag | Nipdau	Level-1-260C-UNLIM	-40 to 85	AXL
TPS79401DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	AXL
TPS79401DGNRM3	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXL
TPS79401DGNT	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	AXL
TPS79418DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 85	PS79418
TPS79418DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79418
TPS79418DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79418
TPS79418DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 85	AXM
TPS79418DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	AXM
TPS79418DGNT	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	AXM
TPS79425DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 85	PS79425
TPS79425DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79425
TPS79425DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79425
TPS79425DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 85	AYB
TPS79425DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	AYB
TPS79425DGNT	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	AYB
TPS79428DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 85	PS79428
TPS79428DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79428
TPS79428DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79428
TPS79428DGNT	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYC
TPS79428DGNT.A	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYC
TPS79430DCQ	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79430
TPS79430DCQ.A	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79430
TPS79430DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79430
TPS79430DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79430

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79430DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYD
TPS79430DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYD
TPS79430DGNT	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	AYD
TPS79433DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 85	PS79433
TPS79433DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79433
TPS79433DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79433
TPS79433DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYE
TPS79433DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYE
TPS79433DGNT	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	AYE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

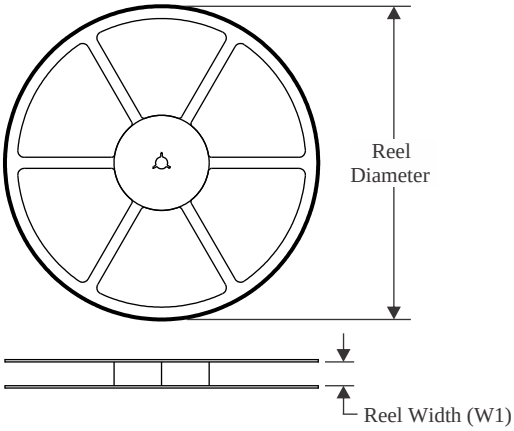
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

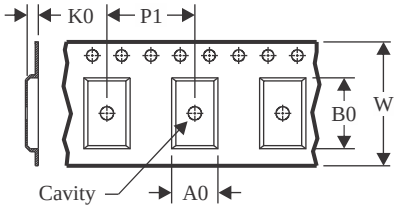
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

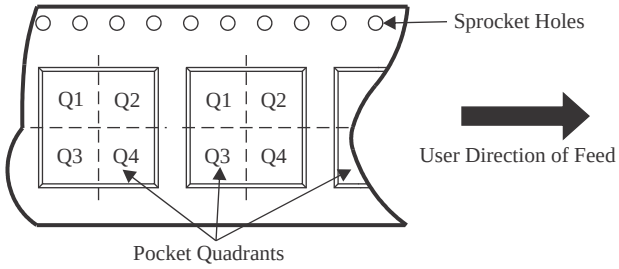


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

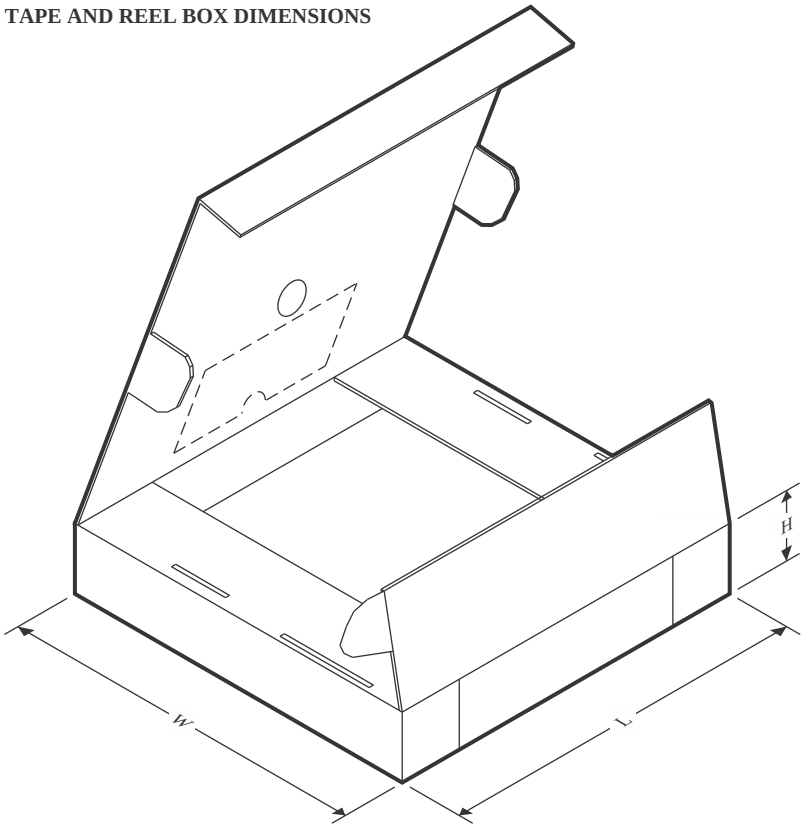
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79401DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79401DGNRM3	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79418DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79418DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79425DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79425DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79428DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79428DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79430DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79430DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79433DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79433DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

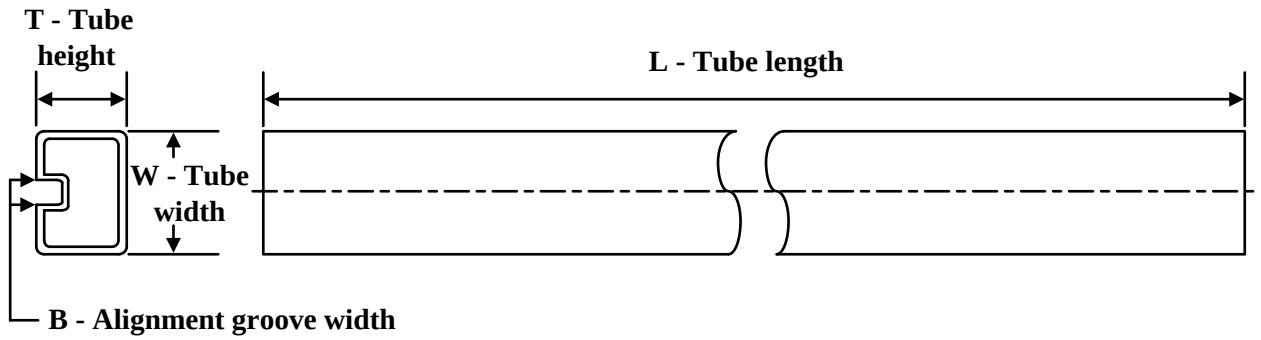
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79401DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79401DGNRM3	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS79418DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS79418DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS79425DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS79425DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS79428DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79428DGNT	HVSSOP	DGN	8	250	213.0	191.0	35.0
TPS79430DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79430DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS79433DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79433DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

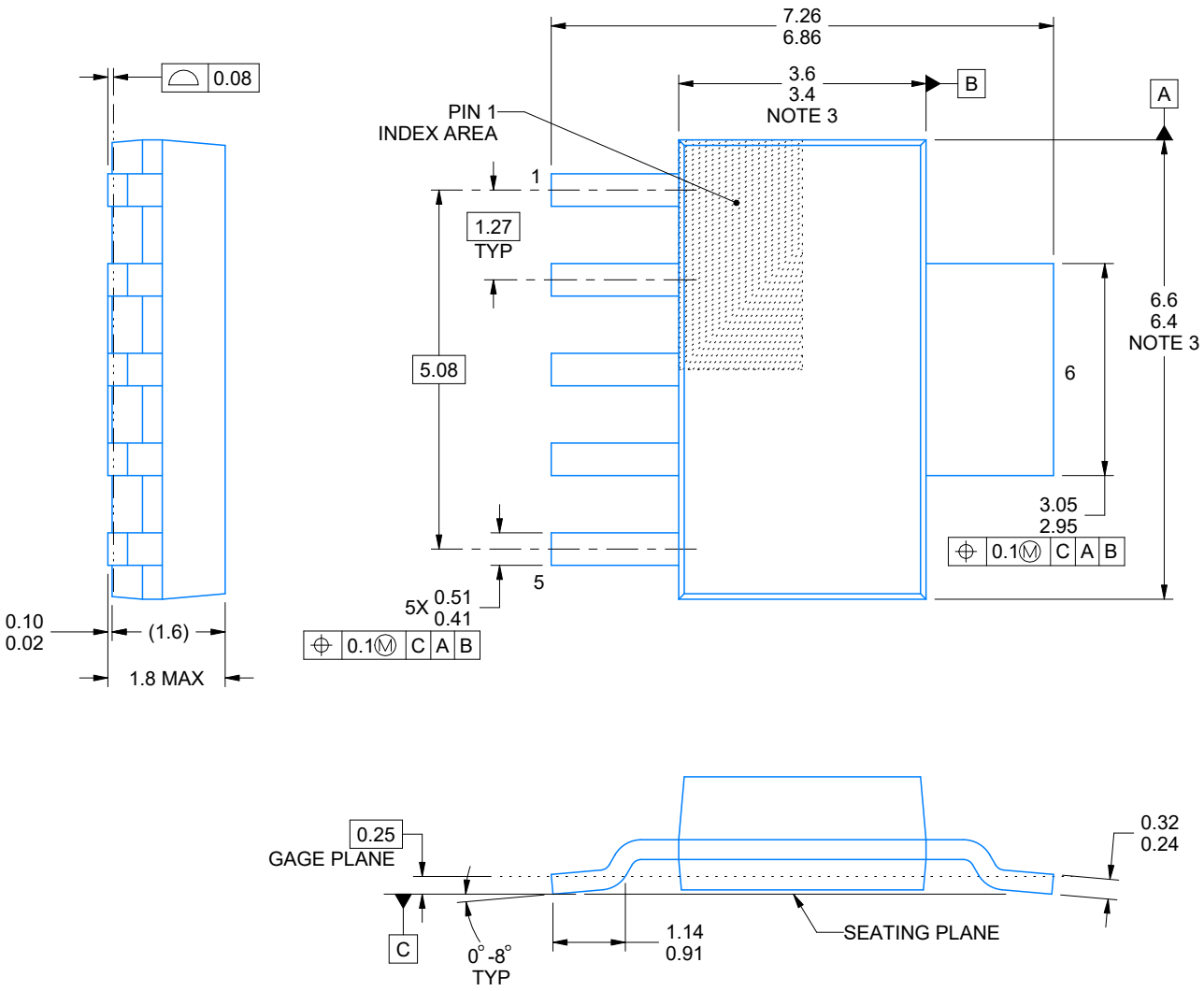
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS79430DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79430DCQ.A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

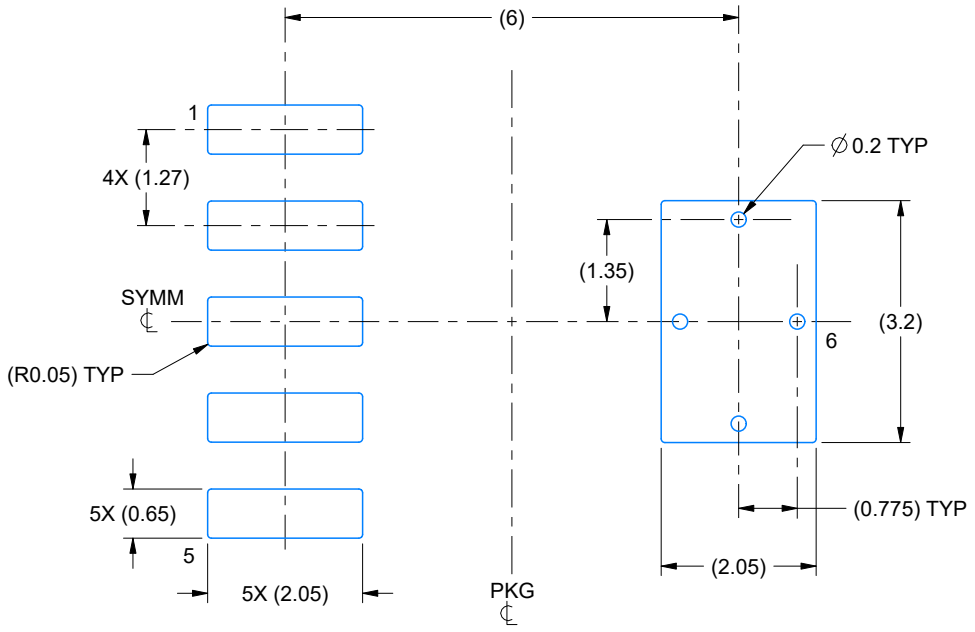
PLASTIC SMALL OUTLINE



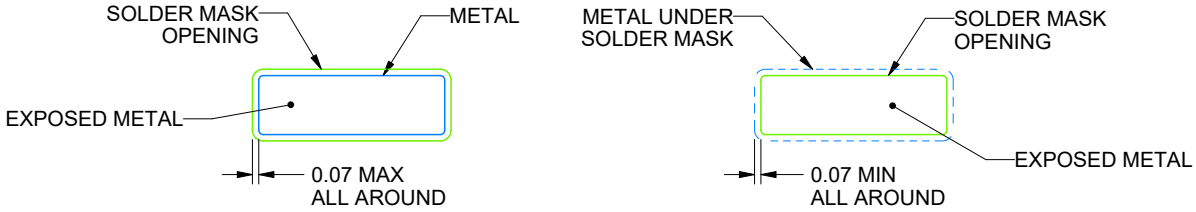
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

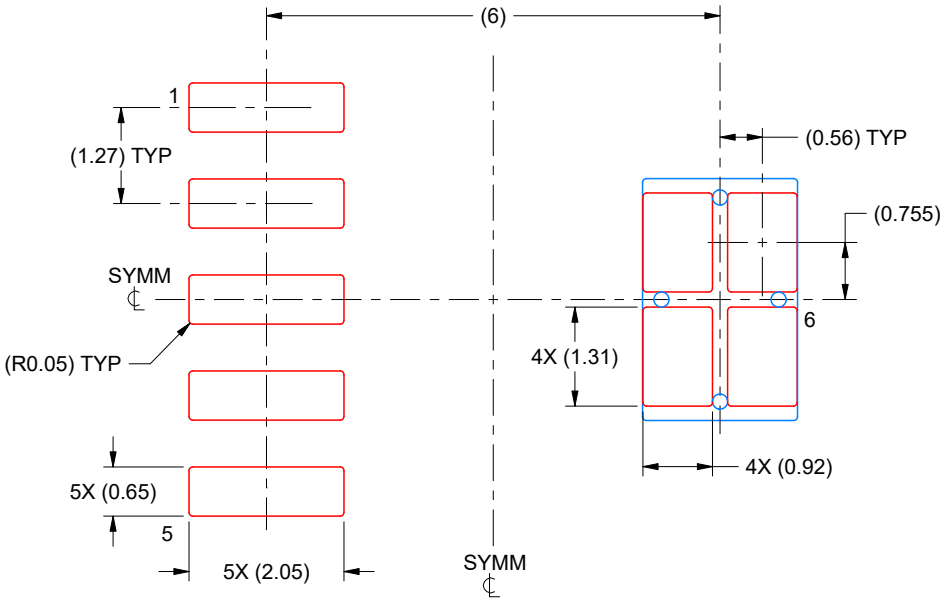


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

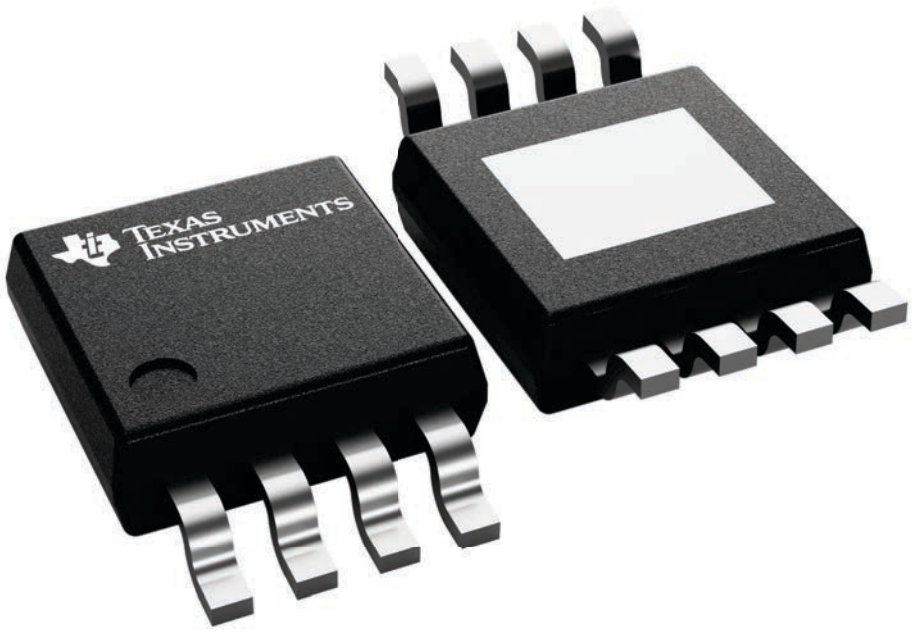
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

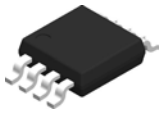
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

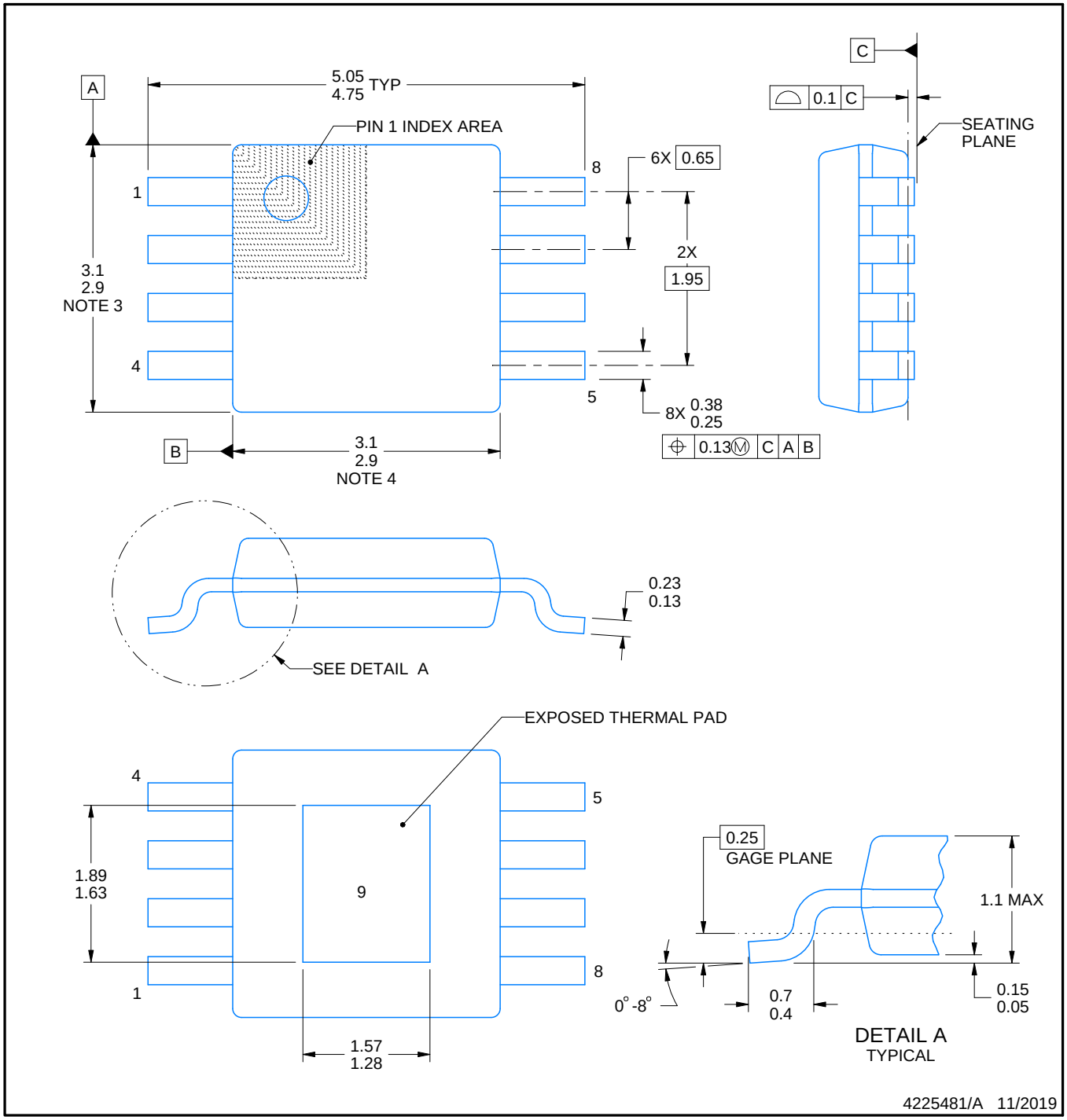
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

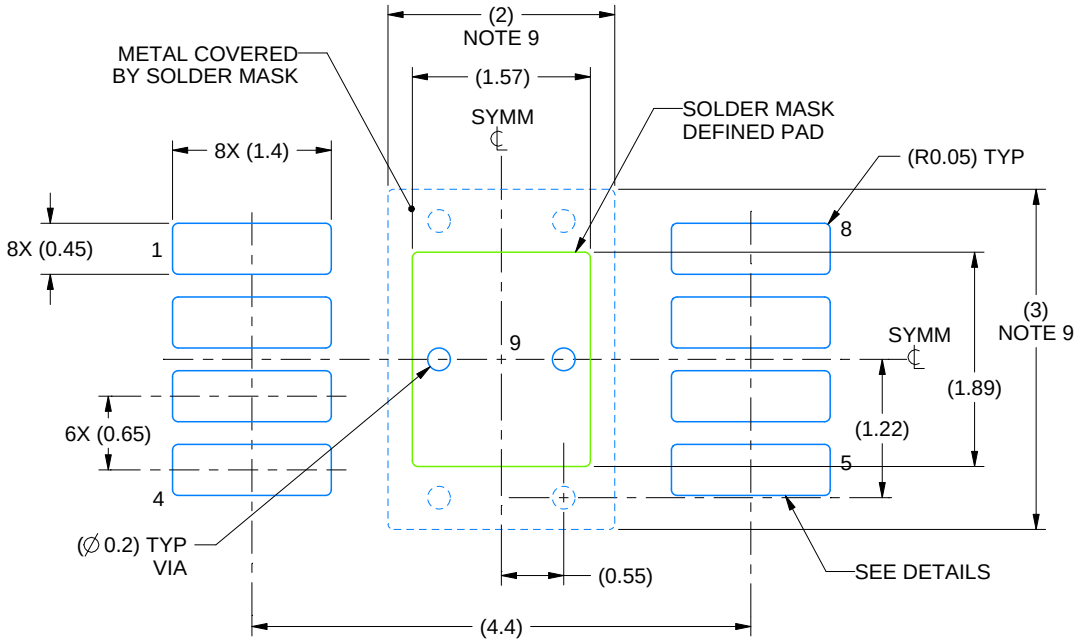
SMALL OUTLINE PACKAGE



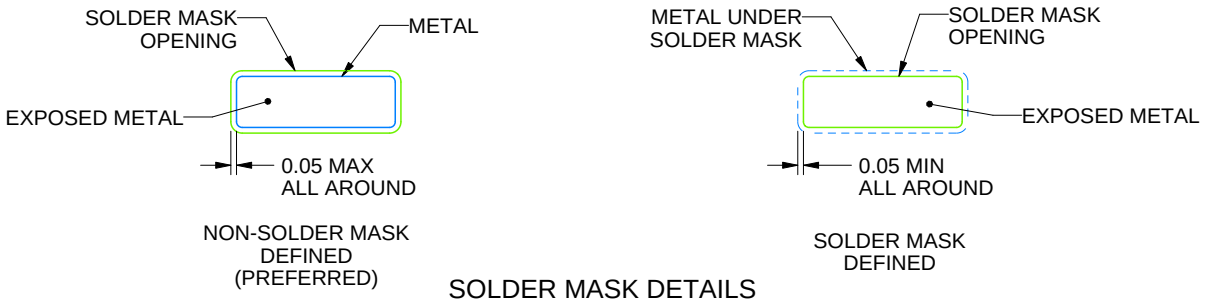
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

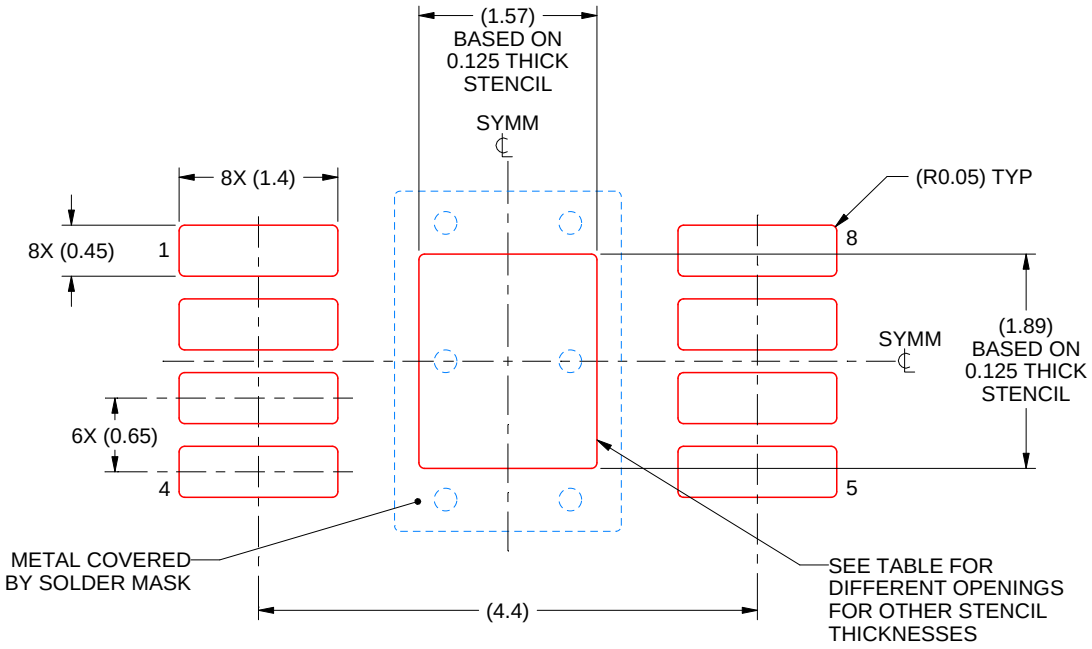


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

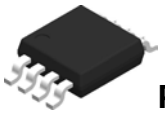
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

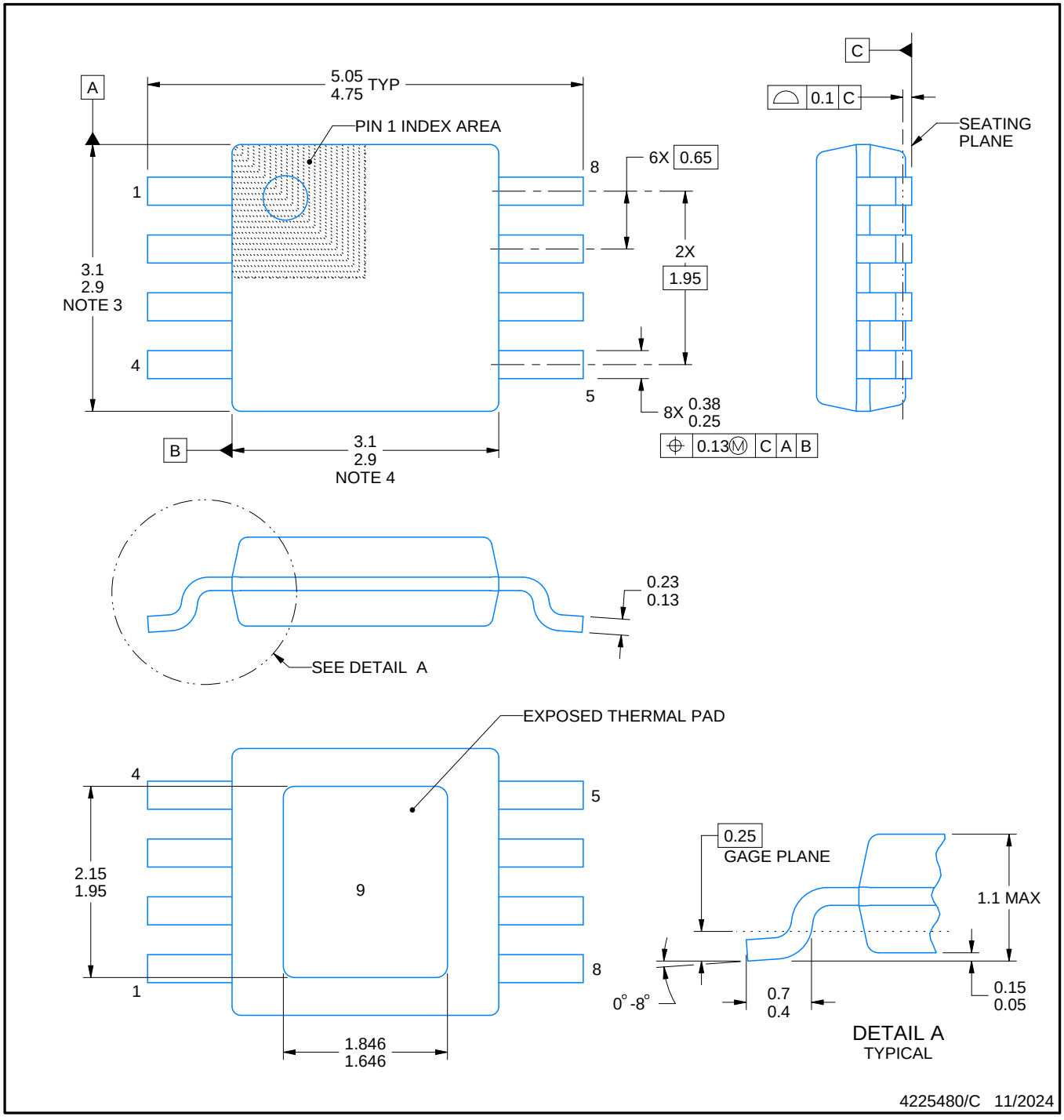
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

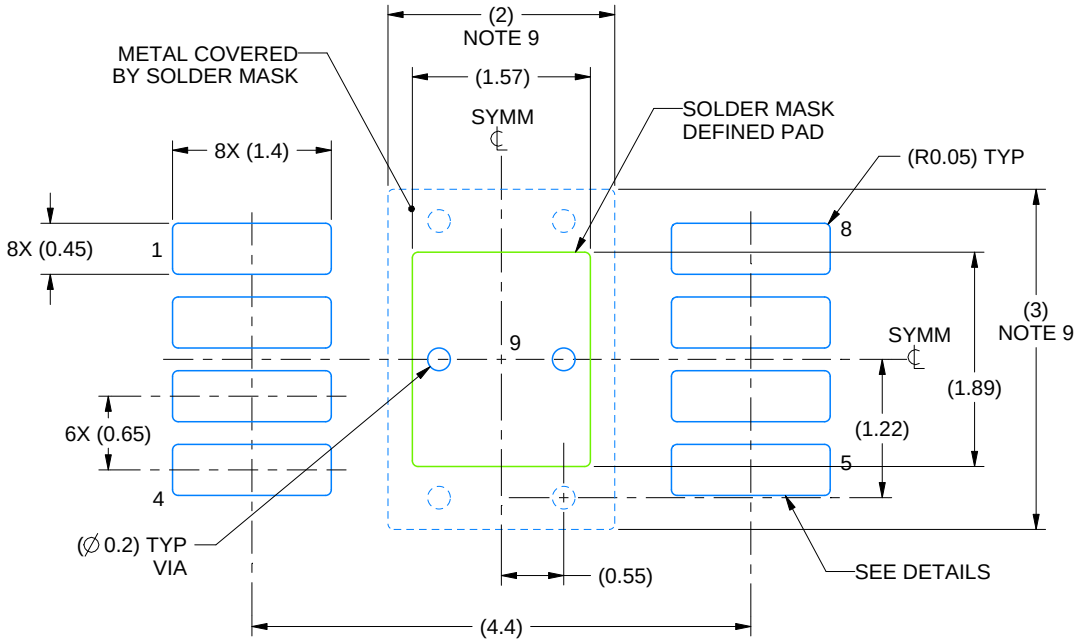
SMALL OUTLINE PACKAGE



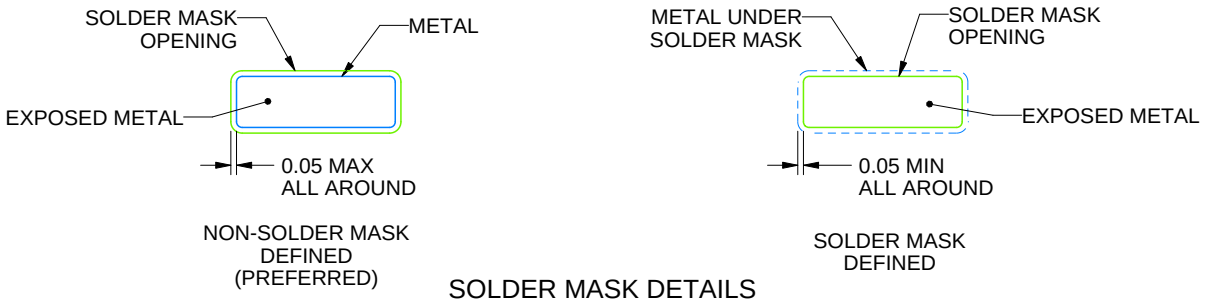
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

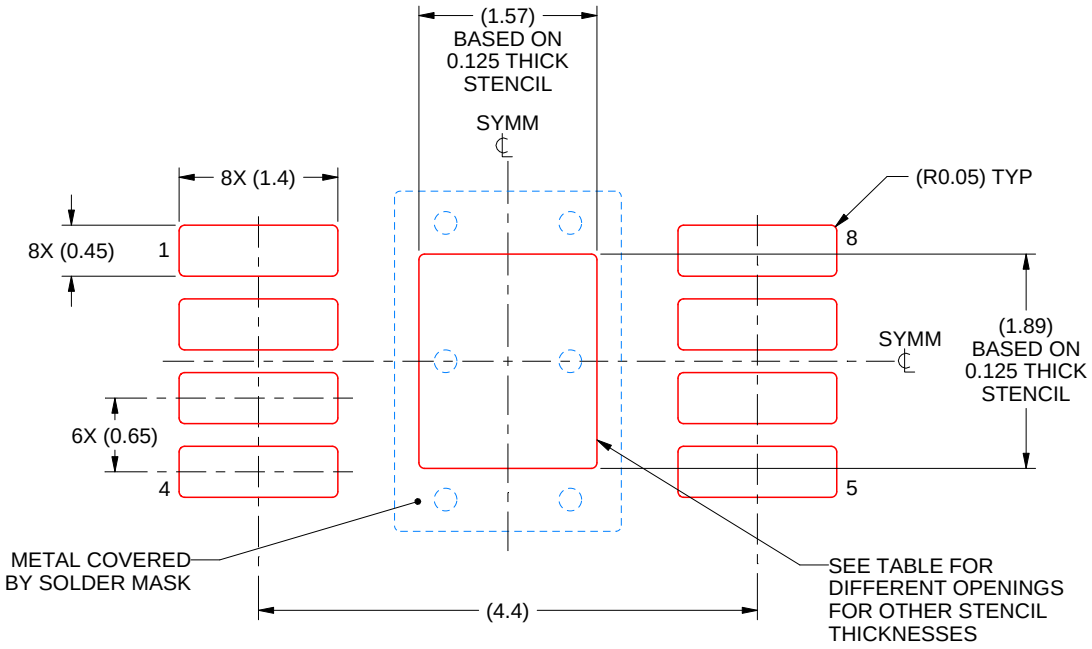


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

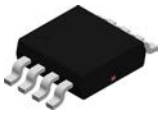
4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

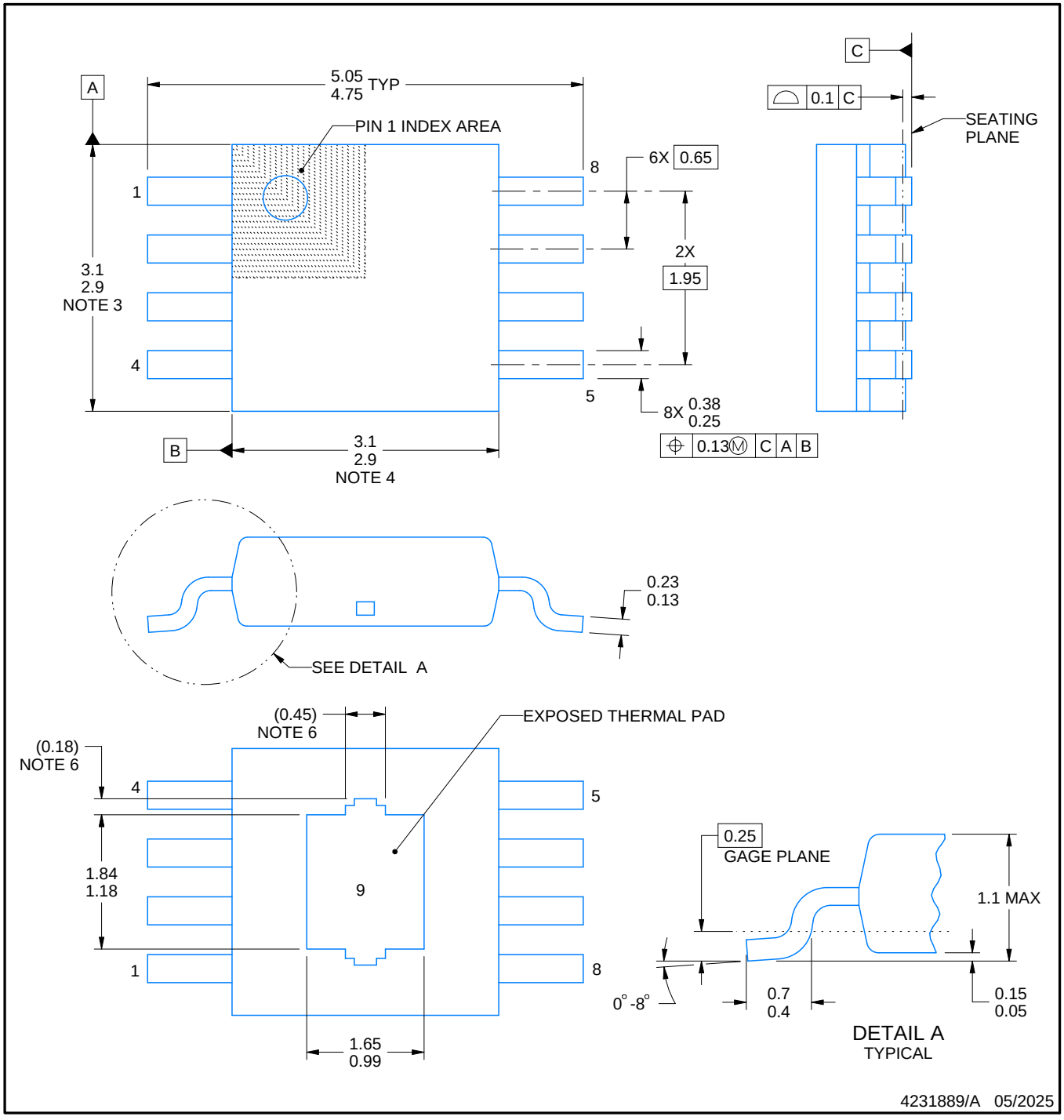
PACKAGE OUTLINE

DGN0008K



PowerPAD™ VSSOP - 1.1 mm max height

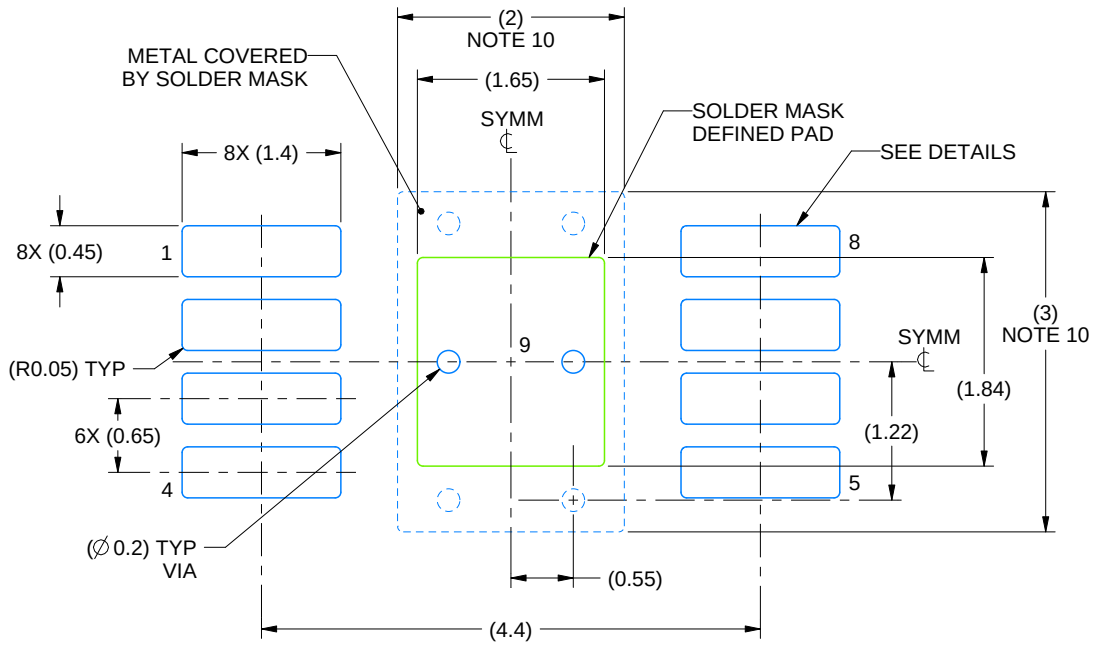
SMALL OUTLINE PACKAGE



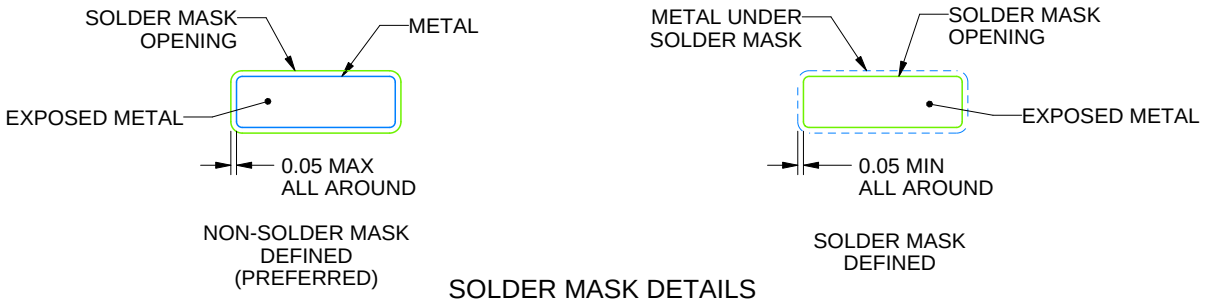
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

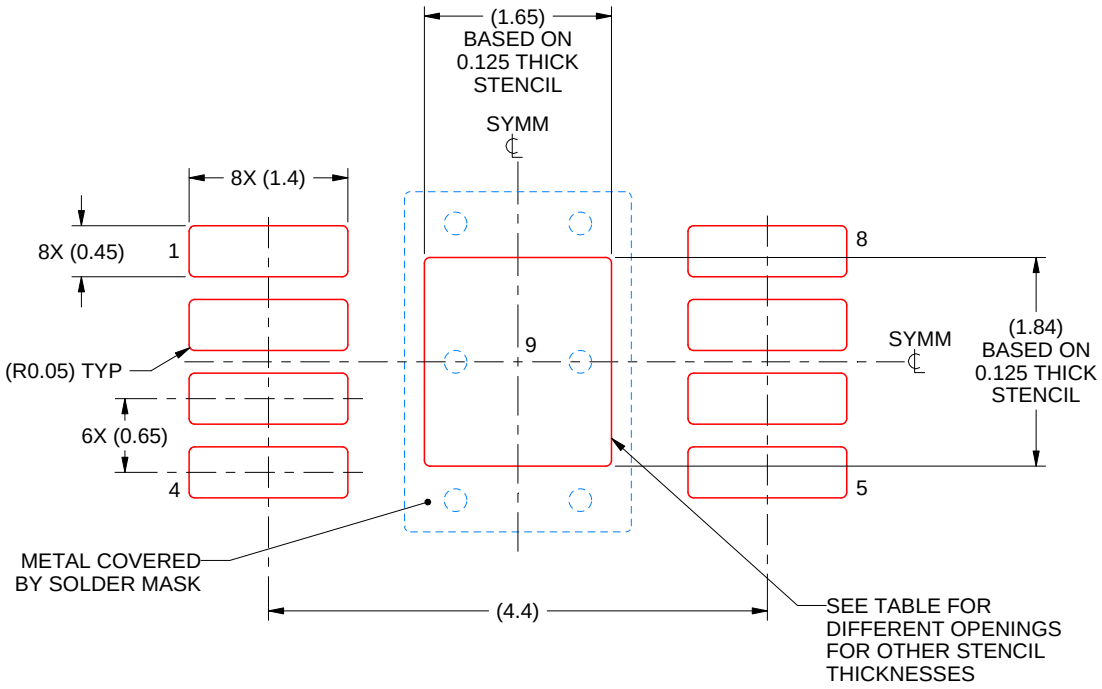


SOLDER MASK DETAILS

4231889/A 05/2025

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 2.06
0.125	1.65 X 1.84 (SHOWN)
0.15	1.51 X 1.68
0.175	1.39 X 1.56

4231889/A 05/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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