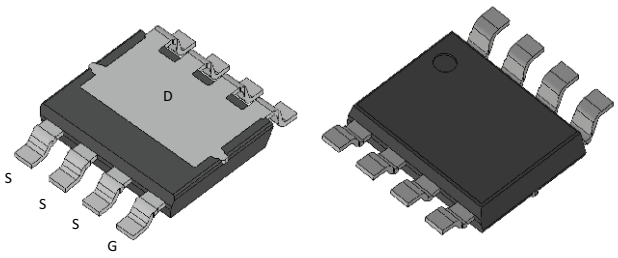
Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8L Reverse Single



Top View

Bottom View

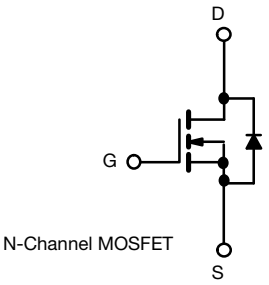
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	80
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0014
I_D (A)	430
Configuration	Single
Package	PowerPAK 8 x 8L Reverse

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	80	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C = 25 °C	I_D	430	A
	T_C = 125 °C		250	
Continuous source current (diode conduction)		I_S	450	
Pulsed drain current [a]		I_{DM}	1200	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	65	
Single pulse avalanche energy		E_{AS}	211	mJ
Maximum power dissipation	T_C = 25 °C	P_D	600	W
	T_C = 125 °C		200	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [b]	R_{thJA}	40	°C/W
Junction-to-case (drain)		R_{thJC}	0.25	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. When mounted on 1" square PCB (FR4 material)

c. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		80	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2	3	3.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 80 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 80 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 80 V, T_J = 175 °C	-	-	500	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	50	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A	-	0.0012	0.0014	Ω
		V_{GS} = 10 V	I_D = 20 A, T_J = 125 °C	-	-	0.00281	
		V_{GS} = 10 V	I_D = 20 A, T_J = 175 °C	-	-	0.0037	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		-	82	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	11 435	16 009	pF
Output capacitance	C_{oss}			-	1896	2655	
Reverse transfer capacitance	C_{rss}			-	92	129	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 40 V, I_D = 10 A	-	183	240	nC
Gate-source charge [c]	Q_{gs}			-	47	-	
Gate-drain charge [c]	Q_{gd}			-	36	-	
Gate resistance	R_g	f = 1 MHz		0.7	1.3	2	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 0.8 Ω I_D ≅ 50 A, V_{GEN} = 10 V, R_g = 1 Ω		-	21	28	ns
Rise time [c]	t_r			-	80	105	
Turn-off delay time [c]	$t_{d(off)}$			-	65	85	
Fall time [c]	t_f			-	20	28	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	1100	A
Forward voltage	V_{SD}	I_F = 40 A, V_{GS} = 0 V		-	0.7	1.2	V

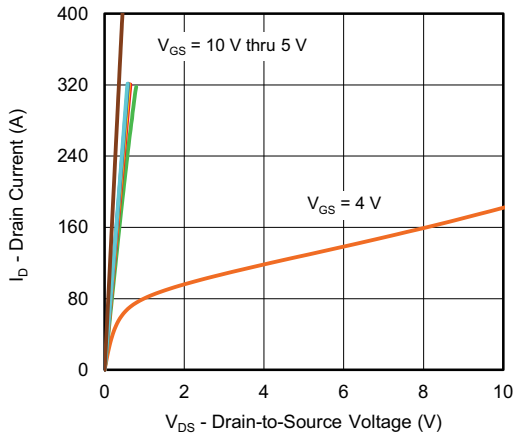
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

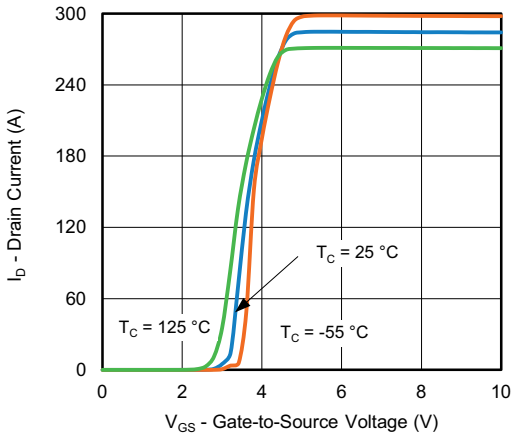
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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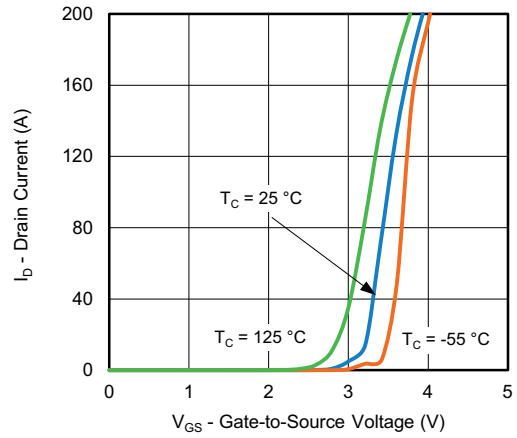
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



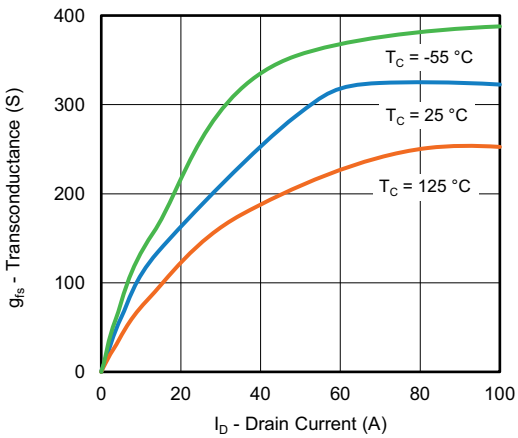
Output Characteristics



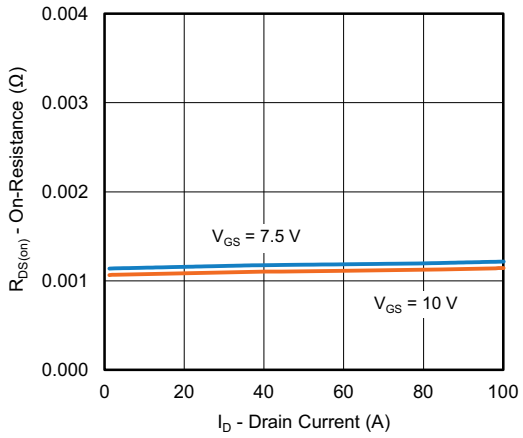
Transfer Characteristics



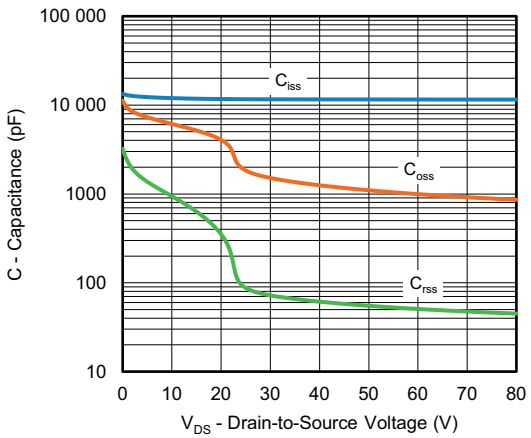
Transfer Characteristics



Transconductance



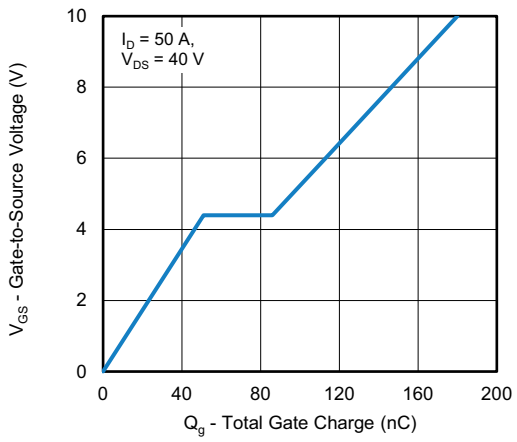
On-Resistance vs. Drain Current



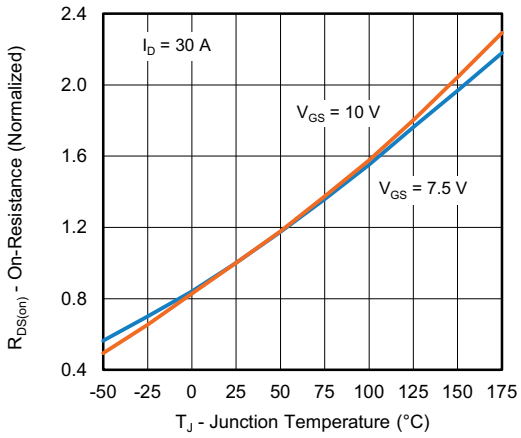
Capacitance

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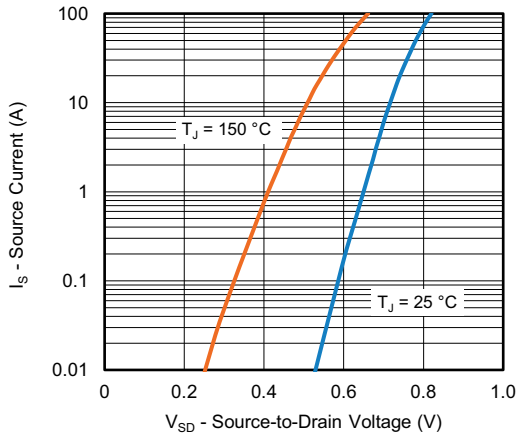
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



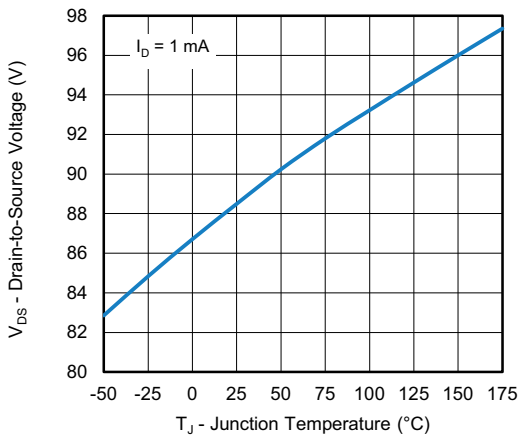
Gate Charge



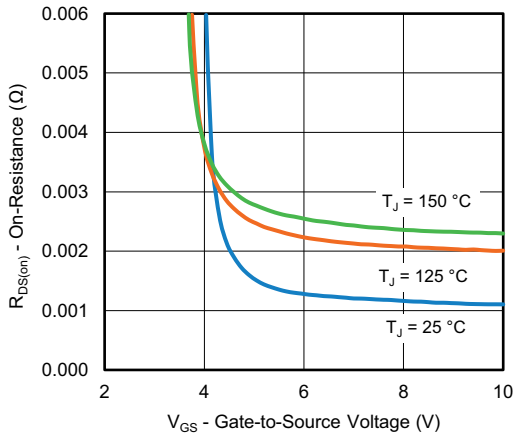
On-Resistance vs. Junction Temperature



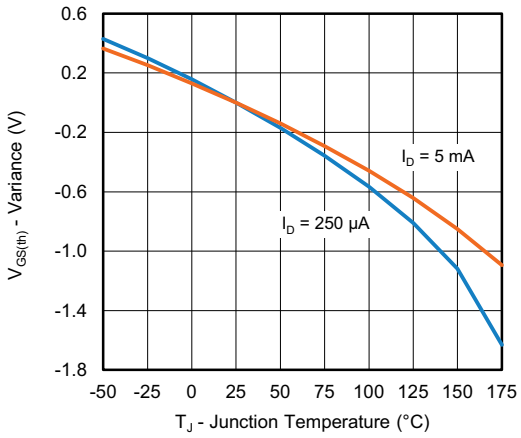
Source Drain Diode Forward Voltage



Drain Source Breakdown vs. Junction Temperature



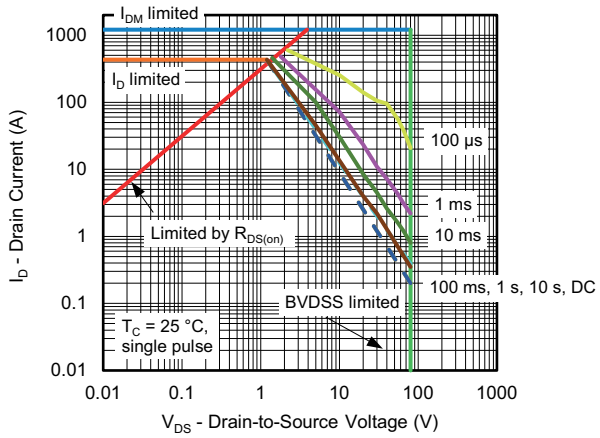
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

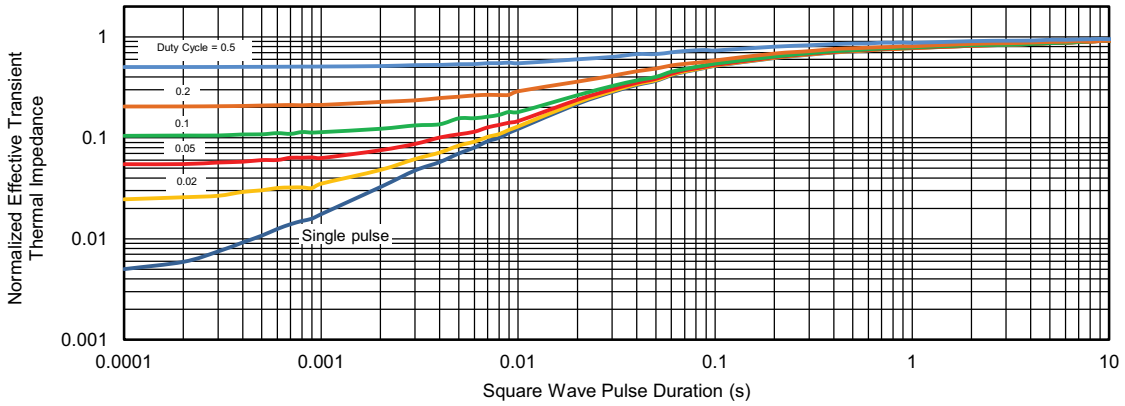
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Safe Operating Area

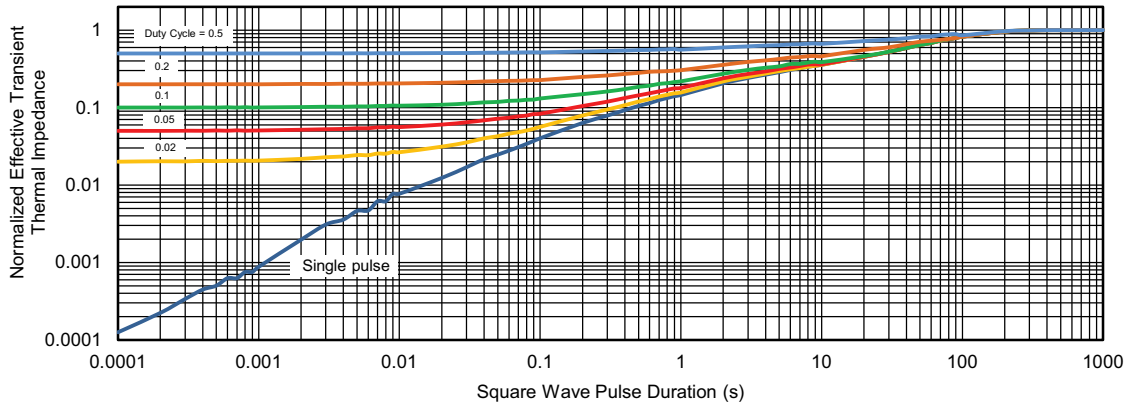
THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

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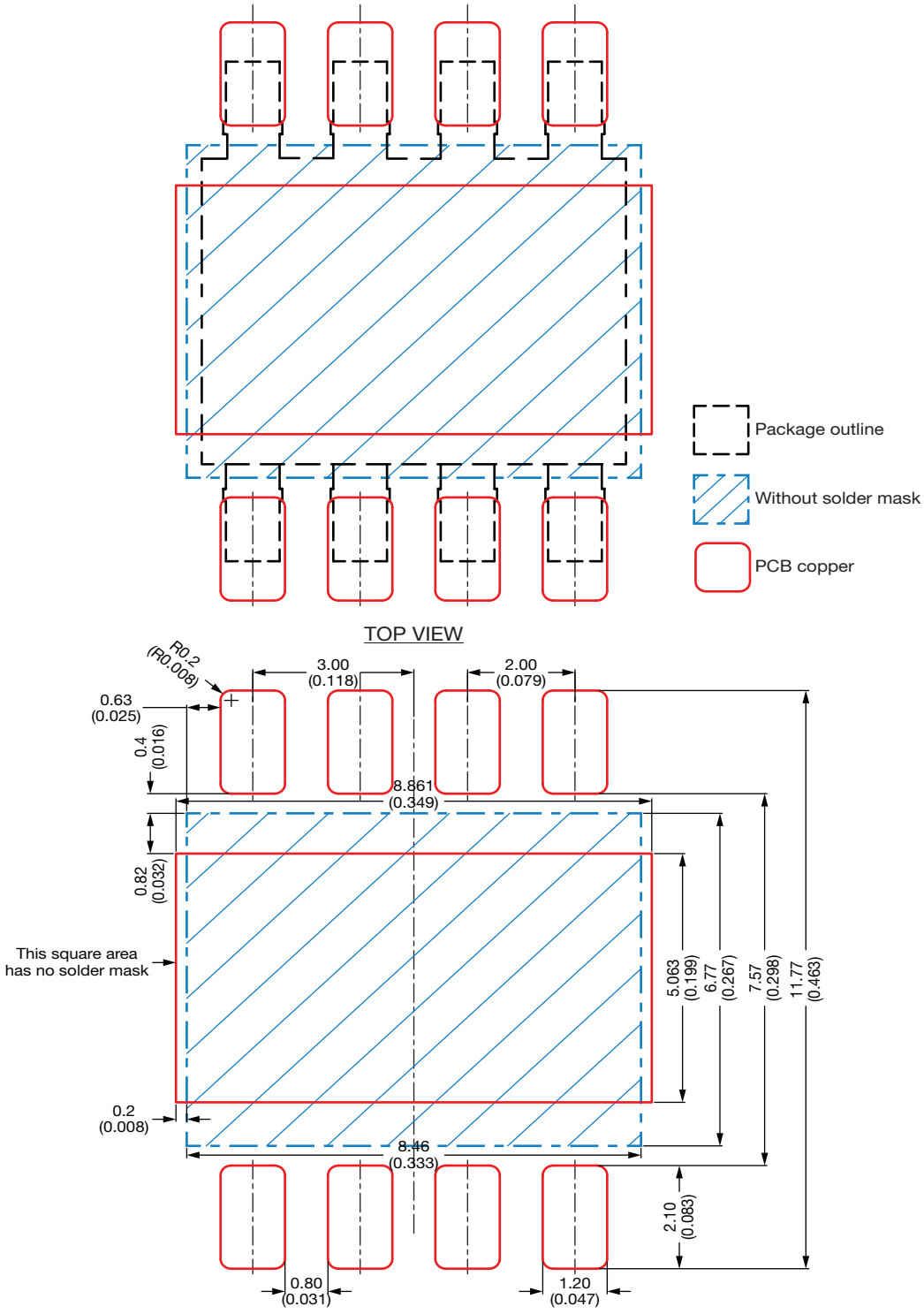


Normalized Thermal Transient Impedance, Junction-to-Ambient

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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023
DWG: 3002

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