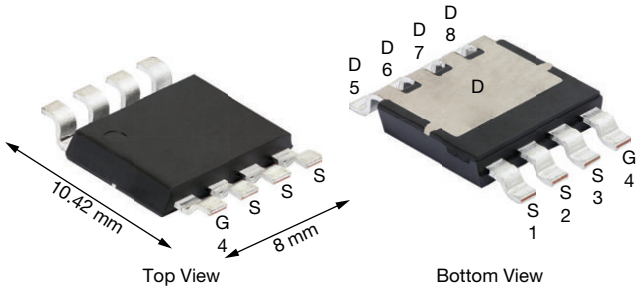
Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8LR



Top View Bottom View

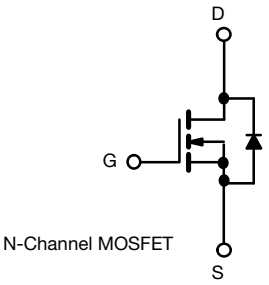
FEATURES

- TrenchFET® Gen V power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.00186
I_D (A) [e]	225
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ510ER (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [e]	T_C = 25 °C	I_D	225	A
	T_C = 125 °C		130	
Continuous source current (diode conduction) [e]		I_S	130	
Pulsed drain current [a, e]		I_{DM}	700	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	73	
Single pulse avalanche energy		E_{AS}	266	mJ
Maximum power dissipation [c, e]	T_C = 25 °C	P_D	214	W
	T_C = 125 °C		71	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [b]	R_{thJA}	40	°C/W
Junction-to-case (drain) [d]		R_{thJC}	0.7	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. When mounted on 1" square PCB (FR4 material)
c. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
d. As per JESD51-14
e. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		100	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.3	2.8	3.3	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 100 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 175 °C	-	-	500	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	50	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A	-	0.0015	0.00186	Ω
		V_{GS} = 10 V	I_D = 20 A, T_J = 125 °C	-	-	0.0033	
		V_{GS} = 10 V	I_D = 20 A, T_J = 175 °C	-	-	0.0043	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 25 A		-	100	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	7776	10 887	pF
Output capacitance	C_{oss}			-	3655	5117	
Reverse transfer capacitance	C_{rss}			-	42	59	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 50 V, I_D = 50 A	-	88	132	nC
Gate-source charge [c]	Q_{gs}			-	41	-	
Gate-drain charge [c]	Q_{gd}			-	4	-	
Gate resistance	R_g	f = 1 MHz		0.4	1.8	3.6	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 1 Ω		-	19	29	ns
Rise time [c]	t_r			-	12	18	
Turn-off delay time [c]	$t_{d(off)}$			-	39	59	
Fall time [c]	t_f			-	10	15	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	520	A
Forward voltage	V_{SD}	I_F = 40 A, V_{GS} = 0 V		-	0.7	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 15 A, di/dt = 100 A/µs		-	100	200	ns
Body diode reverse recovery charge	Q_{rr}			-	224	448	nC
Reverse recovery fall time	t_a			-	57	-	ns
Reverse recovery rise time	t_b			-	43	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-3.8	-	A

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

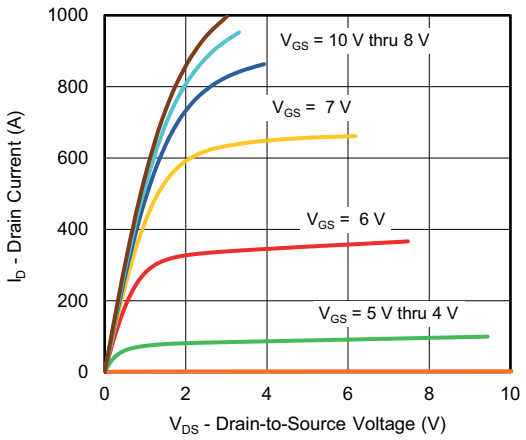
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

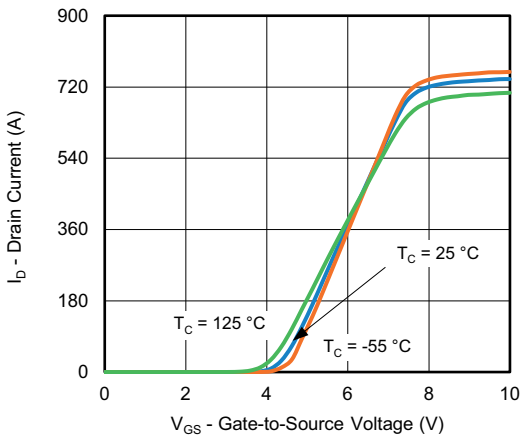
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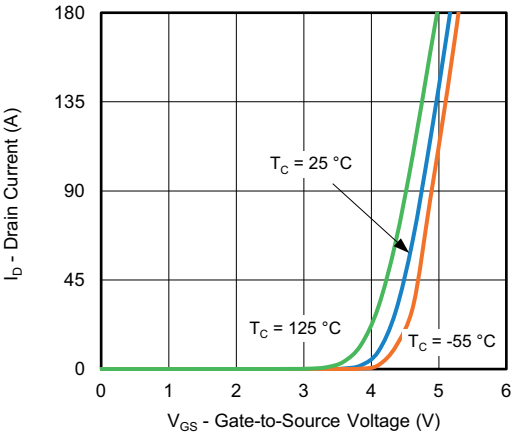
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



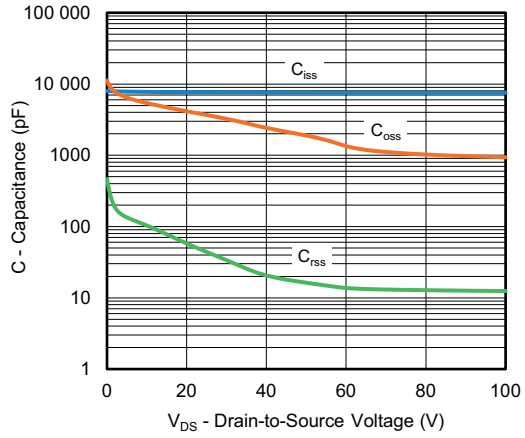
Output Characteristics



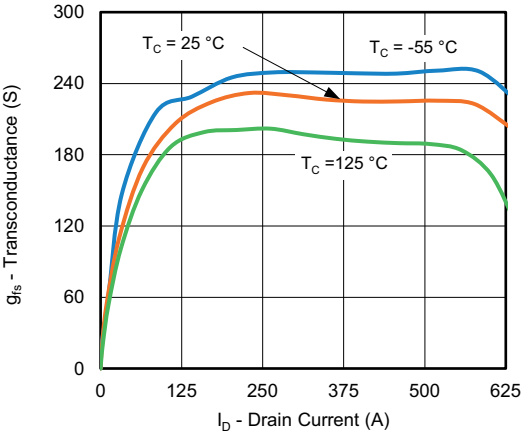
Transfer Characteristics



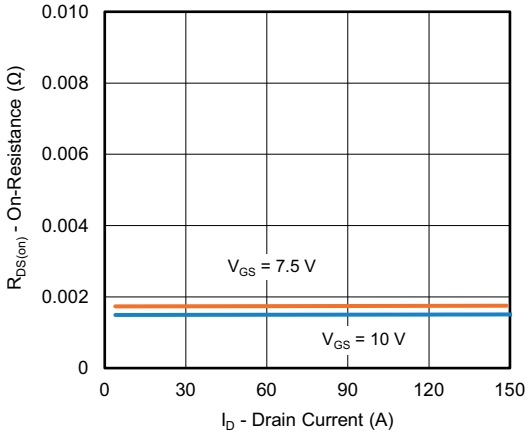
Transfer Characteristics



Capacitance



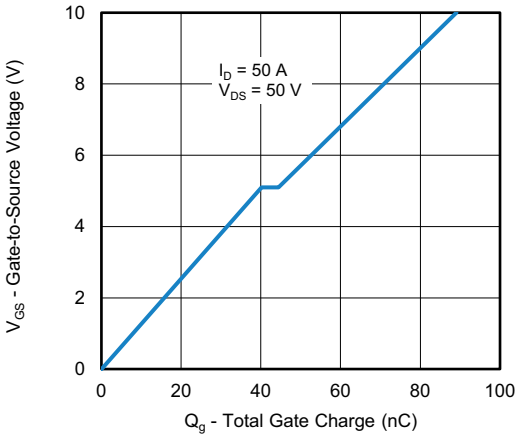
Transconductance



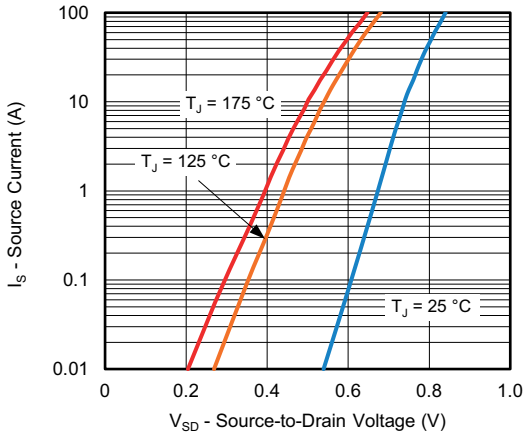
On-Resistance vs. Drain Current

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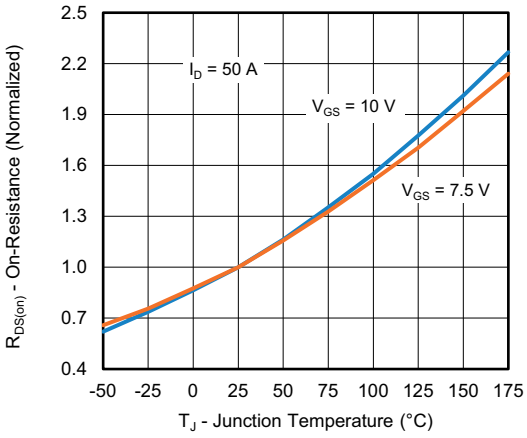
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



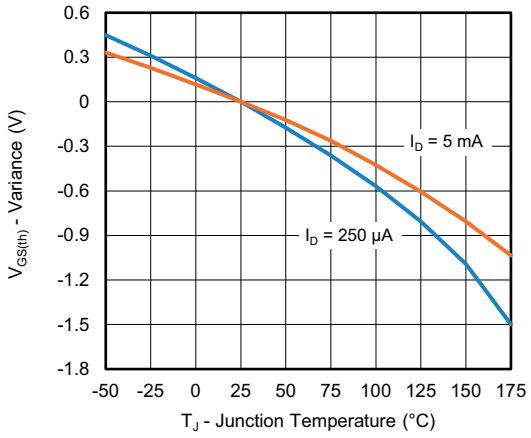
Gate Charge



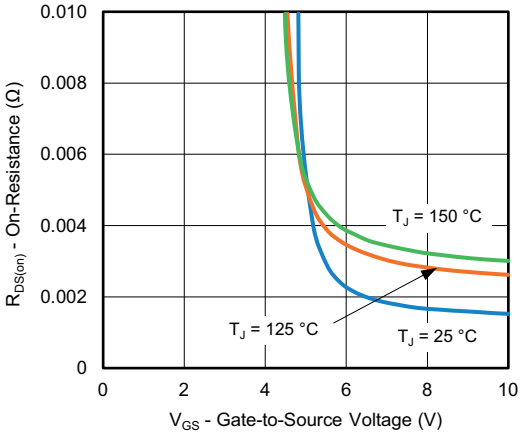
Source Drain Diode Forward Voltage



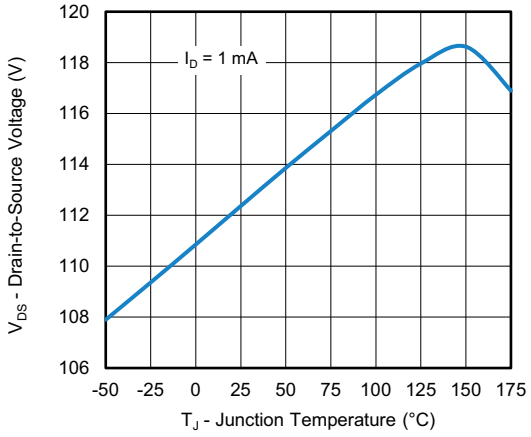
On-Resistance vs. Junction Temperature



Threshold Voltage



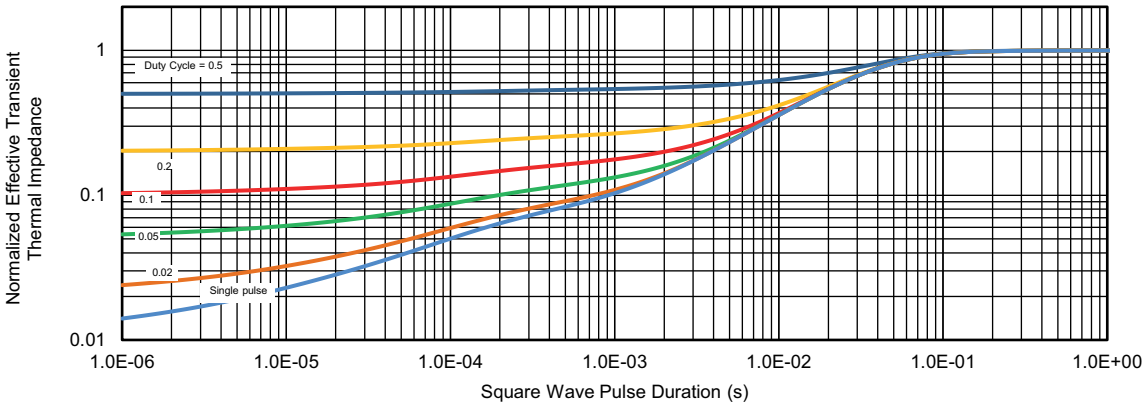
On-Resistance vs. Gate-to-Source Voltage



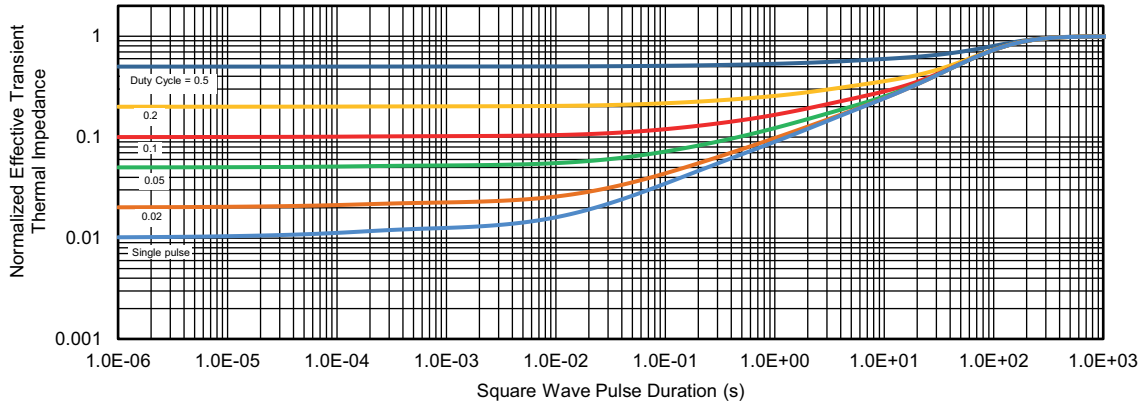
Drain Source Breakdown vs. Junction Temperature

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

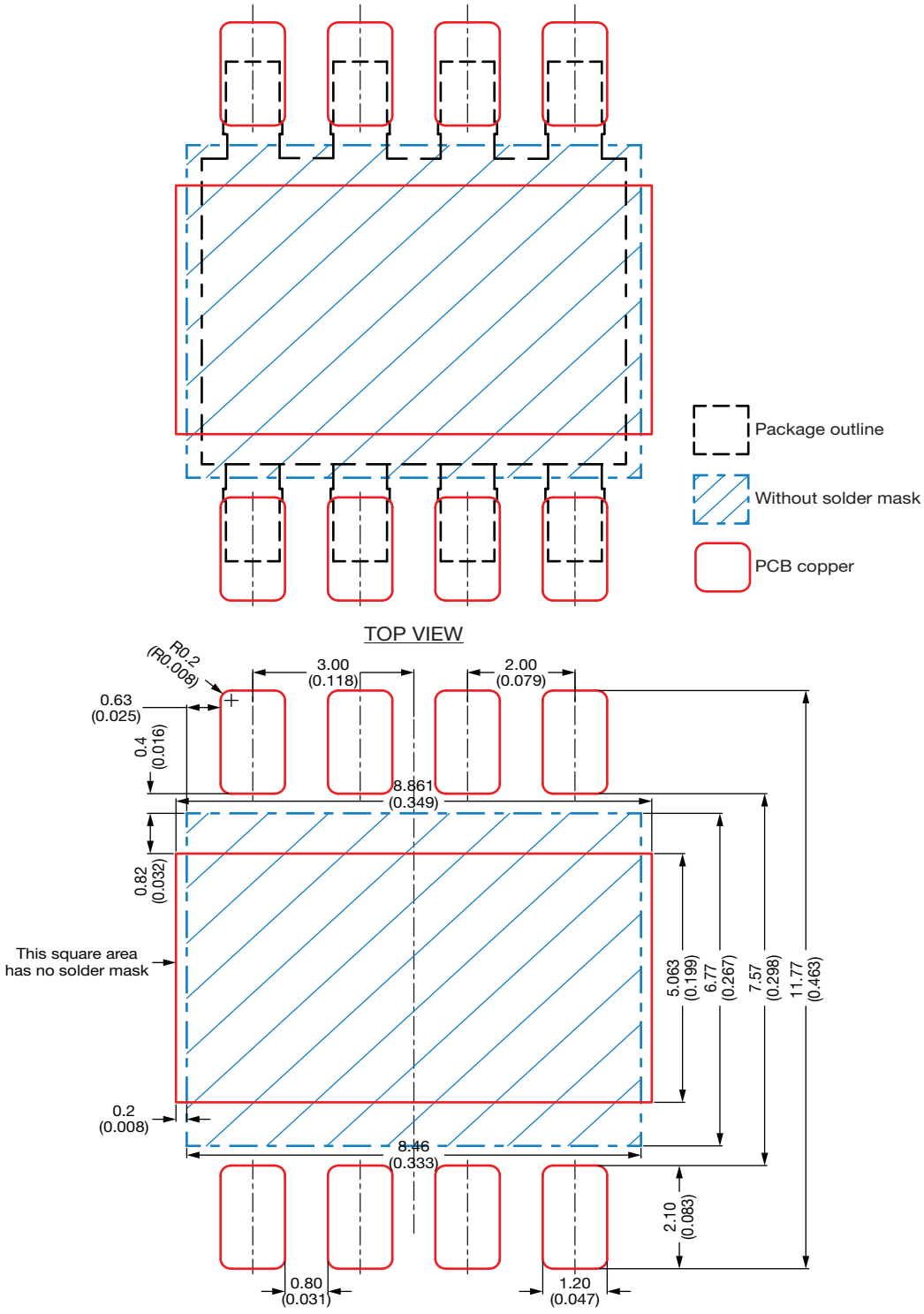


Normalized Thermal Transient Impedance, Junction-to-Ambient

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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023
DWG: 3002

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