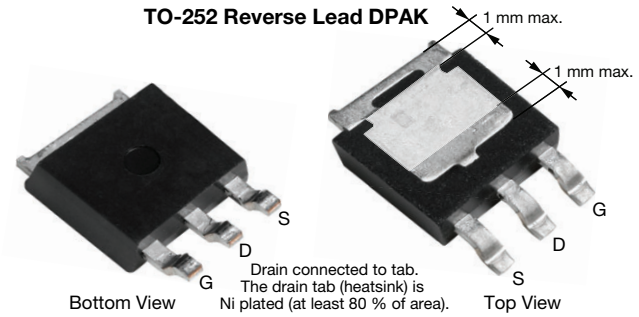
Automotive N-Channel 40 V (D-S) 175 °C MOSFET



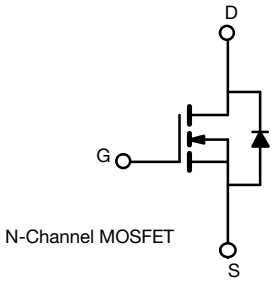
FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- Ni plated drain tab area (heatsink) for top side cooling
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.00233
I_D (A)	100
Configuration	Single
Package	TO-252 reverse lead DPAK

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C = 25 °C [a]	I_D	100	A
	T_C = 125 °C		87.5	
Continuous source current (diode conduction)		I_S	97	
Pulsed drain current [b]		I_{DM}	280	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	46	
Single pulse avalanche energy		E_{AS}	105.8	mJ
Maximum power dissipation [b]	T_C = 25 °C	P_D	107	W
	T_C = 125 °C		35	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	50	°C/W
Junction-to-case (drain)		R_{thJC}	1.4	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.5	3.0	3.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	500	µA
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	50	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A	-	0.00190	0.00233	Ω
		V_{GS} = 10 V	I_D = 20 A, T_J = 125 °C	-	-	0.00390	
		V_{GS} = 10 V	I_D = 20 A, T_J = 175 °C	-	-	0.00470	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		-	84	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	5405	8000	pF
Output capacitance	C_{oss}			-	1942	2700	
Reverse transfer capacitance	C_{rss}			-	175	250	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 50 A	-	84	130	nC
Gate-source charge [c]	Q_{gs}			-	29.5	-	
Gate-drain charge [c]	Q_{gd}			-	19.5	-	
Gate resistance	R_g	f = 1 MHz		1	2	3	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.4 Ω I_D ≅ 50 A, V_{GEN} = 10 V, R_g = 1 Ω		-	17	30	ns
Rise time [c]	t_r			-	17	30	
Turn-off delay time [c]	$t_{d(off)}$			-	34	60	
Fall time [c]	t_f			-	18	35	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	280	A
Forward voltage	V_{SD}	I_F = 25 A, V_{GS} = 0 V		-	0.8	1.5	V
Body diode reverse recovery time	t_{rr}	I_F = 50 A, di/dt = 100 A/µs		-	41	85	ns
Body diode reverse recovery charge	Q_{rr}			-	28	60	nC
Reverse recovery fall time	t_a			-	24	-	ns
Reverse recovery rise time	t_b			-	17	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-1.36	-	A

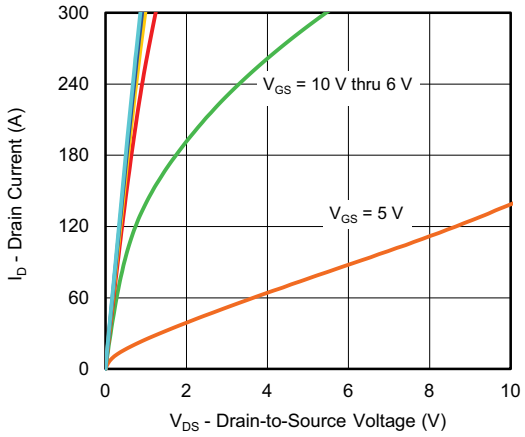
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

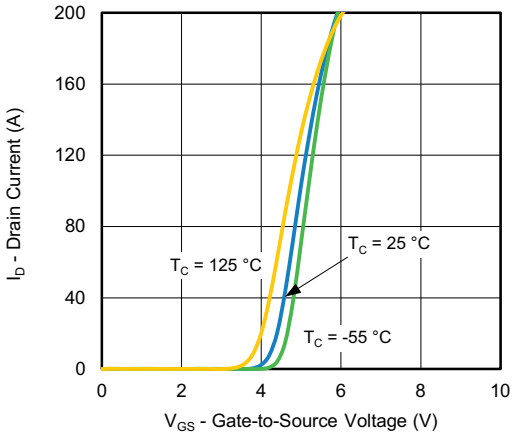
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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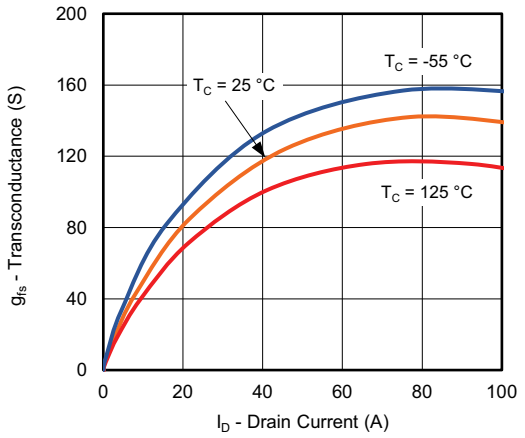
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



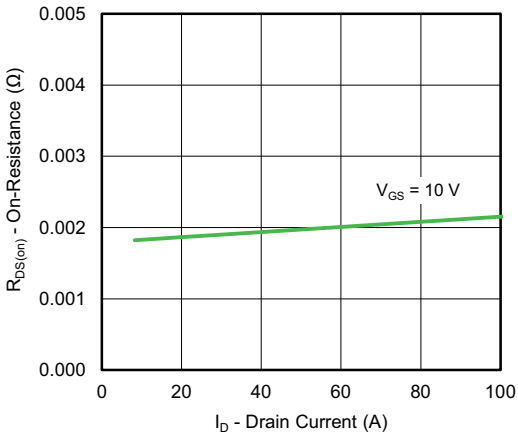
Output Characteristics



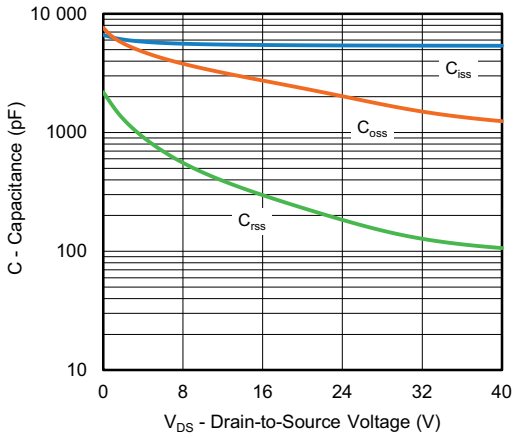
Transfer Characteristics



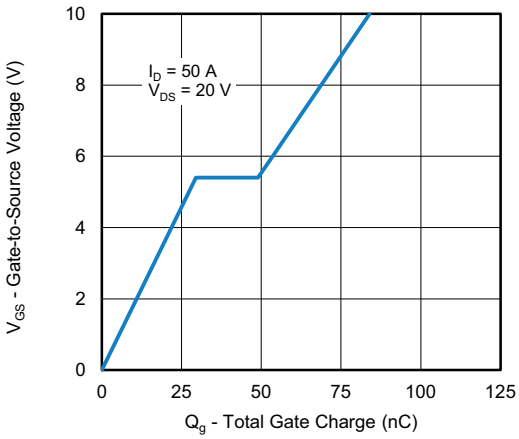
Transconductance



On-Resistance vs. Drain Current



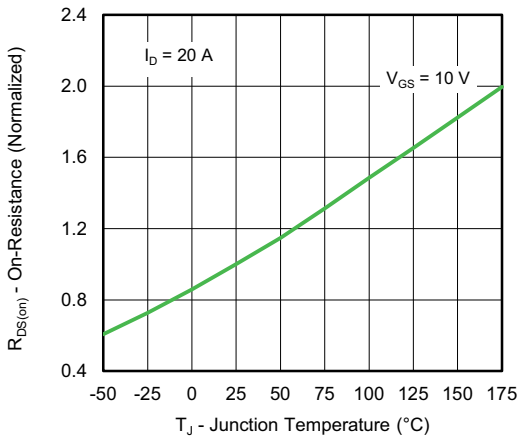
Capacitance



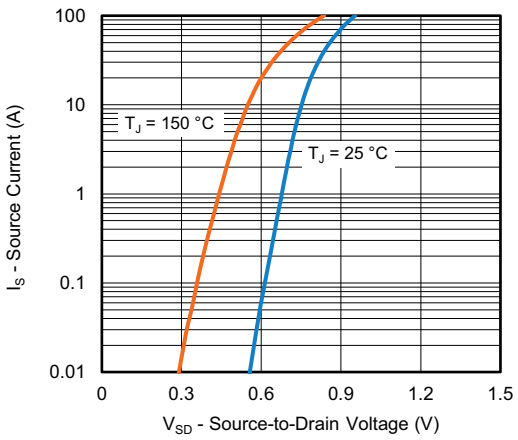
Gate Charge

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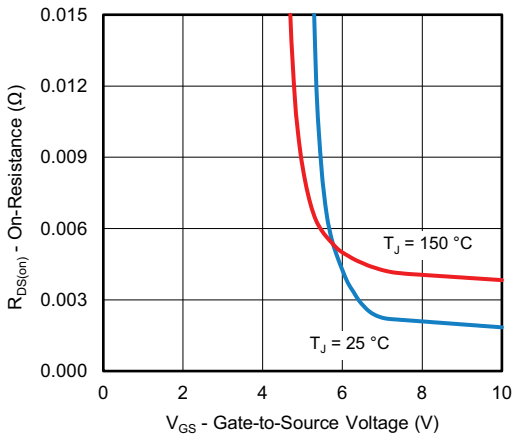
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



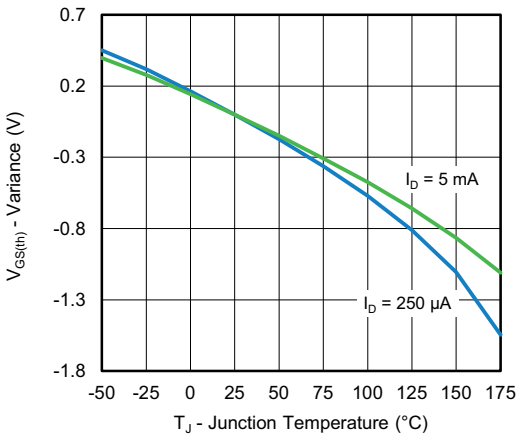
On-Resistance vs. Junction Temperature



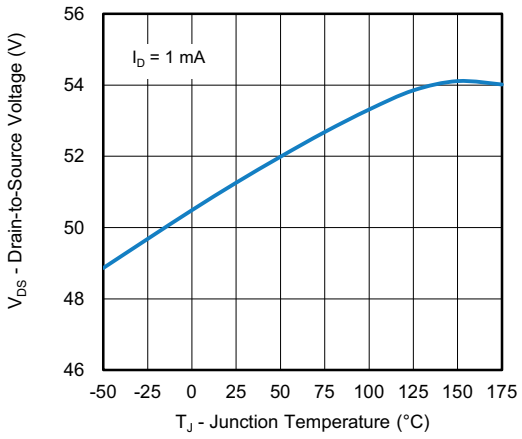
Source Drain Diode Forward Voltage



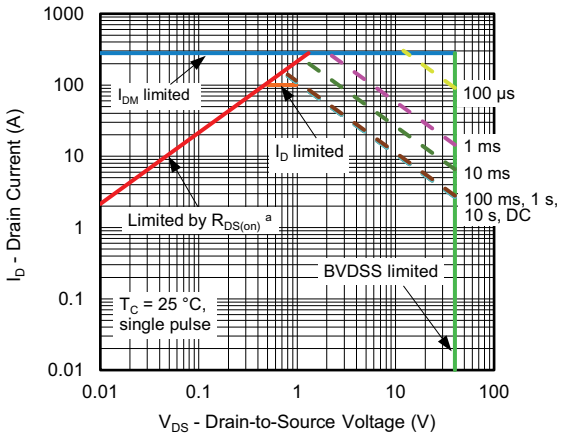
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



Safe Operating Area

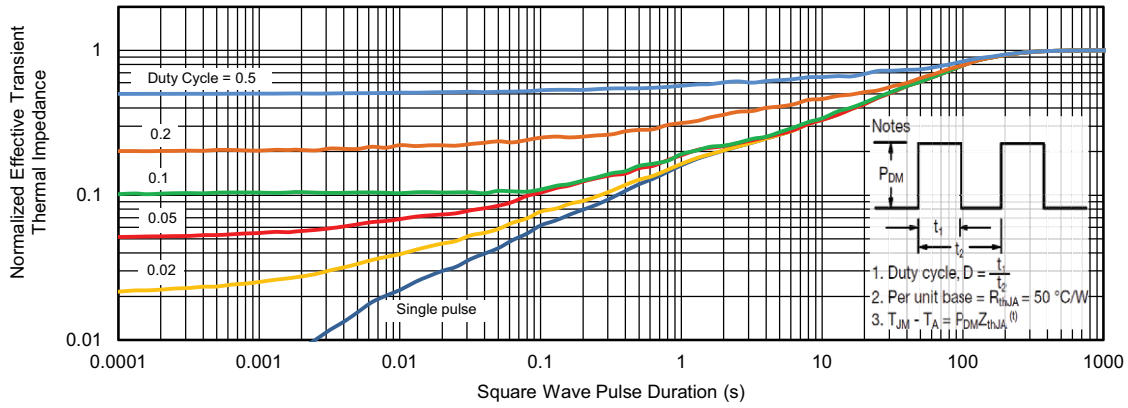
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

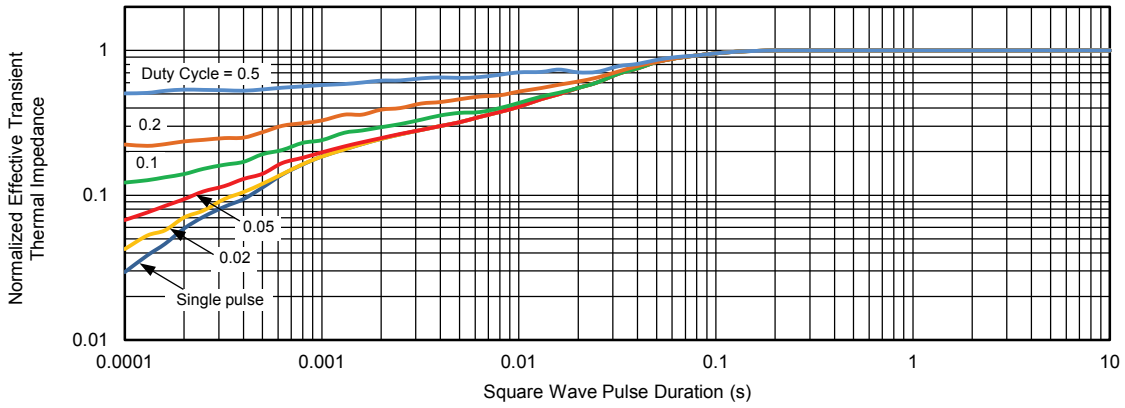
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

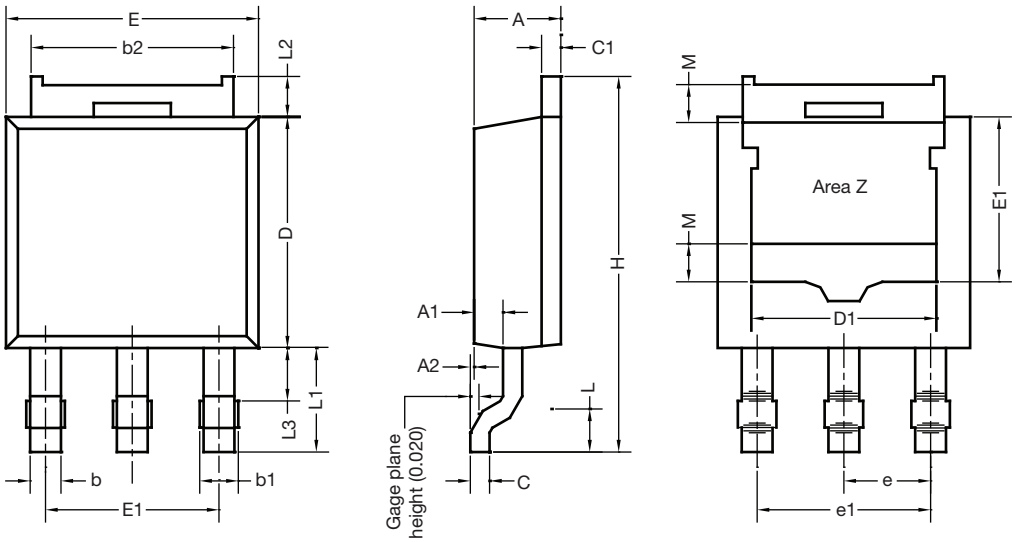
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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TO-252 Reverse Lead Case Outline



Notes

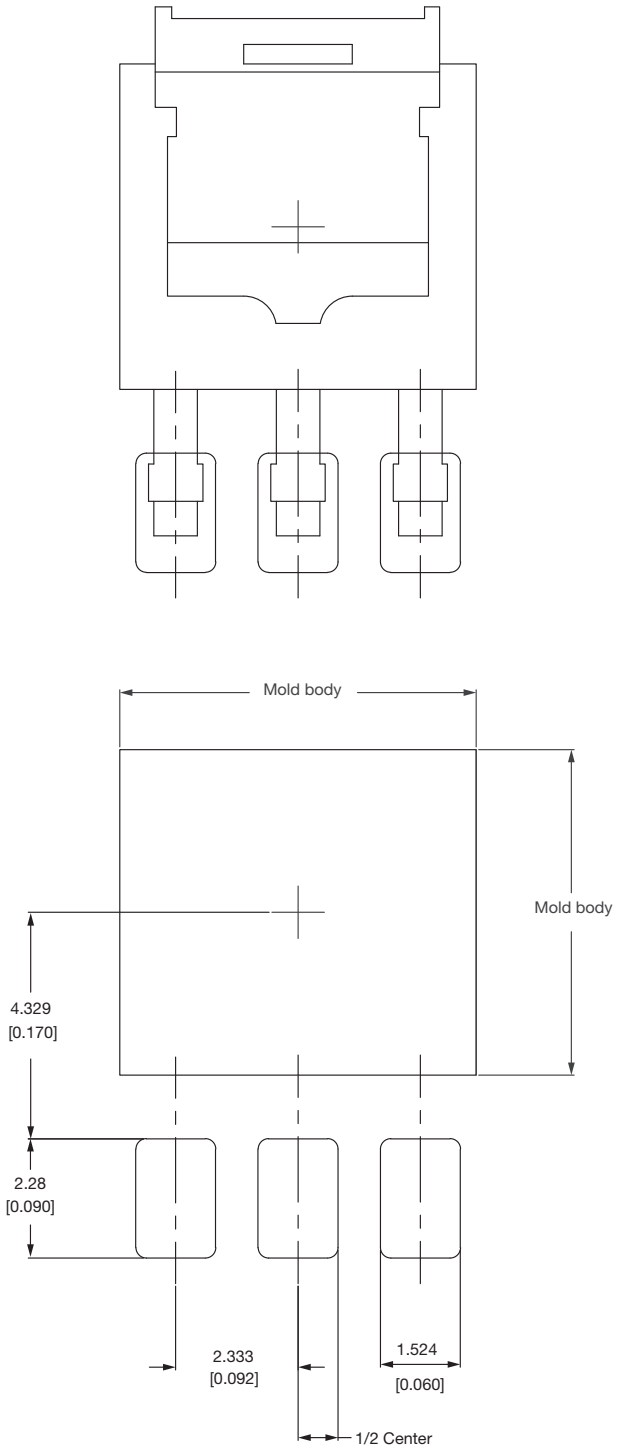
- Dimension L3 for reference only
- Area Z: unplated area more than 80 % heatsink area and for partial plating part only

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.23	2.33	0.088	0.092
A1	0.64	0.89	0.025	0.035
A2	0.03	0.18	0.001	0.007
b	0.71	0.88	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.49	5.00	0.177	0.197
E	6.48	6.73	0.255	0.265
E1	4.32	-	0.170	-
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L1	2.74 BSC		0.108 BSC	
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.040	0.060
M	-	1.00 (reference only)	-	0.039 (reference only)
ECN: T16-0952-Rev. D, 16-Jan-17 DWG: 5894				

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Recommended Land Pattern DPAK (TO-252) 3LR



Note

- Dimensions in mm (inches)

ECN: T22-0575-Rev. A, 12-Dec-2022
DWG: 3015

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