Off-line PWM Controller with Integrated Power MOSFET

STR6S161HXD

Data Sheet

Description

The STR6S161HXD is a power IC for switching power supplies, incorporating a power MOSFET and a current mode PWM control IC.

To enhance efficiency in all load ranges, the IC automatically shifts its operation to the green mode or burst oscillation mode, depending on the load.

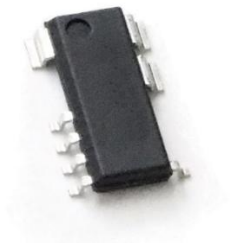
Its enhanced protection functionality allows a more cost-effective power supply system with fewer external components.

Features

- Pb-free (RoHS Compliant)
- Improved Circuit Efficiency (Secondary-side Rectifier Diodes with Lower V_{RM} and V_F Characteristics by Step Drive Control)
- Current Mode PWM Control
- AC Input Voltage Protection Functions:
  - AC Input High-voltage Protection (HVP)
  - Brown-in/Brown-out Function
- Input Power at No Load, P_{IN}: <40 mW
- Load-based Auto-shifting Operation Modes
  - Normal Load: Fixed Switching Frequency Mode, 100 kHz (Typ.)
  - Middle to Light Load: Green Mode, 25 kHz (Typ.) to 100 kHz (Typ.)
  - Light Load: Burst Oscillation Mode
- Random Switching Function
- Slope Compensation Function (for Subharmonic Oscillation Suppression)
- Leading Edge Blanking Function (LEB)
- Bias Assist Function
- Protections Include:
  - Overcurrent Protection (OCP): Pulse-by-Pulse, Two Different OCPs, with Input Compensation Function
  - Overload Protection (OLP) with Timer: Auto-restart
  - Overvoltage Protection (OVP): Auto-restart
  - Thermal Shutdown (TSD): Auto-restart

Package

SOIC16



Not to scale

Specifications

- V_{DSS} = 700 V (Min.)
- $R_{DS(ON)}$ = 3.95 Ω (Max.)
- $f_{OSC(AVG)}$ = 100 kHz
- Output Power, P_{OUT}*

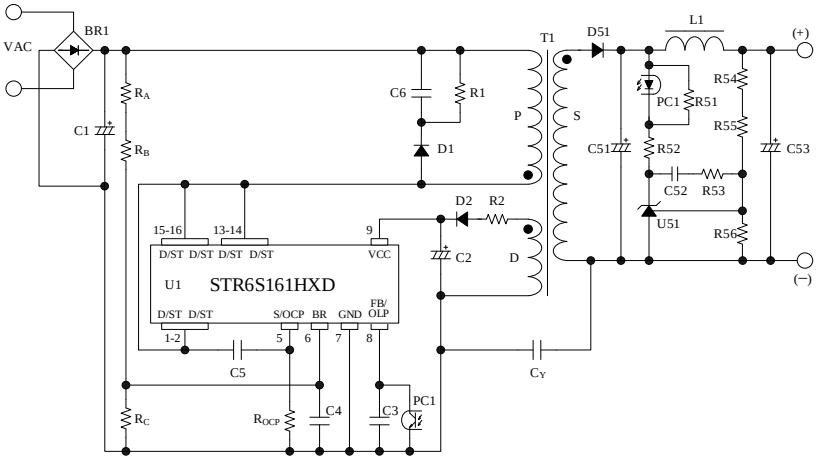
Part Number	Adapter		Open Frame	
	230 VAC	85 to 265 VAC	230 VAC	85 to 265 VAC
STR6S161HXD	19.6 W	14.3 W	33.5 W	22.5 W

* Refers to actual continuous output power measured at 50 °C ambient; the output power can be up to 120-140% of P_{OUT} but may be limited by core size, duty cycle, or thermal design.

Applications

- Large Home Appliance
- Office Automation Equipment
- Audiovisual Equipment
- Industrial Equipment
- Other SMPSs (Switching Mode Power Supplies)

Typical Application



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Contents

Description ---- 1
Contents ---- 2
1. Absolute Maximum Ratings ---- 3
2. Electrical Characteristics ---- 4
3. Mechanical Characteristics ---- 5
4. Derating Curves ---- 6
5. Performance Curves ---- 7
5.1. Power MOSFET SOA Curve ---- 7
5.2. Transient Thermal Resistance Curve ---- 8
6. Block Diagram ---- 9
7. Pin Configuration Definitions ---- 9
8. Typical Application ---- 10
9. Physical Dimensions ---- 11
10. Marking Diagram ---- 12
11. Operational Descriptions ---- 13
11.1. Startup Operation ---- 13
11.2. Undervoltage Lockout (UVLO) ---- 13
11.3. Bias Assist Function ---- 14
11.4. Soft Start Function ---- 14
11.5. Constant Output Voltage Control ---- 15
11.6. Leading Edge Blanking Function ---- 16
11.7. Random Switching Function ---- 16
11.8. Step Drive Control ---- 16
11.9. Operation Modes ---- 16
11.10. AC Input Voltage Protection Functions ---- 17
11.10.1. AC Input High-voltage Protection (HVP) ---- 17
11.10.2. Brown-in/Brown-out Function ---- 17
11.10.3. DC Line Detection ---- 18
11.10.4. AC Line Detection ---- 18
11.11. Overcurrent Protection (OCP) ---- 19
11.11.1. OCP Operation ---- 19
11.11.2. OCP Input Compensation Function ---- 19
11.12. Overload Protection (OLP) ---- 20
11.13. Overvoltage Protection (OVP) ---- 20
11.14. Thermal Shutdown (TSD) ---- 21
12. Design Notes ---- 21
12.1. External Components ---- 21
12.1.1. Input/Output Smoothing Electrolytic Capacitor ---- 21
12.1.2. S/OCP Pin Peripheral Circuit ---- 22
12.1.3. BR Pin Peripheral Circuit ---- 22
12.1.4. FB/OLP Pin Peripheral Circuit ---- 22
12.1.5. VCC Pin Peripheral Circuit ---- 22
12.1.6. Snubber Circuit ---- 22
12.1.7. Phase Compensation ---- 22
12.1.8. Transformer ---- 23
12.2. PCB Pattern Layout ---- 23
13. Pattern Layout Example ---- 25
Important Notes ---- 27

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25°C, all the D/ST pins are shorted on a PCB.

Parameter	Symbol	Conditions	Pins	Rating	Unit
Peak Drain Current(1)	I_{DPEAK}	Single pulse	1 − 5	2.5	A
Maximum Switching Current(2)	I_{DMAX}	T_A = −40 °C to 125 °C	1 − 5	2.5	A
Avalanche Energy(3)(4)	E_{AS}	I_{LPEAK} = 1.78 A	1 − 5	36	mJ
S/OCP Pin Voltage	$V_{S/OCP}$		5 – 7	−2 to 6	V
BR Pin Voltage	V_{BR}		6 – 7	−0.3 to 7.5	V
BR Pin Sink Current	I_{BR}		6 – 7	1.0	mA
FB/OLP Pin Voltage	V_{FB}	$I_{FB} \leq$ 1 mA	8 – 7	−0.3 to 14	V
FB/OLP Pin Sink Current	I_{FB}		8 – 7	1.0	mA
VCC Pin Voltage	V_{CC}		9 – 7	−0.3 to 32	V
D/ST Pin Voltage	$V_{D/ST}$		1 – 7	−1 to V_{DSS}	V
Power MOSFET Allowable Power Dissipation(5)	P_{D1}	When mounted on a PCB of 15 mm × 15 mm	1 − 5	1.25	W
Control Part Allowable Power Dissipation	P_{D2}		9 – 7	1.1	W
Operating Ambient Temperature	T_{OP}		—	−40 to 125	°C
Storage Temperature	T_{STG}		—	−40 to 125	°C
Junction Temperature	T_J		—	150	°C

(1) See Section 5.1.
(2) Refers to a drain current determined by the gate-driving voltage of the IC and the gate-to-source threshold voltage of the power MOSFET, $V_{GS(TH)}$.
(3) See Figure 4-2.
(4) Single pulse, V_{DD} = 99 V, L = 20 mH
(5) See Figure 4-3.

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2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25°C and V_{CC} = 18 V.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		9 – 7	13.8	15.0	16.2	V
Operation Stop Voltage[1]	$V_{CC(OFF)}$		9 – 7	7.6	8.5	9.2	V
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	9 – 7	—	1.5	3.0	mA
Minimum Startup Voltage	$V_{ST(ON)}$		1 – 7	40	47	55	V
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V $V_{D/ST}$ = 100 V	9 – 7	−4.05	−2.50	−1.08	mA
Startup Current Bias Threshold Voltage	$V_{CC(BIAS)}$	I_{CC} = −500 µA	9 – 7	8.0	9.6	10.5	V
Normal Operation							
Average Oscillation Frequency	$f_{OSC(AVG)}$		1 – 7	90	100	110	kHz
Oscillation Frequency Fluctuation Width	Δf		1 – 7	—	8.4	—	kHz
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	8 – 7	−170	−130	−85	µA
Minimum Feedback Current	$I_{FB(MIN)}$		8 – 7	−21	−13	−5	µA
Operation at Light Load							
Frequency Decrease Start FB/OLP Pin Voltage	$V_{FB(FDS)}$	$f_{OSC(AVG)}$ × 0.9	8 – 7	2.88	3.60	4.32	V
Frequency Decrease Stop FB/OLP Pin Voltage	$V_{FB(FDE)}$	$f_{OSC(MIN)}$ × 1.1	8 – 7	2.48	3.10	3.72	V
Minimum Oscillation Frequency	$f_{OSC(MIN)}$		1 − 7	18	25	32	kHz
Standby Operation							
Oscillation Stop FB/OLP Pin Voltage	$V_{FB(OFF)}$		8 – 7	1.62	1.77	1.92	V
Brown-in/Brown-out Function							
AC Input High-voltage Protection (HVP) Threshold Voltage[2]	$V_{BR(HVP)}$		6 – 7	5.34	5.51	5.68	V
AC Input High-voltage Protection (HVP) Release Threshold Voltage	$V_{BR(HVPR)}$		6 – 7	5.23	5.39	5.55	V
Brown-in Threshold Voltage	$V_{BR(IN)}$		6 – 7	1.02	1.11	1.20	V
Brown-out Threshold Voltage	$V_{BR(OUT)}$		6 – 7	0.76	0.85	0.94	V
Protection Operation							
Maximum Duty Cycle	D_{MAX}		1 − 7	70	75	80	%
Leading Edge Blanking (LEB) Time	t_{BW}		—	—	330	—	ns
OCP Compensation Coefficient	DPC		—	—	25.8	—	mV/µs
OCP Compensation Duty Cycle	D_{DPC}		—	—	36	—	%
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		5 − 7	0.735	0.795	0.855	V

[1] Always in the condition of $V_{CC(BIAS)} > V_{CC(OFF)}$.
[2] In the condition of $V_{BR(HVP)} > V_{BR(HVPR)}$.

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Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$		1 − 7	0.843	0.888	0.933	V
OCP Threshold Voltage during LEB Time	$V_{OCP(LEB)}$		1 − 7	—	1.69	—	V
OLP Threshold Voltage	$V_{FB(OLP)}$		8 – 7	6.8	7.3	7.8	V
OLP Delay Time	t_{OLP}		8 – 7	55	75	90	ms
Circuit Current in OLP Operation	$I_{CC(OLP)}$		9 – 7	—	260	—	µA
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		8 – 7	10.5	11.8	13.5	V
OVP Threshold Voltage	$V_{CC(OVP)}$		9 – 7	27.0	29.1	31.2	V
TSD Operating Temperature(3)	$T_{J(TSD)}$		—	127	145	—	°C
TSD Operating Temperature Hysteresis	$T_{J(TSD)HYS}$		—	—	80	—	°C
Power MOSFET							
Drain-to-Source Breakdown Voltage	V_{DSS}	I_{DS} = 300 µA	1 − 5	700	—	—	V
Drain Leakage Current	I_{DSS}	V_{DS} = 700 V	1 − 5	—	—	50	µA
On-resistance	$R_{DS(ON)}$	I_{DS} = 0.4 A	1 − 5	—	—	3.95	Ω
Switching Time	t_f		1 − 5	—	—	250	ns
Thermal Resistance							
Junction-to-Case Thermal Resistance	θ_{J-C}		—	—	—	25	°C/W

(3) Refers to the junction temperature of the control stage chip inside the IC.

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.17	—	g

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4. Derating Curves

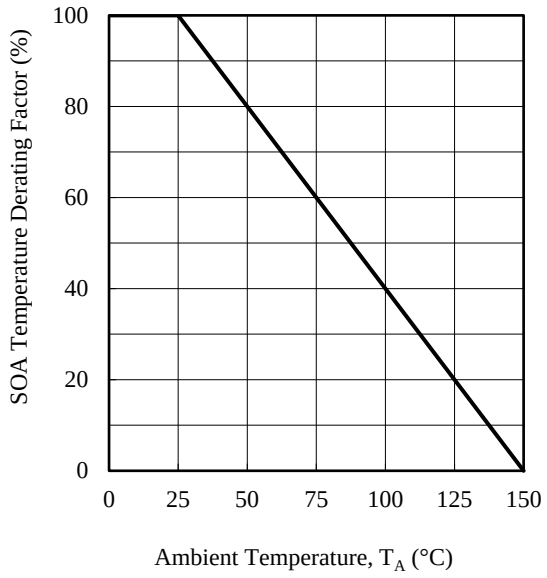

Figure 4-1. SOA Temperature Derating Factor Curve

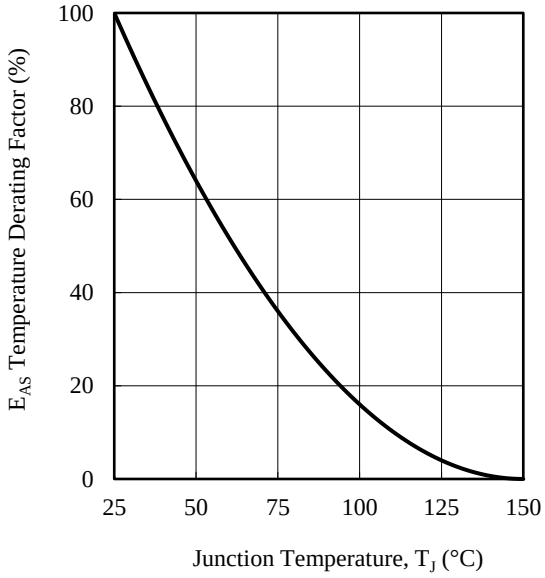

Figure 4-2. Avalanche Energy Derating Factor Curve

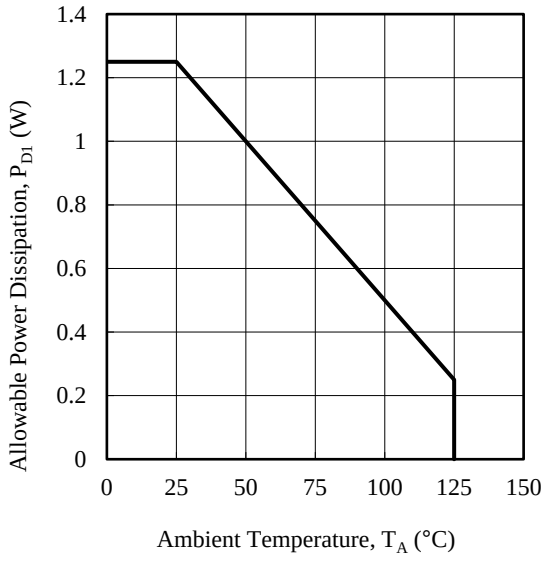

Figure 4-3. Allowable Power Dissipation Temperature Derating Curve

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5. Performance Curves

5.1. Power MOSFET SOA Curve

When using the IC, its safe operating area (SOA) curve should be derated by a temperature derating factor, according to Figure 4-1.

The dashed line in the SOA curve below represents a drain current limited by on-resistance.

Unless specifically noted, T_A = 25 °C, single pulse.

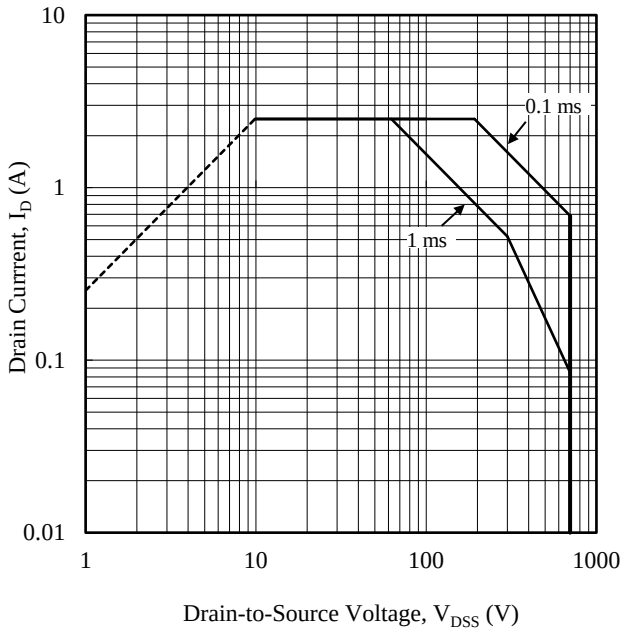

Figure 5-1. Power MOSFET SOA Curve

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5.2. Transient Thermal Resistance Curve

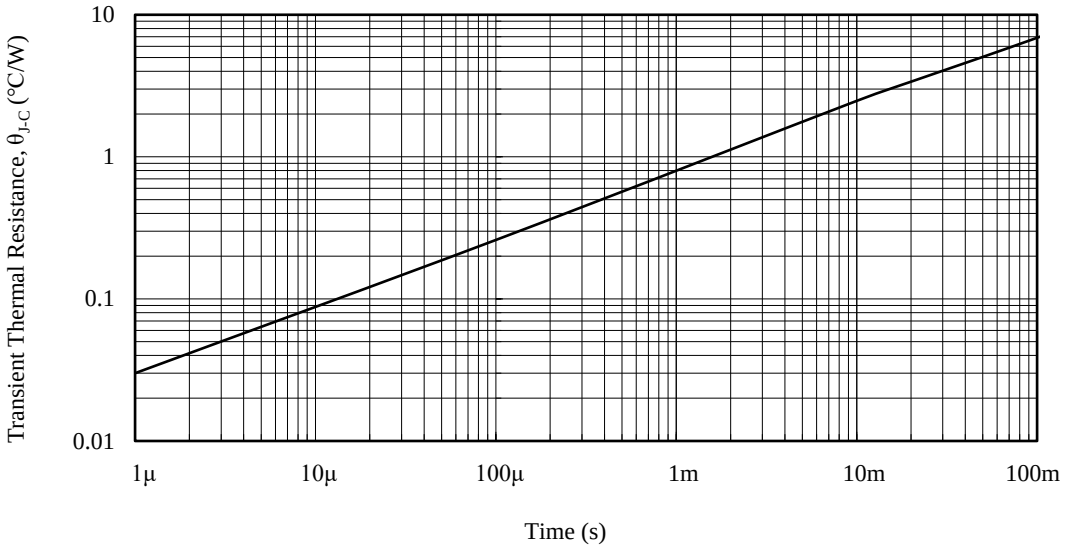

Figure 5-2. Junction-to-Case Transient Thermal Resistance

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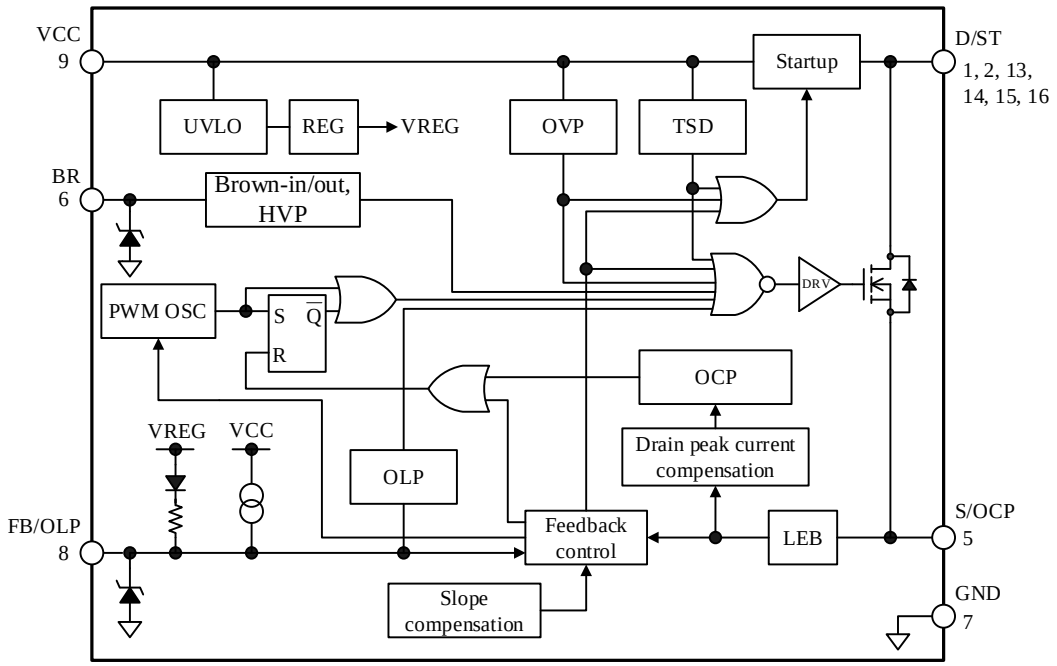
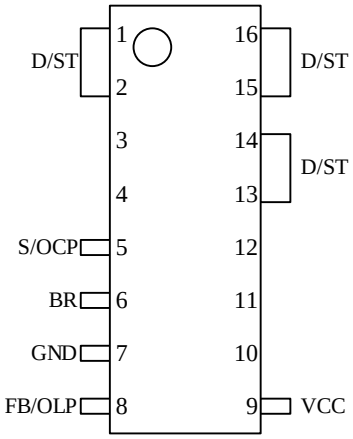
6. Block Diagram



7. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	D/ST	Power MOSFET drain; startup current input
2		
3	—	(Pin removed)
4	—	(Pin removed)
5	S/OCP	Power MOSFET source; overcurrent protection (OCP) signal input
6	BR	AC input voltage detection signal input
7	GND	Ground
8	FB/OLP	Constant voltage control signal input; overload protection (OLP) signal input
9	VCC	Logic power supply input; overvoltage protection (OVP) signal input
10	—	(Pin removed)
11	—	(Pin removed)
12	—	(Pin removed)
13	D/ST	Power MOSFET drain; startup current input
14		
15		
16		

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8. Typical Application

To enhance heat dissipation effects, the D/ST pins (Pins 1, 2, 13 to 16) should have traces as wide as possible on a PCB. If your power supply specifications may cause the D/ST pin to have high transient surge voltages, add one or more of the following snubber circuits: a capacitor-resistor-diode (CRD) clamp circuit close to the primary-side main winding P; a capacitor (C) or resistor-capacitor (RC) damper circuit between the D/ST and S/OCP pins.

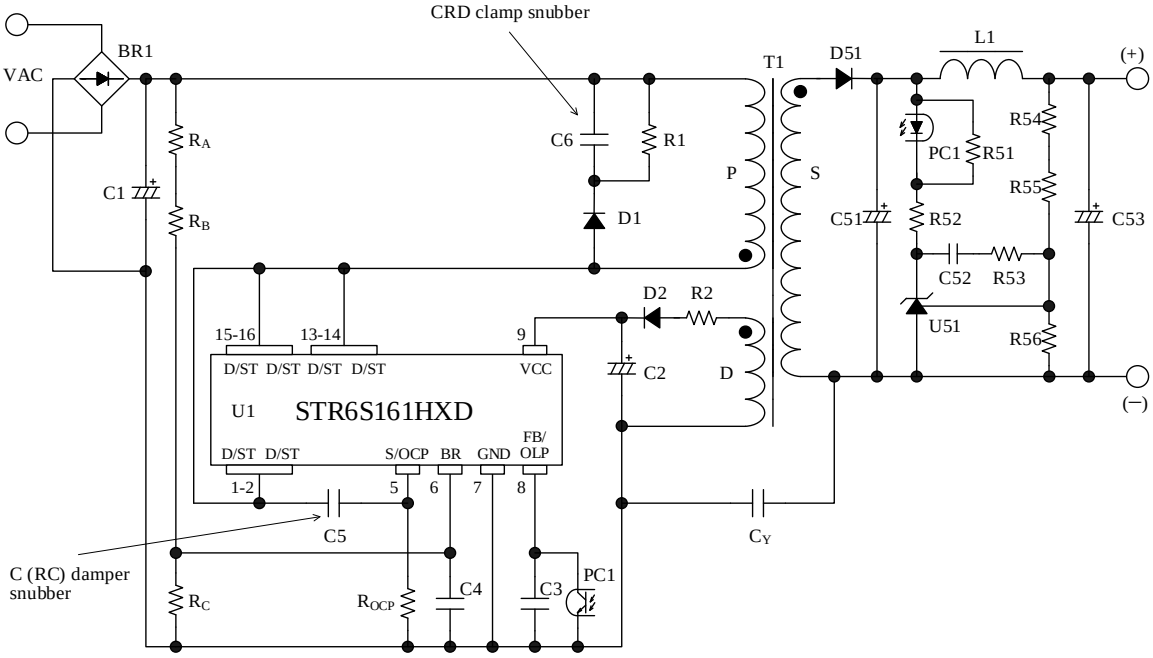

Figure 8-1. Typical Application

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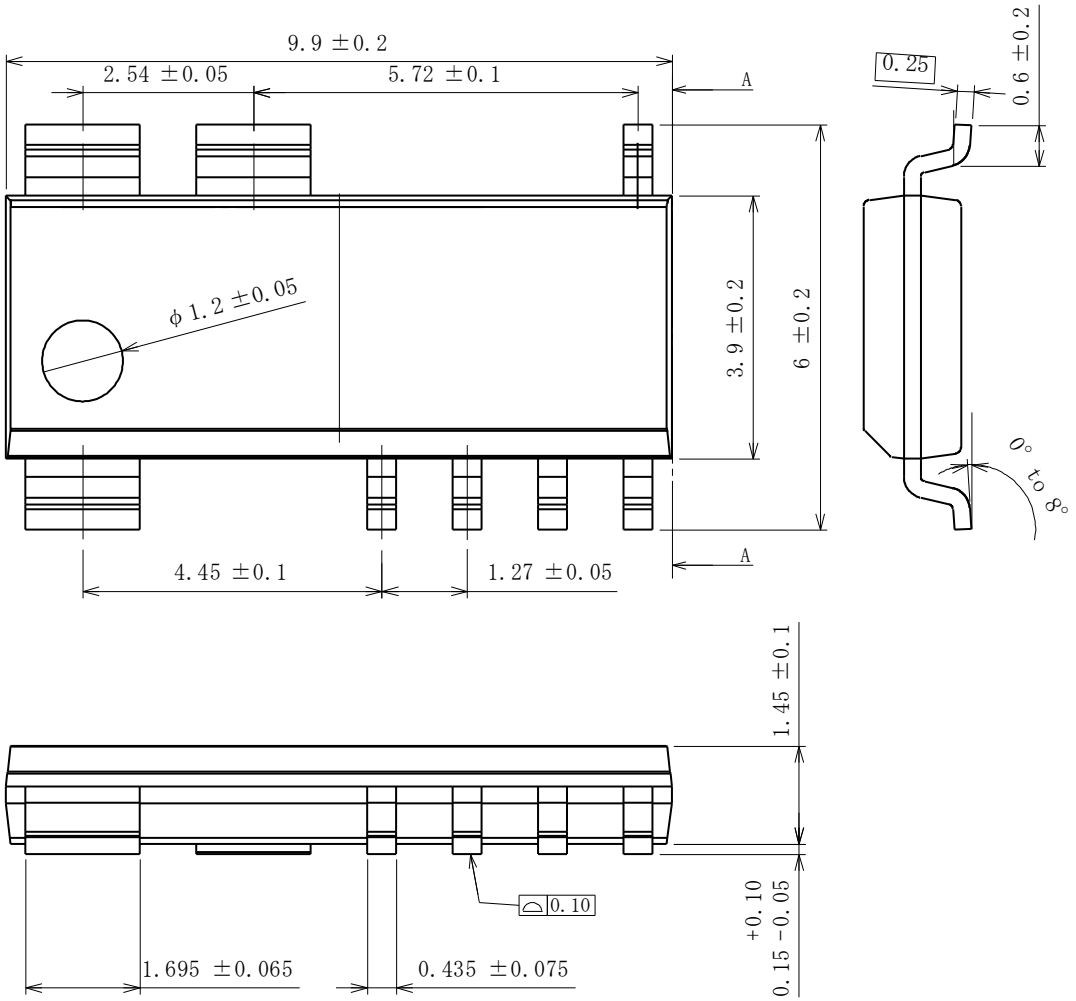
9. Physical Dimensions

- SOIC16



NOTES:

- Dimension in millimeters
- Dimensions do not include mold burrs.
- Pb-free (RoHS compliant)
- MSL 1 (Moisture Sensitivity Level 1)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Reflow
  Preheat: 150 °C to 200 °C / 60 s to 120 s
  Solder heating: 255 °C / 30s, 3 times (260 °C peak)
  Soldering iron: 350 °C / 3.5 s, 1 time

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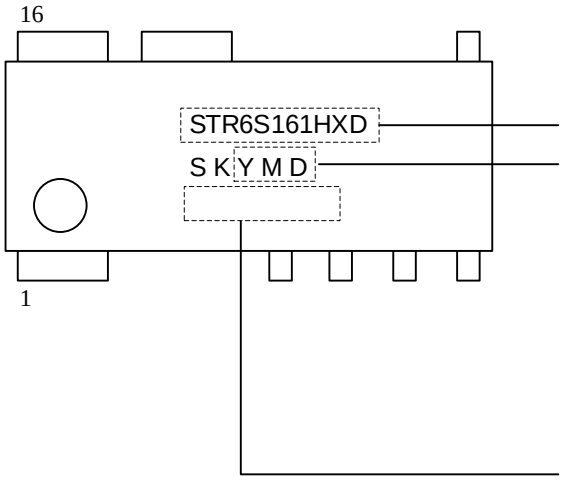
10. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is the period of days represented by:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

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11. Operational Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

11.1. Startup Operation

Figure 11-1 illustrates the VCC pin and its peripheral circuit, whereas Figure 11-2 depicts operational waveforms at startup.

The IC incorporates its own startup circuit, which is connected to the D/ST pin. When the D/ST pin voltage reaches the Minimum Startup Voltage, $V_{ST(ON)}$ = 47 V, the startup circuit starts to operate.

During the startup operation, the Startup Current, $I_{CC(ST)}$ = −2.50 mA, which becomes constant inside the IC, charges C2 connected to the VCC pin. When the VCC pin voltage increases to the Operation Start Voltage, $V_{CC(ON)}$ = 15.0 V, the control circuit starts to operate.

t_{START} is a period of time until the control circuit starts to operate (see Figure 11-2) and is determined by the capacitance of C2. The approximate startup time, t_{START}, can be calculated by Equation (1) below:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left|I_{CC(ST)}\right|} \quad . \tag{1}$$

Where:
t_{START} is the startup time of the IC (s), and
$V_{CC(INT)}$ is the initial VCC pin voltage (V).

When the BR pin voltage is less than $V_{BR(IN)}$ = 1.11 V, the bias assist function is disabled (see Section 11.3). Thus, the VCC pin voltage repeats fluctuating between $V_{CC(ON)}$ and $V_{CC(OFF)}$, as shown in Figure 11-2. When the BR pin voltage increases to $V_{BR(IN)}$ or more after that, the IC starts to oscillate. After the IC starts oscillating, a voltage to be applied to the VCC pin is the rectified auxiliary winding voltage, V_D, as shown in Figure 11-1. When the power startup sequence ends, the startup circuit automatically turns off to eliminate the power dissipation by itself.

The winding turns of the auxiliary winding D should be adjusted so that the VCC pin voltage falls within the range defined by Equation (2), in accordance with the power supply specifications giving the variation range of input and output voltages. The reference voltage across the auxiliary winding is about 18 V.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.}) \ ,$$

that is,

$$10.5\ (\text{V}) < V_{CC} < 27.0\ (\text{V}). \tag{2}$$

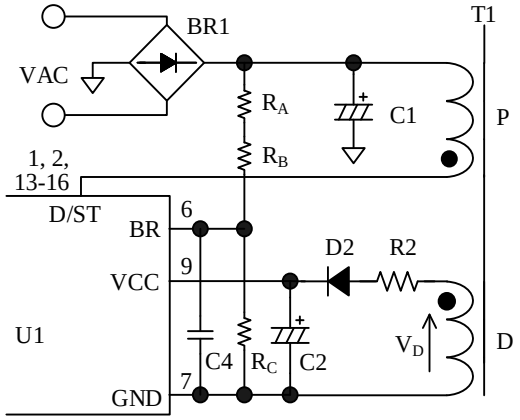

Figure 11-1. VCC Pin Peripheral Circuit

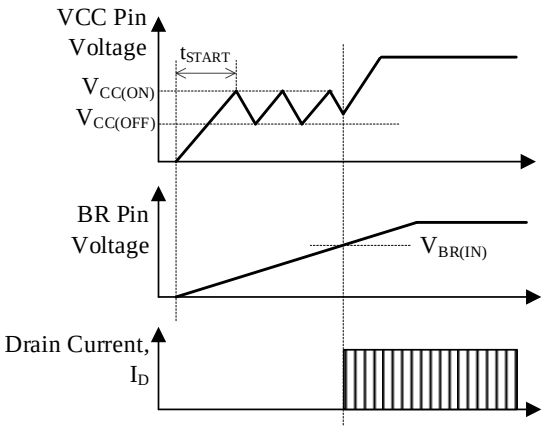

Figure 11-2. Operational Waveforms at Startup

11.2. Undervoltage Lockout (UVLO)

Figure 11-3 shows the relation between the VCC pin voltage and the circuit current, I_{CC}. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V after the control circuit activation, the undervoltage lockout (UVLO) circuit stops the control circuit operation. The control circuit is then put back into the state before startup.

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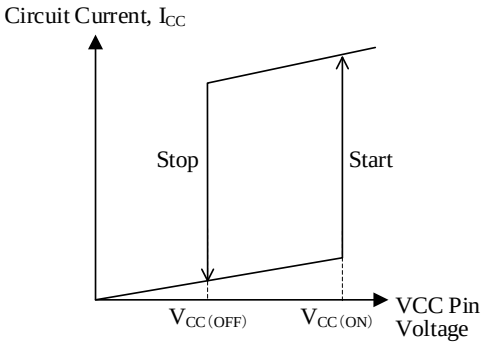

Figure 11-3. VCC Pin Voltage vs. Circuit Current, I_{CC}

11.3. Bias Assist Function

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V at startup, the control circuit stops operating, thus resulting in a startup failure. The bias assist function prevents startup failures. The bias assist function starts to operate when the following two conditions are met: when the FB/OLP pin voltage decreases to the Oscillation Stop FB/OLP Pin Voltage, $V_{FB(OFF)}$ = 1.77 V or less; when the VCC pin voltage decreases to the Startup Current Bias Threshold Voltage, $V_{CC(BIAS)}$ = 9.6 V.

During the bias assist function operation, the startup circuit supplies startup current so that the VCC pin voltage can be near-constant at $V_{CC(BIAS)}$. Accordingly, the VCC pin voltage is held above $V_{CC(OFF)}$.

Since startup failures are prevented by the bias assist function, the capacitor C2 connected to the VCC pin requires a smaller capacitance. As a result, a startup time of the IC and a response time of the overvoltage protection (OVP) can be shortened.

The following explains how the bias assist function operates at power startup. For assured startup failure prevention, the startup constants must be adjusted based on the operation performance checked with an actual board.

Figure 11-4 shows an example waveform of the VCC pin voltage at power startup.

When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V at startup, the IC starts to operate. Then, the VCC pin voltage decreases due to an increase in the circuit current. At the same time, the auxiliary winding voltage, V_D, increases in proportion to a rise in the output voltage. The VCC pin voltage consists of these well-balanced voltages.

If the output load is light at startup, the output voltage may increase to the target voltage or more due to a delayed response of the feedback control circuit. In this case, the feedback control circuit decreases the FB/OLP pin voltage to $V_{FB(OFF)}$ or less. This causes the IC to stop oscillating and the VCC pin voltage to decrease. When the VCC pin voltage decreases to $V_{CC(BIAS)}$ under this condition, the bias assist function starts to prevent a possible startup failure.

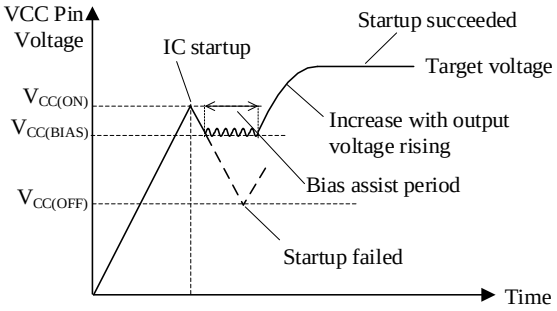

Figure 11-4. VCC Pin Voltage at Startup

11.4. Soft Start Function

Figure 11-5 shows the operational waveforms of the VCC pin voltage and drain current at startup. The IC activates the soft start function at power startup.

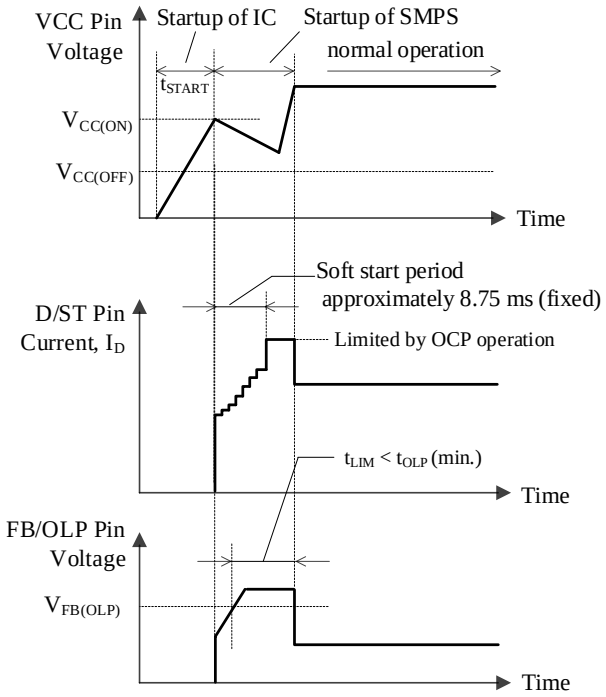

Figure 11-5. Operational Waveforms at Startup

A soft start operation period is internally fixed to approximately 8.75 ms. During this period, an overcurrent threshold increases in 7 steps. This stepwise increase reduces voltage and current stresses on the power MOSFET and a secondary-side rectifier diode.

During the soft start operation, the leading edge blanking function (see Section 11.6) is disabled. This may cause the power MOSFET to have an on-time of

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t_{BW} = 330 ns or less.

After the soft start operation, the power MOSFET drain current, I_D, is limited by the overcurrent protection (OCP) until the output voltage reaches the target voltage. This period is defined as t_{LIM}.

When t_{LIM} is the OLP Delay Time, t_{OLP}, or longer, the IC enables the overload protection (OLP) to limit the output power.

For that reason, a capacitance of the output electrolytic capacitor and a winding turns ratio of the transformer auxiliary winding D must be adjusted so that t_{LIM} is less than t_{OLP} = 55 ms (min.) during the startup operation.

11.5. Constant Output Voltage Control

For the constant voltage control of output voltages, the IC uses a current mode control (peak current mode control), which excels in transient response and stability.

The IC has the internal FB comparator, which compares the voltage across the current detection resistor R_{OCP} (V_{ROCP}) and the target voltage (V_{SC}) to control a peak value of V_{ROCP} to be approximated to V_{SC}.

The target voltage, V_{SC}, is a reference voltage generated by applying slope compensation to the FB/OLP pin voltage input to the feedback control block (see Section 6), as shown in Figure 11-6 and Figure 11-7.

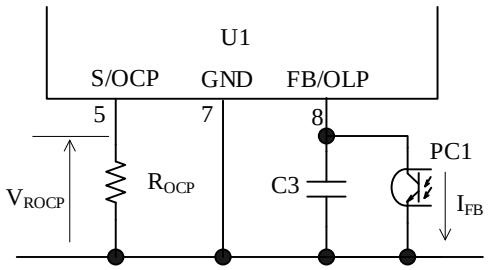

Figure 11-6. FB/OLP Pin Peripheral Circuit

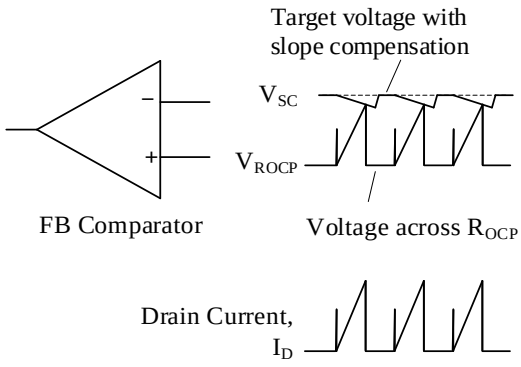

Figure 11-7. Drain Current, I_D, and FB Comparator in Normal Operation

In light-load operation, the feedback current flowing through the secondary-side error amplifier increases along with a rise in the output voltage. The feedback current is sunk from the FB/OLP pin via the optocoupler PC1, thus lowering the FB/OLP pin voltage. As a result, the target voltage, V_{SC}, decreases. The IC controls the peak value of V_{ROCP} to decrease along with this V_{SC} drop. Since the constant voltage control reduces the peak value of the drain current, a rise in the output voltage can be suppressed.

Contrary to the light-load operation, the FB comparator target voltage, V_{SC}, increases in heavy-load operation. This raises the peak value of the drain current, thus preventing a decrease in the output voltage.

When the PWM peak current mode control operates in continuous conduction mode (CCM), triangular waveforms of the drain current become trapezoidal. As shown in Figure 11-8, this CCM operation causes subharmonic oscillation because the on-time varies due to the initial value of the drain current even if the peak drain current is constant, which is determined by a control amount (i.e., the target voltage, V_{SC}).

Subharmonic oscillation is a phenomenon in which an on-time varies at integral multiples of a switching frequency.

To prevent this phenomenon, the IC has the slope compensation function that suppresses subharmonic oscillation by applying a downslope compensation signal (which decreases the peak drain current as the duty cycle increases) to the FB/OLP pin voltage signal.

Subharmonic oscillation may occur if the power supply is in a transient state (e.g., during a startup or load short). However, this does not cause operational problems for the IC.

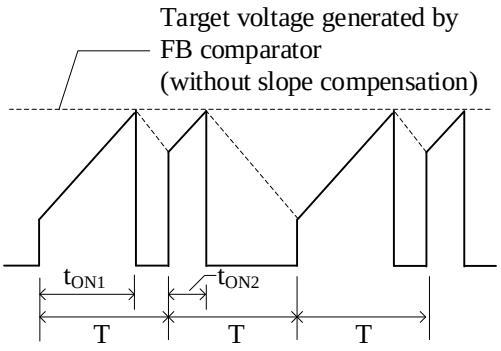

Figure 11-8. Drain Current Waveform in Subharmonic Oscillation

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11.6. Leading Edge Blanking Function

The IC controls the output voltage to be constant with a peak current mode control.

In the peak current mode control, the power MOSFET can be turned off because the FB comparator or the OCP circuit responds to a steep surge current occurred at power MOSFET turn-on. As a prevention against such operation, the IC has the Leading Edge Blanking Time (t_{BW} = 330 ns), which starts immediately after power MOSFET turn-on. During t_{BW}, the IC controls the OCP circuit so that it does not respond to any drain current surge at power MOSFET turn-on by setting its threshold voltage to $V_{OCP(LEB)}$ = 1.69 V, which is higher than that of normal operation (see Section 11.11).

11.7. Random Switching Function

The IC has the random switching function to reduce mains terminal disturbance voltage (conduction noise). The random switching function superposes a frequency variation on the PWM Average Oscillation Frequency, $f_{OSC(AVG)}$, so that the IC randomly modulates its switching frequency in normal operation by producing a slight variation in $f_{OSC(AVG)}$. Accordingly, the IC minimizes the mains terminal disturbance voltage less than that of a product without this function and thus simplifies a noise filter for the input line of a power supply.

11.8. Step Drive Control

Figure 11-9 shows a flyback control circuit. A surge voltage is generated across the secondary-side rectifier diode D51 at power MOSFET turn-on. Therefore, the surge voltage must be taken into account when you select a breakdown voltage (V_{RM}) of D51.

The IC optimally controls the drive capability for the gate of the internal power MOSFET depending on the load condition (i.e., a step drive control), thus reducing the surge voltage across D51 at power MOSFET turn-on (see Figure 11-10). This step drive control allows the IC to use D51 with V_{RM} lower than conventional MOSFETs; as a result, cost-reduced and lower-V_F D51 can bring higher circuit efficiency.

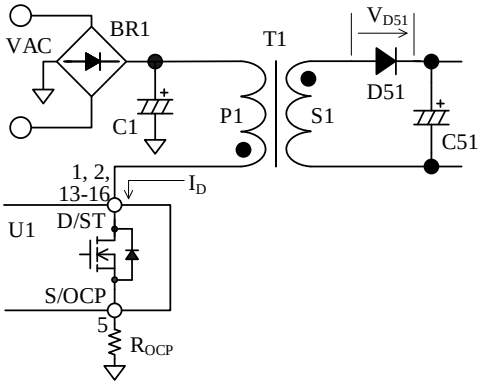

Figure 11-9. Flyback Control Circuit

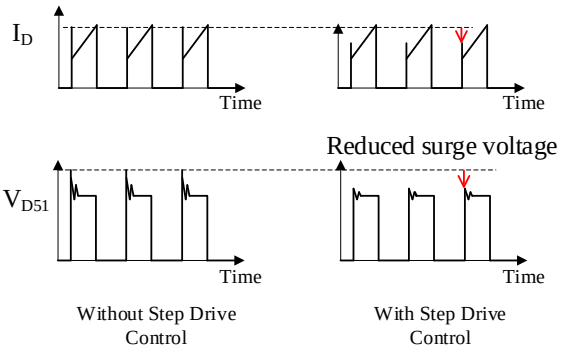

Figure 11-10. Waveforms of I_D and V_{D51}

11.9. Operation Modes

As Figure 11-11 shows, the IC automatically shifts into the following operation modes when the power MOSFET drain current lowers due to a decrease in the output power: the fixed switching frequency mode (100 kHz), the green mode (25 kHz to 100 kHz), and the burst oscillation mode. The IC brings higher efficiency by reducing switching losses: the green mode decreases the number of switching times, whereas the burst oscillation mode stops switching operations for a certain period.

When the load becomes lighter, the FB/OLP pin voltage decreases. The IC enters the green mode when the FB/OLP pin voltage decreases to the Frequency Decrease Start FB/OLP Pin Voltage, $V_{FB(FDS)}$ = 3.60 V or less. Then, the frequency continues decreasing until the FB/OLP pin voltage reaches the Frequency Decrease Stop FB/OLP Pin Voltage, $V_{FB(FDE)}$ = 3.10 V. During this frequency decrease, the minimum oscillation frequency is $f_{OSC(MIN)}$ = 25 kHz.

When the FB/OLP pin voltage further decreases and reaches the standby operation point, the IC enters the burst oscillation mode. As shown in Figure 11-12, the burst oscillation mode includes oscillating and non-oscillating periods.

In the burst oscillation mode, the IC performs

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switching operation at $f_{OSC(MIN)}$ = 25 kHz during an oscillating period.

In general, a burst oscillation frequency is set to several kHz or less to increase efficiency at light load. This low-frequency operation, however, may cause audible noise from the transformer. The IC suppresses such audible noise by regulating the peak drain current to a low level during the burst oscillation mode.

Propagation delay times generally occur in IC operations, such as an overcurrent detection. For this reason, the higher the AC input voltage, the steeper the slope of the drain current, I_D. Consequently, the higher the AC input voltage, the higher the peak value of I_D in a burst oscillation operation. It must be noted that the burst oscillation frequency lowers as the AC input voltage rises.

When the VCC pin voltage decreases to the Startup Current Bias Threshold Voltage, $V_{CC(BIAS)}$ = 9.6 V, during a transition to the burst oscillation mode, the bias assist function is activated to supply the Startup Current, $I_{CC(ST)}$, to the VCC pin. This operation suppresses a decrease in the VCC pin voltage and enables a stable standby operation. If the bias assist function is activated in steady-state operations (including the burst oscillation mode), power dissipation increases. Therefore, the VCC pin voltage should be set higher than $V_{CC(BIAS)}$ by adjusting the turns ratios of the auxiliary winding and the secondary winding or by reducing the value of R2 (see Section 12.1).

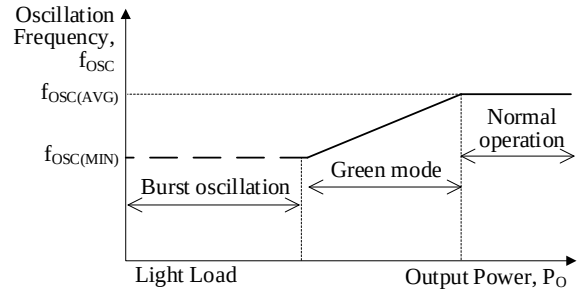

Figure 11-11. Output Power, P_O (Load) vs. Oscillation Frequency, f_{OSC}

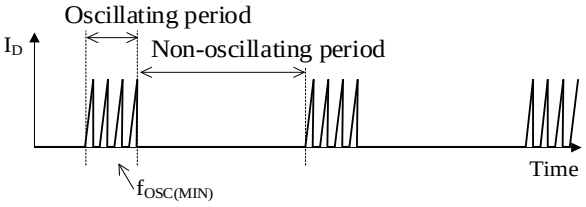

Figure 11-12. Operational Waveform in Burst Oscillation Mode

11.10. AC Input Voltage Protection Functions

The AC input voltage protection includes two protections: the high-voltage protection (HVP) for higher supply input voltages and the brown-in/brown-out function for lower supply input voltages. These functions prevent the IC from excessive input current or overheating.

The BR pin is used for detecting AC input voltages. According to the levels that the BR pin voltage reaches, the IC turns on and off switching operations.

Sections 11.10.1 and 11.10.2 describe the HVP and brown-in/brown-out functions, respectively.

The IC also has two ways to detect AC input voltages from AC or DC lines (see Sections 11.10.3 and 11.10.4). Figure 11-13 depicts operational waveforms during the AC input voltage protection.

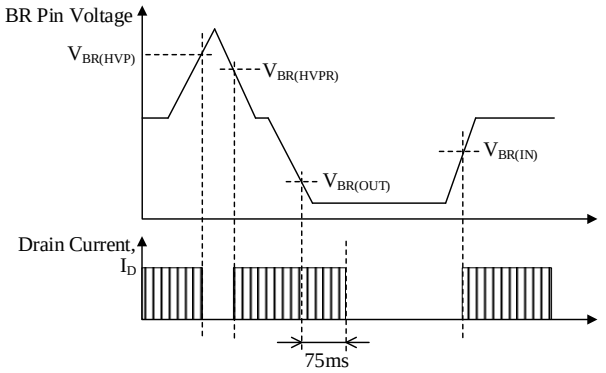

Figure 11-13. Waveforms during AC Input Voltage Protection

11.10.1. AC Input High-voltage Protection (HVP)

When the BR pin voltage increases to $V_{BR(HVP)}$ = 5.51 V or more after an AC input voltage rises from its steady-state level, the high-voltage protection (HVP) is activated. Then, the IC stops the switching operation.

The IC has a hysteresis for the HVP threshold voltage. Because of the AC Input High-voltage Protection (HVP) Release Threshold Voltage, $V_{BR(HVPR)}$ = 5.39 V, the IC keeps a stable HVP operation even if the BR pin voltage fluctuates slightly.

When the BR pin voltage decreases to $V_{BR(HVPR)}$ or less after the AC input voltage lowers, the IC resumes the switching operation.

11.10.2. Brown-in/Brown-out Function

When the BR pin voltage decreases to $V_{BR(OUT)}$ = 0.85 V or less after an AC input voltage lowers from its steady-state level, and remains in this condition for t_{OLP} = 75 ms even with the IC in operation

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(i.e., $V_{CC(OFF)} \leq V_{CC}$), the IC stops the switching operation. When the IC is in operation and the BR pin voltage increases to $V_{BR(IN)}$ = 1.11 V or more after the AC input voltage rises, the IC resumes the switching operation. Note that this function is disabled during a non-oscillating period of the burst oscillation mode. In the burst oscillation mode, when the BR pin voltage decreases to $V_{BR(OUT)}$ or less and the sum of oscillating periods is t_{OLP} = 75 ms or longer, the IC stops the switching operation.

11.10.3. DC Line Detection

Figure 11-14 shows the BR pin peripheral circuit for DC line detection. There is a ripple voltage with a 1/2 cycle of an AC power supply frequency across C1. To detect peak AC ripple voltages at both ends of C1, the time constants of RC and C4 should be shorter than a 1/2 cycle of the AC power supply frequency.

Even if the bottom of the ripple voltage falls below $V_{BR(OUT)}$ due to load variation, the IC does not stop the switching operation because the ripple cycle is shorter than t_{OLP}.

In this way, the DC line detection is less affected by load conditions.

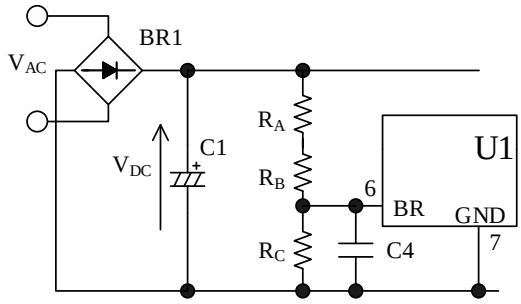

Figure 11-14. Circuit Connections for DC Line Detection

Reference circuit constants are as follows:

- R_A, R_B: About 1 MΩ to 10 MΩ
  These are set at high resistance such that high voltage is applied to them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; connect resistors in series to reduce each applied voltage.
- R_C: About 10 kΩ to 150 kΩ
- C4: 470 pF to 2200 pF (for high-frequency noise filtering)

If an input resistance or a forward voltage of a rectifier diode is not factored into, the equation below determines a reference voltage across C1 at which the HVP or brown-in/brown-out function is activated:

$$V_{DC(OP)} = V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right). \quad (3)$$

Where:

$V_{DC(OP)}$ is the voltage across C1 at which the HVP or brown-in/brown-out operation starts, and

$V_{BR(TH)}$ is the BR pin threshold voltage (see Table 11-1).

Table 11-1. BR Pin Threshold Voltages

Parameter	Symbol	Value (Typ.)
AC Input High-voltage Protection (HVP) Threshold Voltage	$V_{BR(HVP)}$	5.51 V
AC Input High-voltage Protection (HVP) Release Threshold Voltage	$V_{BR(HVPR)}$	5.39 V
Brown-in Threshold Voltage	$V_{BR(IN)}$	1.11 V
Brown-out Threshold Voltage	$V_{BR(OUT)}$	0.85 V

$V_{DC(OP)}$ can be converted to an effective value of the AC input voltage by the equation below:

$$V_{AC(OP)RMS} = \frac{1}{\sqrt{2}} \times V_{DC(OP)}. \quad (4)$$

The constants of R_A, R_B, R_C, and C4 should be adjusted based on the operation performance checked with an actual board.

11.10.4. AC Line Detection

Figure 11-15 shows the BR pin peripheral circuit for AC line detection. To detect AC input voltages with the BR pin, the time constants of RC and C4 should be longer than the cycle of an AC power supply frequency. This setting makes a response speed of the BR pin slower than that of the DC line detection.

However, the AC line detection is less affected by C1 charging/discharging times and load conditions.

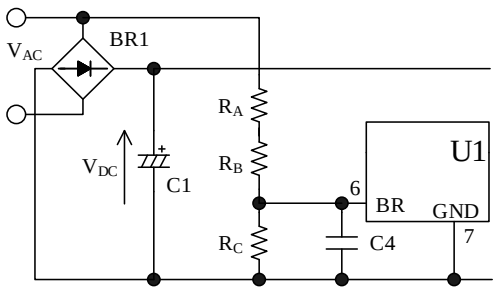

Figure 11-15. Circuit Connections for AC Line Detection

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Reference circuit constants are as follows:

- R_A, R_B: About 1 MΩ to 10 MΩ
  These are set at high resistance such that high voltage is applied to them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; connect resistors in series to reduce each applied voltage.
- R_C: About 10 kΩ to 150 kΩ
- C4: 0.22 µF to 1 µF (for AC input voltage averaging and high-frequency noise filtering)

If an input resistance is not factored into, the equation below determines a reference effective value of the AC input voltage at which the HVP or brown-in/brown-out function is activated:

$$V_{AC(OP)RMS} = \frac{\pi}{\sqrt{2}} \times V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right). \quad (5)$$

Where:

$V_{AC(OP)RMS}$ is the effective AC input voltage at which the HVP or brown-in/brown-out operation starts, and

$V_{BR(TH)}$ is the BR pin threshold voltage (see Table 11-1).

The constants of R_A, R_B, R_C, and C4 should be adjusted based on the operation performance checked with an actual board.

11.11. Overcurrent Protection (OCP)

11.11.1. OCP Operation

The overcurrent protection (OCP) turns off the power MOSFET to limit the output power when a peak drain current of the power MOSFET reaches the OCP threshold voltage (pulse-by-pulse basis).

The OCP threshold voltage during t_{BW} is set to $V_{OCP(LEB)}$ = 1.69 V, which is higher than that of normal operation. Changing the threshold voltage to a higher level prevents the IC from responding to a drain current surge at power MOSFET turn-on. The OCP function protects against abnormal conditions, such as when output windings are shorted or when a secondary-side rectifier diode has an abnormal breakdown voltage. The width of a surge voltage on the drain pin at power MOSFET turn-on should be shorter than t_{BW}, as shown in Figure 11-16. To suppress such surge voltage, extreme care should be taken for the R_{OCP} trace layout. For the notes on PCB pattern layouts, see Section 12.2.

When your application uses a damper snubber as in Figure 11-17, reduce its capacitance to suppress the surge voltage.

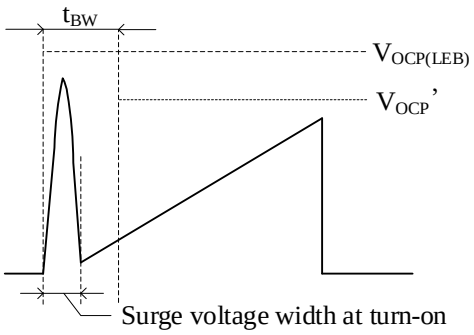

Figure 11-16. S/OCP Pin Voltage Waveform

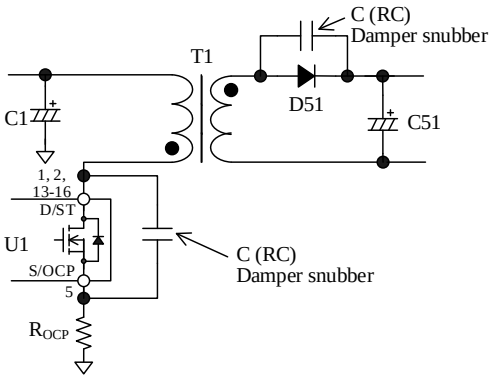

Figure 11-17. Damper Snubber

11.11.2. OCP Input Compensation Function

ICs commonly have propagation delay times; and a slope of the drain current becomes steeper as an AC input voltage to a power supply increases. Due to this, the higher the AC input voltage is, the steeper the slope of the peak drain current becomes. Consequently, the peak drain current during OCP operation tends to vary along with the AC input voltage.

To reduce such variation, the IC incorporates the OCP input compensation function.

The OCP input compensation function corrects the OCP threshold voltage depending on the AC input voltage, as shown in Figure 11-18.

When an AC input voltage is lower (a larger duty cycle), the IC sets a higher OCP threshold voltage to reduce the difference between peak drain currents at a higher AC input voltage (a smaller duty cycle) and a lower AC input voltage.

The amount of the correction depends on the duty cycle. Equation (6) determines the compensated OCP threshold voltage, V_{OCP}', which corresponds to the duty cycle. Note that, however, V_{OCP}' becomes constant at $V_{OCP(H)}$ = 0.888 V when the duty cycle is 36% or more.

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$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{ONDuty}{f_{OSC(AVG)}}. \quad (6)$$

Where:

$V_{OCP(L)}$ is the OCP threshold voltage at zero duty cycle,
DPC is the OCP compensation coefficient,
ONTime is the power MOSFET on-time,
ONDuty is the duty cycle of the power MOSFET, and
$f_{OSC(AVG)}$ is the average oscillation frequency.

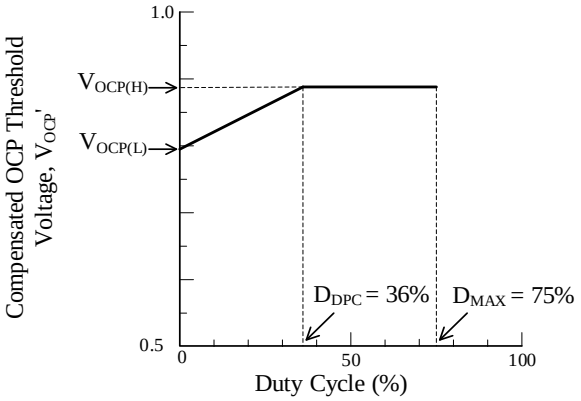

Figure 11-18 Duty Cycle vs. Compensated V_{OCP}

11.12. Overload Protection (OLP)

Figure 11-19 and Figure 11-20 show the FB/OLP pin peripheral circuit and the waveforms during OLP operation, respectively.

In an overload condition (where the peak drain current is limited by OCP operation), the secondary-side error amplifier is cut off due to a drop in the output voltage. As a result, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin, and the FB/OLP pin voltage increases. When the FB/OLP pin voltage exceeds and remains above $V_{FB(OLP)}$ = 7.3 V for t_{OLP} = 75 ms or longer, the overload protection (OLP) is activated to stop the switching operation.

During the OLP operation, the intermittent oscillation operation repeated by the VCC pin voltage reduces stress on components such as the power MOSFET or a secondary-side rectifier diode.

After the IC stops the switching operation by the OLP operation, the VCC pin voltage decreases.

Since the bias assist function is disabled during the OLP operation, the VCC pin voltage decreases to $V_{CC(OFF)SKP}$ (about 9 V) once and increases as the startup current flows through. When the VCC pin voltage increases to $V_{CC(ON)}$, the control circuit starts to operate. After the control circuit activation, the VCC pin voltage decreases due to the operating circuit current. When the VCC pin voltage reaches $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operating.

In this way, skipping $V_{CC(OFF)}$ during UVLO operation (see Section 11.2) lengthens a non-oscillating period and limits a temperature rise of the power MOSFET in the intermittent oscillation operation.

When the causes of the overload condition are eliminated, the IC automatically returns to normal operation.

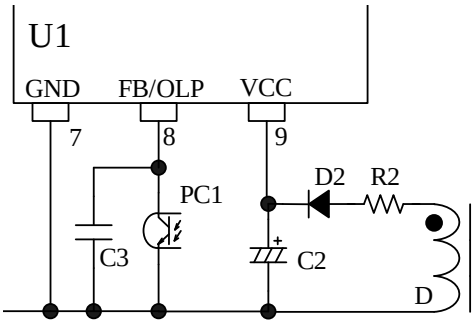

Figure 11-19. FB/OLP Pin Peripheral Circuit

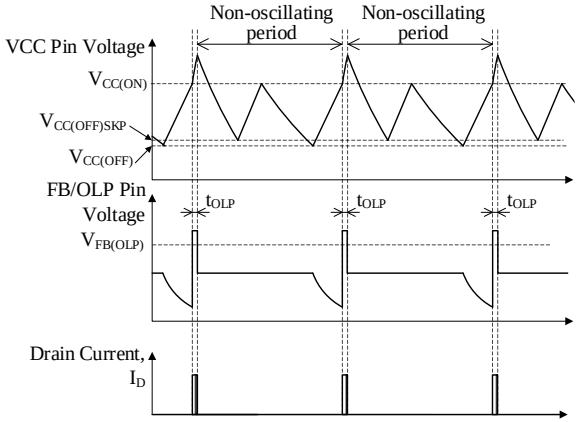

Figure 11-20. OLP Operational Waveforms

11.13. Overvoltage Protection (OVP)

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 29.1 V or more, the overvoltage protection (OVP) is activated to stop the switching operation. During the OVP operation, the bias assist function is disabled, and the intermittent operation by the UVLO is repeated (see Section 11.12). When the causes of the overvoltage condition are eliminated, the IC automatically returns to normal operation (see Figure 11-21).

When the VCC pin voltage is supplied through the auxiliary winding of the transformer, the VCC pin voltage is proportional to the output voltage. As a result,

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the VCC pin can detect a secondary-side overvoltage condition caused by abnormality (e.g., when an output voltage detection circuit is open). The approximate value of the secondary-side output voltage, $V_{OUT(OVP)}$, at the OVP activation can be calculated by Equation (7), below:

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.1\ (V). \quad (7)$$

Where:

$V_{OUT(NORMAL)}$ is the output voltage in normal operation, and

$V_{CC(NORMAL)}$ is the VCC pin voltage in normal operation.

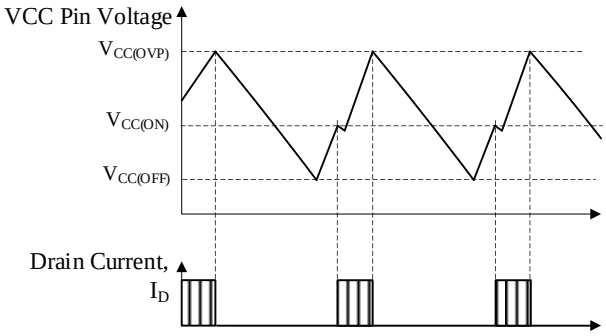

Figure 11-21. OVP Operational Waveforms

11.14. Thermal Shutdown (TSD)

Figure 11-22 shows operational waveforms of the thermal shutdown (TSD).

The TSD has the temperature hysteresis. When the control circuit temperature increases to $T_{J(TSD)}$ = 145 °C or more, the TSD is activated.

After the IC stops the switching operation by the TSD operation, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated to maintain the VCC pin voltage at $V_{CC(OFF)}$ or more.

When the junction temperature decreases to $T_{J(TSD)}-T_{J(TSD)HYS}$ or less, the bias assist function is disabled, and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops operating. After that, the control circuit resumes operating when the VCC pin voltage increases with a startup current and reaches $V_{CC(ON)}$.

In this way, the intermittent oscillation operation by the TSD and the UVLO is repeated in an overheating condition.

When the causes of the overheating condition are eliminated and the IC temperature decreases to $T_{J(TSD)}-T_{J(TSD)HYS}$ or less, the IC automatically returns to normal operation.

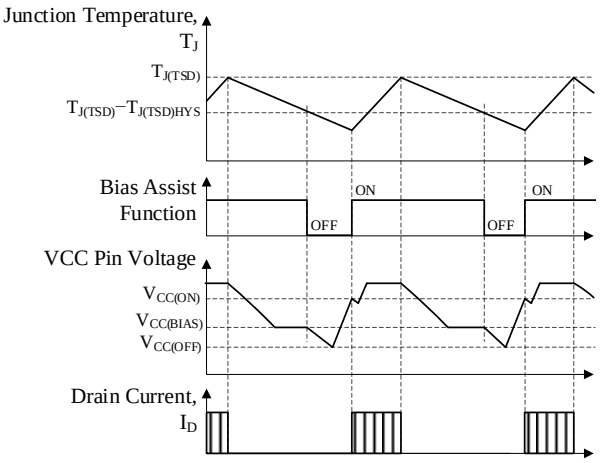

Figure 11-22. TSD Operational Waveforms

12. Design Notes

12.1. External Components

Components fit for the use condition should be used.

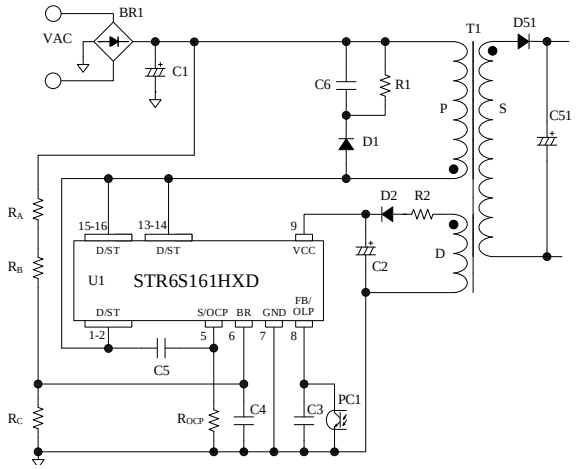

Figure 12-1. IC Peripheral Circuit

12.1.1. Input/Output Smoothing Electrolytic Capacitor

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

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12.1.2. S/OCP Pin Peripheral Circuit

R_{OCP} in Figure 12-1 is the resistor for current detection. It is required to use a resistor with low internal inductance because high-frequency switching current will flow through R_{OCP}. In addition, choose a resistor with allowable power dissipation according to your application.

12.1.3. BR Pin Peripheral Circuit

Note that the following must be taken into account because high voltages are applied to R_A and R_B in Figure 12-1.

- Select a resistor designed against electromigration according to the specifications of the application.
- Add resistors in series to reduce individual applied voltages.

Section 11.10 describes the AC input voltage protection functions and the peripheral circuit constants of the BR pin.

12.1.4. FB/OLP Pin Peripheral Circuit

The capacitor C3 between the FB/OLP and GND pins shown in Figure 12-1 is for high-frequency noise suppression and phase compensation. C3 should be about 2200 pF to 0.01 µF and connected close to the FB/OLP and GND pins. The constant of C3 should be adjusted based on the operation performance checked with an actual board.

12.1.5. VCC Pin Peripheral Circuit

In general power supply specifications, the capacitance of C2 shown in Figure 12-1 should be about 10 µF to 47 µF (C2 affects the startup time. See Section 11.1).

In actual power supply circuits, the overvoltage protection (OVP) may be activated due to fluctuation of the VCC pin voltage in proportion to the output current, I_{OUT} (see Figure 12-2). This happens because the transient surge voltage that occurs at power MOSFET turn-off induces a voltage across the auxiliary winding D. C2 is charged at the peak of the induced voltage.

To prevent the C2 peak charging, add R2 of about 2.2 Ω to 82 Ω, in series with D2 (see Figure 12-1). The optimal value of R2 should be determined with a transformer to be actually used because a variation in the VCC pin voltage over the output current depends on the transformer structure.

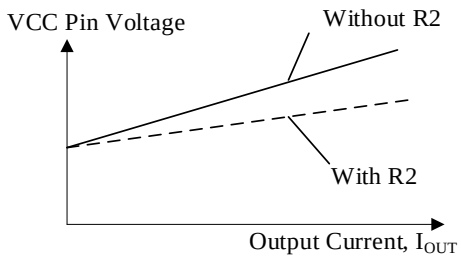

Figure 12-2. I_{OUT} vs V_{CC} with or without R2

12.1.6. Snubber Circuit

For the power supply specifications where V_{DS} will cause a high surge voltage, the following circuits should be added (see Figure 12-1):

- Add a clamp snubber circuit consisting of a capacitor-resistor-diode (CRD) combination across the primary-side main winding P.
- Add a damper snubber circuit consisting of a capacitor (C) or resistor-capacitor (RC) combination between the D/ST and S/OCP pins.

Note that the damper snubber circuit should be connected close to the D/ST and S/OCP pins.

12.1.7. Phase Compensation

Figure 12-3 shows the secondary-side detection circuit using a typical shunt regulator (U51). C52 and R53 are a capacitor and a resistor for phase compensation. C52 should have a capacitance of about 0.047 µF to 0.47 µF; R53 should have a resistance of about 4.7 kΩ to 470 kΩ. The constants of C52 and R53 should be adjusted based on the operation performance checked with an actual board.

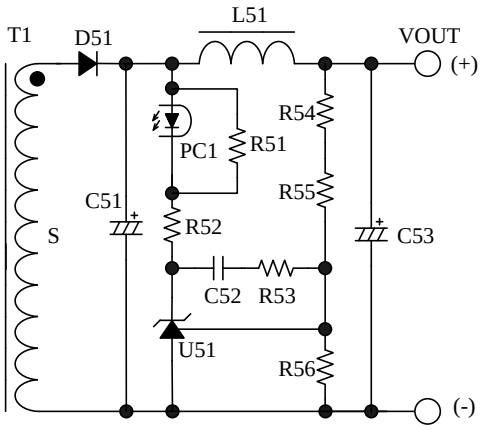

Figure 12-3. Peripheral Circuit of Secondary-side Shunt Regulator (U51)

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12.1.8. Transformer

Apply proper design margin to core temperature rise by core loss and copper loss. Because the switching currents contain high frequency currents, the skin effect may become a consideration.

For this reason, the wire diameter of a transformer winding should be selected by taking the RMS of the operating current into account, and the current density should be 4 A/mm^2 to 6 A/mm^2.

If the measures to further reductions in temperature are still necessary, the following should be taken into account to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of the VCC pin voltage becomes high:

- The surge voltage of the primary-side main winding P is high (low output voltage and high output current power supply designs).
- The winding structure of the auxiliary winding D is susceptible to the noise of the primary-side main winding P.

When the surge voltage of the auxiliary winding D is high, the VCC pin voltage increases, and the overvoltage protection (OVP) may be activated. In transformer designing, the following should be taken into account:

- Maximize the coupling of the primary-side main winding P and the secondary-side output winding S (to reduce the leakage inductance).
- Maximize the coupling of the auxiliary winding D and the secondary-side output winding S.
- Minimize the coupling of the auxiliary winding D and the primary-side main winding P.

In a multi-output power supply, the coupling between the secondary-side stabilizing output winding S1 and the others (S2, S3⋯) should be maximized to improve the line regulation of output voltages.

Figure 12-4 shows the winding structural examples of a two-output transformer.

- Winding Structural Example (a):

S1 is sandwiched between P1 and P2 to maximize their coupling and reduce a surge in P1 and P2.

D is wound away from P1 and P2 to minimize their coupling and reduce a surge in D.

- Winding Structural Example (b):

P1 and P2 are wound close to S1 to maximize their coupling and reduce a surge in P1 and P2.

D and S2 are sandwiched between S1s to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces a surge in D, thus improving the line regulation of the S2 output voltage.

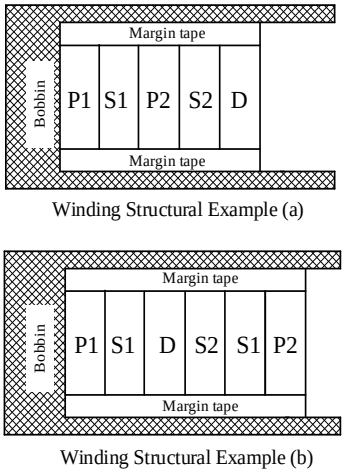

Figure 12-4. Winding Structural Examples

12.2. PCB Pattern Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced. The following considerations also should be taken into account in designing pattern layouts for your application.

Figure 12-5 is a peripheral circuit example of the IC.

(1) Main Circuit Trace Layout

Traces connected to the main circuit, where switching currents pass through, should be as wide and looped as small as possible.

If the IC and C1 are distant from each other, add an electrolytic capacitor or a film capacitor (about 0.1 μF) close to the transformer or the IC to reduce impedance of the high frequency current loop.

(2) Logic Ground Trace Layout

If a large current flows through a logic ground, the IC malfunction may be caused. Therefore, connect the logic ground traces as close as possible to R_{OCP} at a single-point ground (point A in Figure 12-5) and separate them from the power ground.

(3) Peripheral Connections to the VCC Pin

Traces connected to the VCC pin should be looped as small as possible because the pin supplies power to the IC. If the IC and C2 are distant from each other or additional noise filter capacitors are required, connect a high-frequency ceramic capacitor

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(equivalent to X7R; about 0.1 µF to 1.0 µF) between the VCC and GND pins with a minimum length of trace.

(4) Peripheral Connections to R_{OCP}

R_{OCP} should be placed as close as possible to the S/OCP pin. Traces of the main circuit and the logic ground should be connected at a single-point ground (point A in Figure 12-5) which is close to the root of R_{OCP}.

(5) Peripheral Components of the IC

Control components that are to be connected to the IC should be placed as close as possible to the IC and connected to each pin with a minimum length of trace.

(6) Secondary-side Rectifier Smoothing Circuit

Traces connected to the secondary-side main circuit, where switching currents pass through, should be as wide and looped as small as possible. Lowering the impedance of these traces can reduce the surge voltage at power MOSFET turn-off. Therefore, a proper rectifier smoothing trace layout permits your application to have an increased margin to the power MOSFET breakdown voltage and reduced component stress and loss in the clamp snubber circuit.

(7) Thermal Considerations

Extreme care must be taken in thermal design because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$.

Traces under the IC or connected to the D/ST pin must be as wide as possible because these traces act as heatsinks.

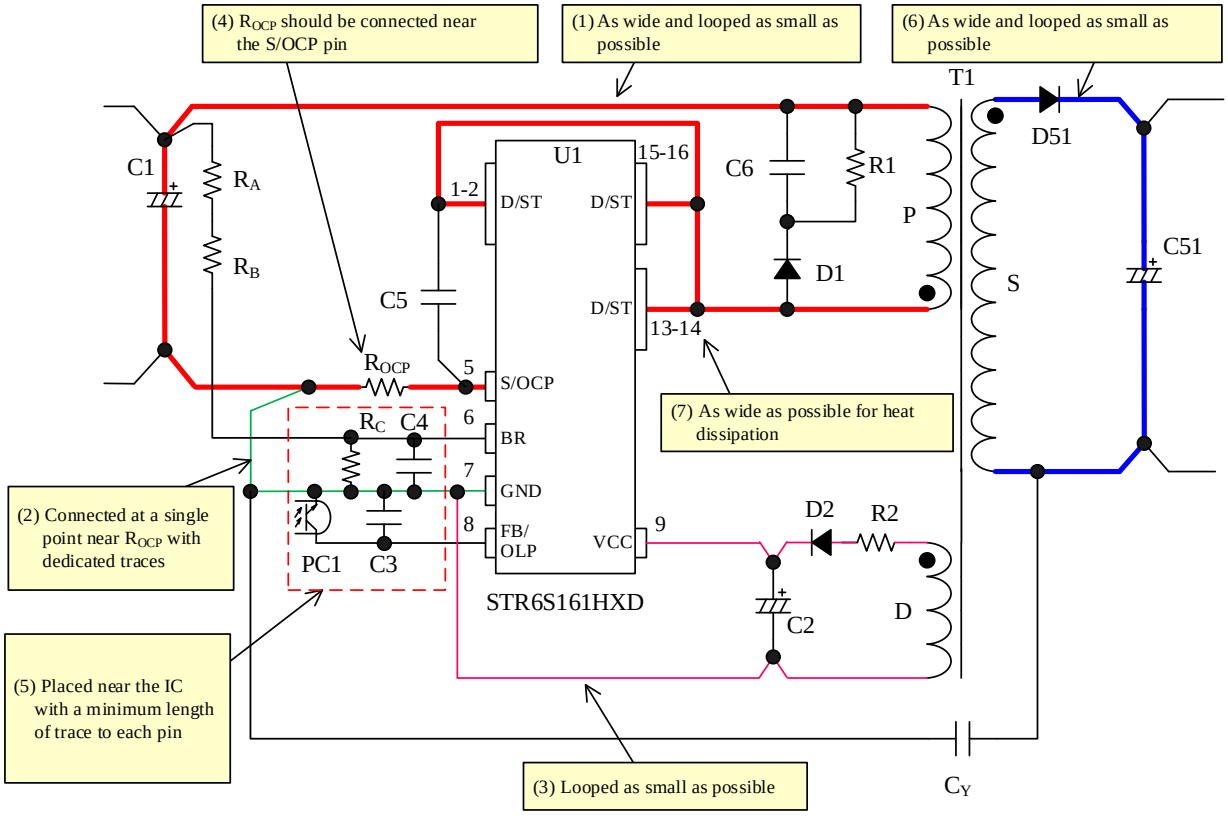

Figure 12-5. Example Connections to the IC and Its Peripheral Circuits

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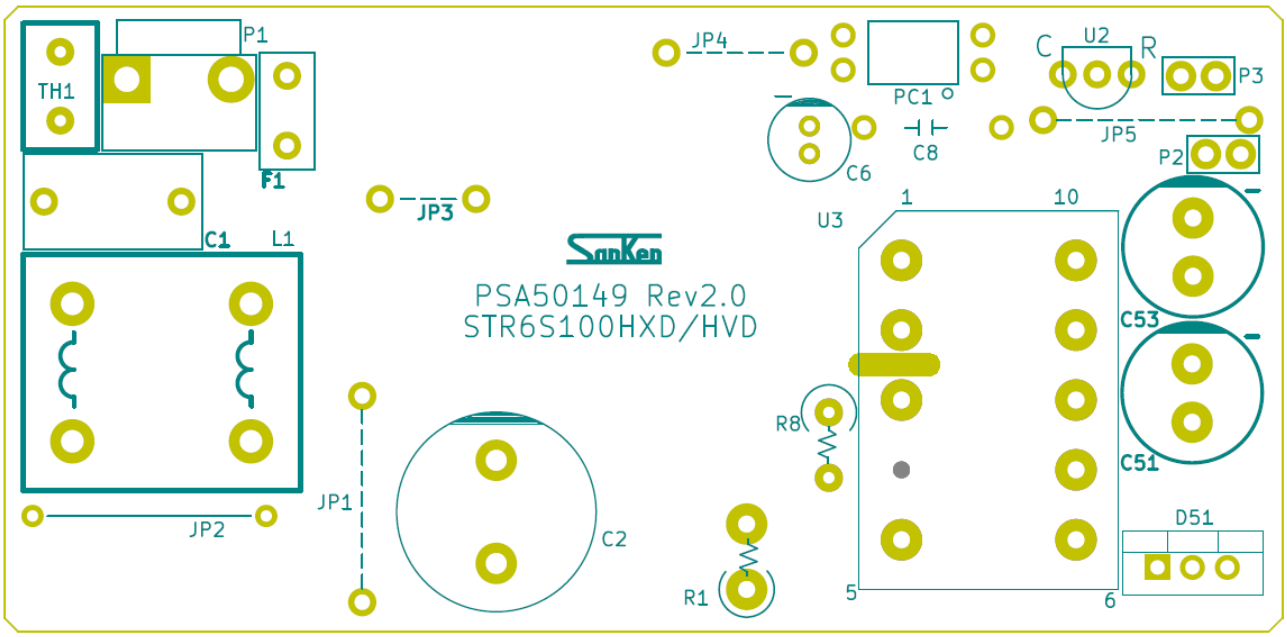
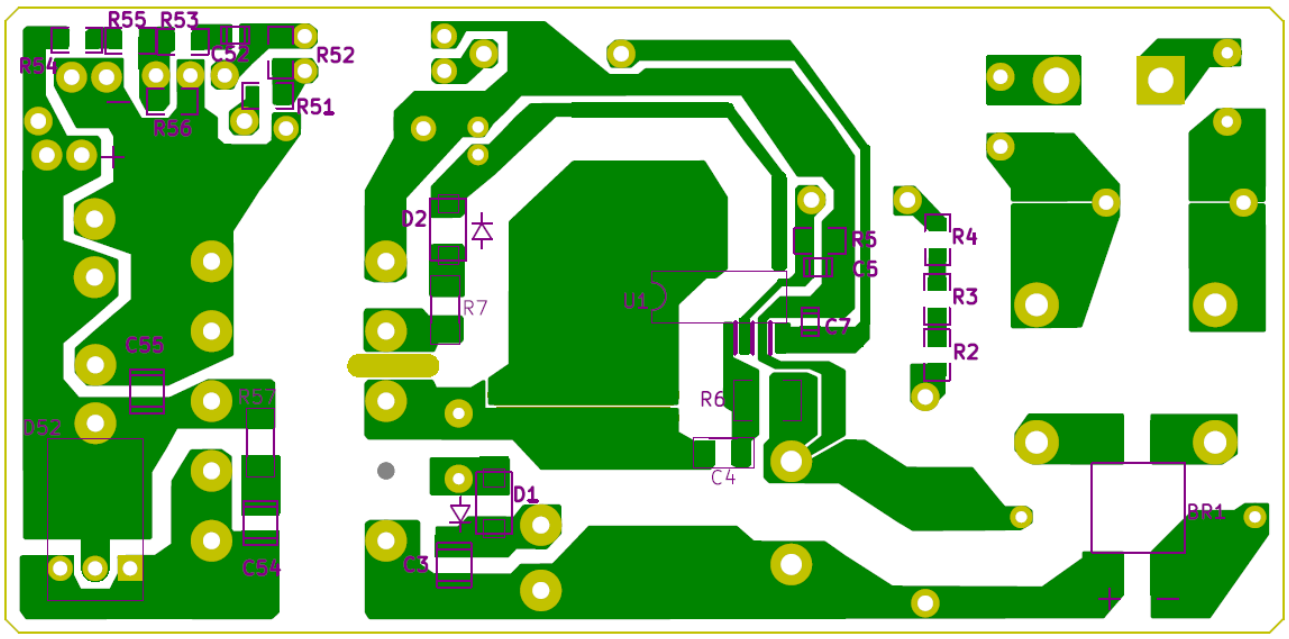
13. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using the STR6S161HXD.



(a) Top View



(b) Bottom View

Figure 13-1. Pattern Layout Example

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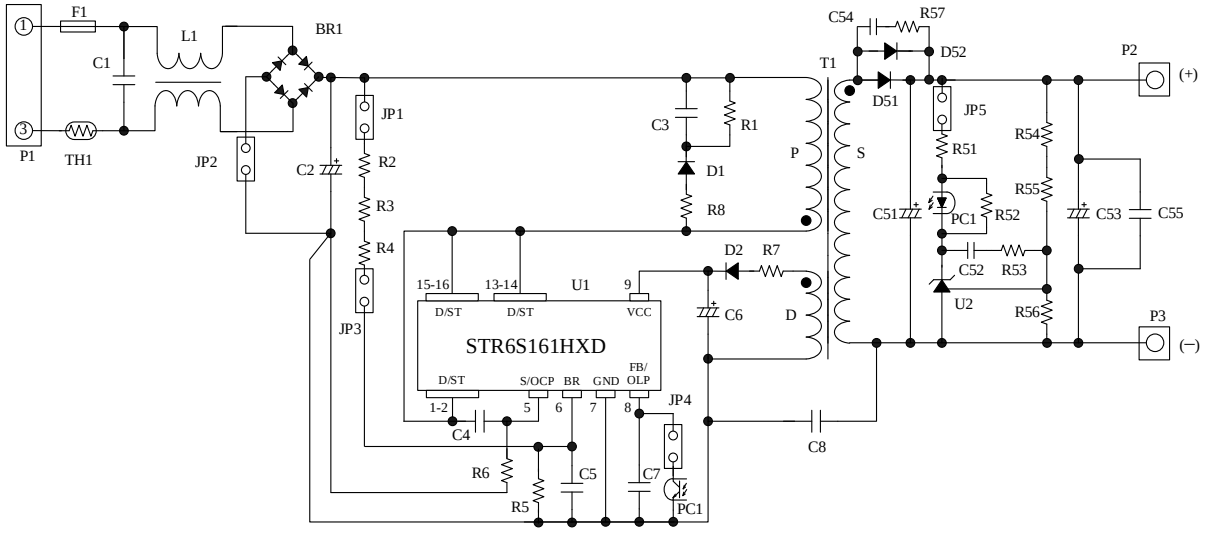

Figure 13-2. Circuit Diagram of PCB Pattern Layout Example

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