TLE4275-Q1 Automotive, 500mA, 40V, Low-Dropout Regulator With Power-Good

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range:
  - Legacy chip: 5.5V to 42V (45V absolute max)
  - New chip: 3.0V to 40V (42V absolute max)
- Maximum output current:
  - Legacy chip: 450mA
  - New chip: 500mA
- Output voltage accuracy: ±2.0% (across line, load and temperature)
- Low dropout voltage: 500mV (max) at 300mA
- Low quiescent current:
  - Legacy chip: 100µA (typ) at I_{OUT} = 1mA
  - New chip: 28µA (typ) at I_{OUT} = 1mA
- Excellent line transient response (new chip):
  - ±2% V_{OUT} deviation during cold-crank
  - ±2% V_{OUT} deviation (1V/µs V_{IN} slew rate)
- Power-good (reset) with programmable delay period
- Stable with a 2.2µF or larger capacitor (new chip)
- Reverse-polarity protection (legacy chip)
- Overcurrent and overtemperature protection
- Packages:
  - 5-pin TO-252 (KVU)
  - 5-pin DDPAK/TO-263 (KTT)
  - 20-pin HTSSOP (PWP) (legacy chip)

2 Applications

- Reconfigurable instrument clusters
- Body control modules (BCM)
- Always-on, battery-connected applications:
  - Automotive gateways
  - Remote keyless entries (RKE)

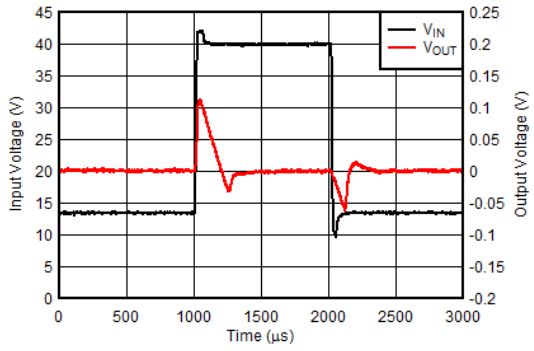
3 Description

The TLE4275-Q1 is a low-dropout linear regulator designed to connect to the battery in automotive applications. For the new chip, the device has an input voltage range extending to 40V that drives loads up to 500mA. This range allows the device to withstand transients (such as load dumps) that are anticipated in automotive systems. With only a 28µA quiescent current at I_{OUT} = 1mA (new chip), the device is designed for powering always-on components. Microcontrollers (MCUs) and controller area network (CAN) transceivers in standby systems are examples of such components.

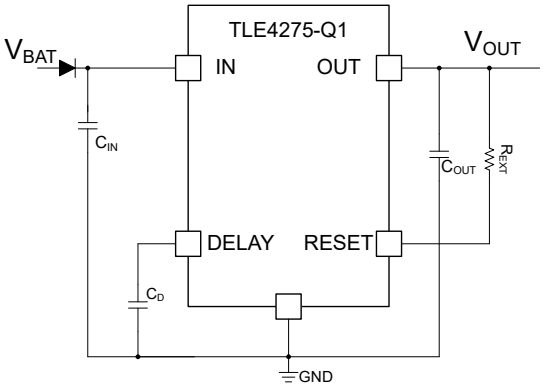
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLE4275-Q1	KTT (DDPAK/ TO-263, 5)	10.16mm × 15.24mm
	KVU (TO-252, 5)	6.6mm × 10.11mm
	PWP (HTSSOP, 20) (3)	6.5mm × 6.4mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Legacy chip.



Line Transient Response (3V/µs V_{IN} Slew Rate) (New Chip)



Typical Application

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The new chip version of the device has state-of-the-art transient response that allows the output to quickly react to changes in load or line (for example, during cold-crank conditions). Additionally, the new chip version has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±2.0% over line, load, and temperature (new chip).

The power-good (reset) delay is adjusted by an external capacitor on the delay pin, allowing the delay time to be configured to fit application-specific systems.

The device also incorporates a number of internal circuits for protection against overload and overtemperature. The legacy chip also provides protection against reverse polarity. The legacy chip requires $C_{OUT} \geq 22\mu F$ with max supported ESR range of ≤ 5Ω and new chip requires COUT ≥ 2.2µF with max supported ESR range of ≤ 2Ω, within the operating temperature range.

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4 Pin Configuration and Functions

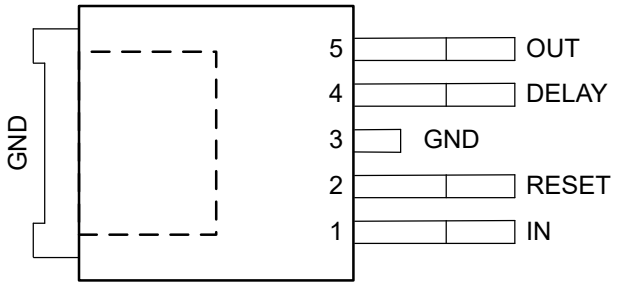


Figure 4-1. KVU Package, 5-Pin TO-252 (Top View)

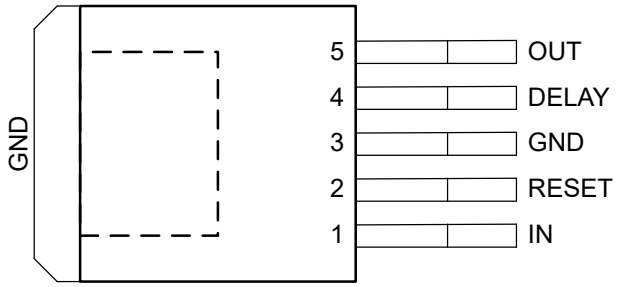


Figure 4-2. KTT Package, 5-Pin DDPAK/TO-263 (Top View)

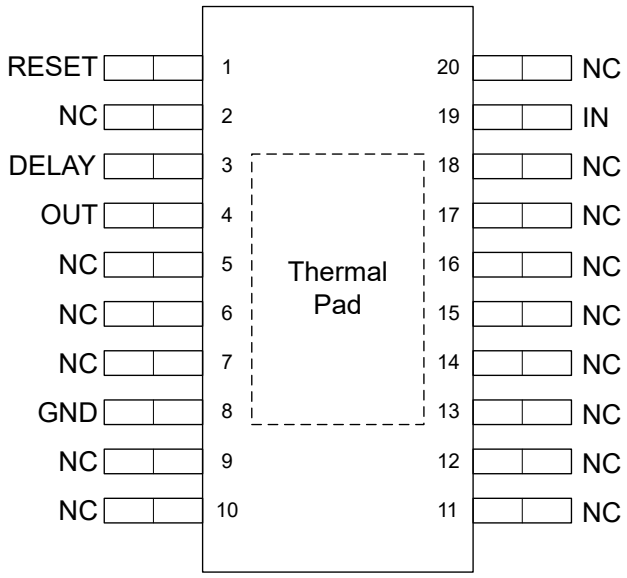


Figure 4-3. PWP Package, 20-Pin HTSSOP (Top View, Legacy Chip)

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Table 4-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	KVU	KTT	PWP		
DELAY	4	4	3	I	Reset (power-good) delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay. Leave this pin floating for a default ($t_{(DLY_FIX)}$) delay. See the *Power-Good Reset (RESET)* section for more information. If RESET/DELAY functionality is not desired, leave this pin floating because connecting this pin to GND causes a permanent increase in the GND current.
GND	3	3	8	G	Ground reference.
IN	1	1	19	P	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the input of the device as possible.
NC	—	—	2, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 20	—	No internal connection. This pin can be left floating, or connected to GND for best thermal performance
OUT	5	5	4	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. Increasing the output capacitance from the minimum value required for stability results in improved transient response. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible. If using a high equivalent series resistance (ESR) capacitor, decouple the output with a 100nF ceramic capacitor.
RESET	2	2	1	I	Reset (power-good) pin with active-high functionality. An open-drain output indicates when the output voltage reaches $V_{PG(TH,RISING)}$ of the target. Using a feed-forward capacitor disrupts RESET functionality. See the *Power-Good Reset (RESET)* section for more information.
Thermal pad	Pad	Pad	Pad	—	Connect the thermal pad to a large area GND plane for improved thermal performance.

(1) I = input; O = output; P = power; G = ground.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range (for legacy chip)	–42	45	V
	Input voltage range (for new chip)	–0.3	42	
V_{OUT}	Output voltage range (for legacy chip)	–1	16	V
	Output voltage range (for new chip)	–0.3	V_{IN} + 0.3(2)	
DELAY	Reset delay input (for legacy chip)	–0.3	7	V
	Reset delay input, power-good adjustable threshold (for new chip)	–0.3	6	
RESET	Reset output (for legacy chip)	–0.3	25	V
	Reset (power-good) output (for new chip)	–0.3	20	
I_{DELAY}	DELAY current (for legacy chip)		±2	mA
I_{RESET}	RESET current (for legacy chip)		±5	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 20 V, whichever is smaller.

5.2 ESD Ratings

				VALUE (Legacy Chip)	VALUE (New chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±6000	±2000	V
		Machine model (MM)		±400	±500	
		Charged-device model (CDM), per AEC Q100-011	All pins	N/A	±500	
			Corner pins	N/A	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range (for legacy chip)	5.5		42	V
	Input voltage range (for new chip)	3		40	
V_{OUT}	Output voltage		5.0		V
I_{OUT}	Output current range (for new chip)	0		500	mA
V_{DELAY}	Delay pin voltage, power-good adjustable threshold (for new chip)	0		5.5	V
V_{RESET}	Reset (power-good) output pin (for new chip)	0		18	
C_{OUT}	Output capacitor (for legacy chip)	22			µF
	Output capacitor (for new chip) (2)	2.2		220	
ESR	Output capacitor ESR requirements (for legacy chip)	0.001		5	Ω
	Output capacitor ESR requirements (for new chip)	0.001		2	
C_{IN}	Input capacitor (for new chip)(1)	0.1	1		µF
C_{DELAY}	Power-good delay capacitor (for new chip)			1	µF
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance is 500 nF.
(2) Effective output capacitance of 1 µF minimum required for stability.

5.4 Thermal Information

THERMAL METRIC (1)		TLE4275-Q1					UNIT
		KVU (TO-252-5)		KTT (TO-263-5)		PWP (HTSSOP-20)	
		Legacy Chip	New Chip	Legacy Chip	New Chip	Legacy Chip	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	28.6	32.8	22.5	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	36.3	38.0	7.2	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	7.3	5.3	32.3	19.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	1.8	6.3	2.0	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.1	7.2	5.4	3.4	18.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	0.7	0.8	6.8	1.5	°C/W

(1) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered tothe thermal land pattern. Also, correct attachment procedure must be incorporated.

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5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 0 mA, COUT = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, C_{IN} = 1µF, typical values are at T_J = 25°

PARAMETER		Test Conditions		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	V_{IN} = 6V to 28V, I_{OUT} = 5mA to 400mA		4.9	5	5.1	V
		V_{IN} = 6V to 40V, I_{OUT} = 5mA to 200mA		4.9	5	5.1	
I_O	Output current limit			450	700	950	mA
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (for legacy chip)	I_{OUT} = 5mA to 400mA			15	30	mV
	Load regulation (for new chip)	I_{OUT} = 5mA to 400mA, V_{IN} = 6V			15	30	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (for legacy chip)	V_{IN} = 8V to 32V, I_{OUT} = 5mA		–15	5	15	mV
	Line regulation (for new chip)	V_{IN} = 6V to 40V, I_{OUT} = 5mA		–15	5	15	
I_Q	Current consumption, $I_Q = I_{IN} - I_{OUT}$ (for legacy chip)	I_{OUT} = 1mA	T_J = 25ºC		150	200	µA
			T_J ≤ 85ºC		150	220	
	Current consumption, $I_Q = I_{IN} - I_{OUT}$ (for new chip)		T_J = 25ºC		28	50	
			T_J ≤ 85ºC		28	55	
	Current consumption, $I_Q = I_{IN} - I_{OUT}$	I_{OUT} = 250mA			5	10	mA
		I_{OUT} = 400mA			12	22	
V_{DO}	Dropout voltage	I_{OUT} = 300mA, $V_{DO} = V_{IN} - V_{OUT}$			250	500	mV
$V_{UVLO(RISING)}$	Rising input supply UVLO (for new chip)	V_{IN} rising		2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO (for new chip)	V_{IN} falling		2.38	2.5	2.6	V
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis (for new chip)				230		mV
PSRR	Power-supply rejection ratio	frequency = 100Hz, V_r = 0.5 V_{pp}			60		dB
$\Delta V_{OUT}/\Delta T$	Temperature output voltage drift				0.5		mV/K
$V_{RESET(OL)}$	RESET (PG) pin low-level output voltage (for legacy chip)	R_{ext} ≥ 5kΩ, V_{OUT} > 1V			0.2	0.4	V
	RESET (PG) pin low-level output voltage (for new chip)	R_{ext} ≥ 5kΩ, 1V ≤ V_{OUT} < 4.5V			0.2	0.4	
$V_{OUT(RT)}$	RESET (PG) switching threshold (for legacy chip)			4.5	4.65	4.8	V
	RESET (PG) switching threshold (for new chip)	V_{OUT} rising		4.25		4.75	
I_{ROH}	RESET output leakage current	V_{ROH} = 5V			0	10	µA
$I_{DLY(CHARGE)}$	RESET charging current (for legacy chip)	Voltage at DELAY pin = 1V		3	5.5	9	µA
	RESET charging current (for new chip)			1	1.5	2	
$V_{DELAY_U\ (TH)}$	RESET upper timing threshold (for legacy chip)	Voltage at DELAY pin rising		1.5	1.8	2.2	V
	RESET upper timing threshold (for new chip)	Voltage at DELAY pin rising		1.17	1.21	1.25	
$V_{DELAY_RL\ (TH)}$	RESET lower timing threshold (for legacy chip)	Voltage at DELAY pin rising		0.2	0.4	0.7	V
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature (for new chip)				175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown (for new chip)				20		°C

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5.6 Timing Diagrams

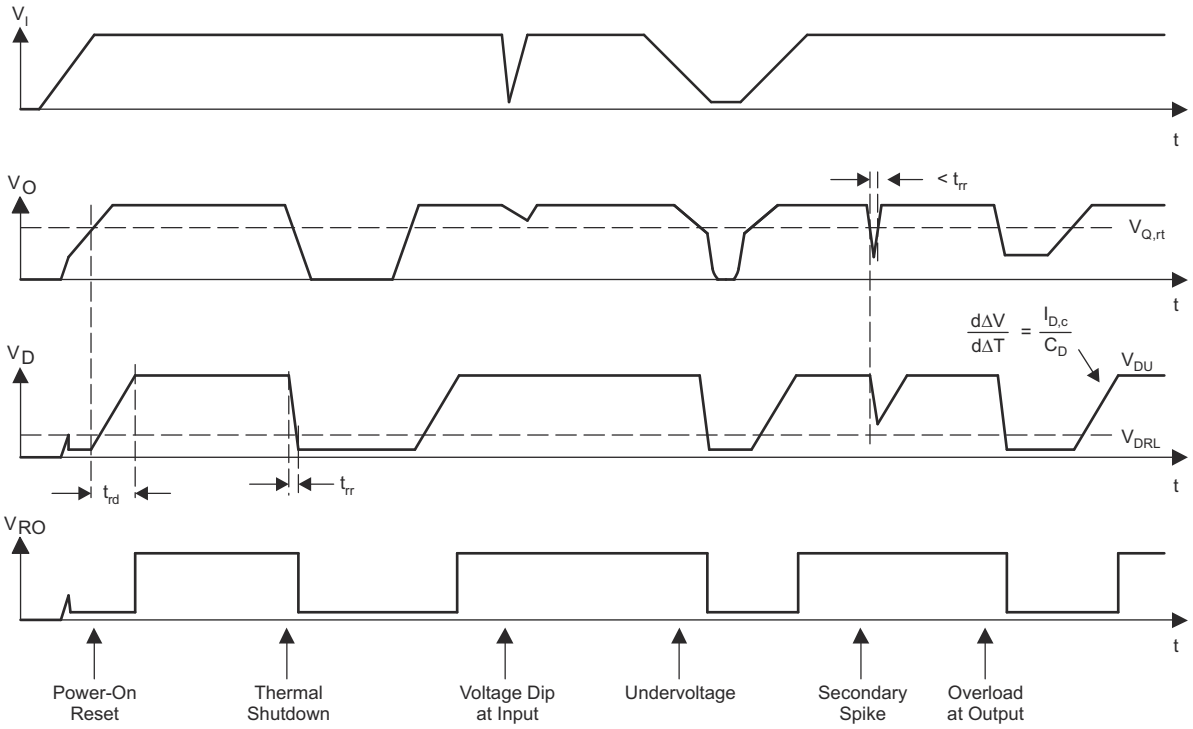
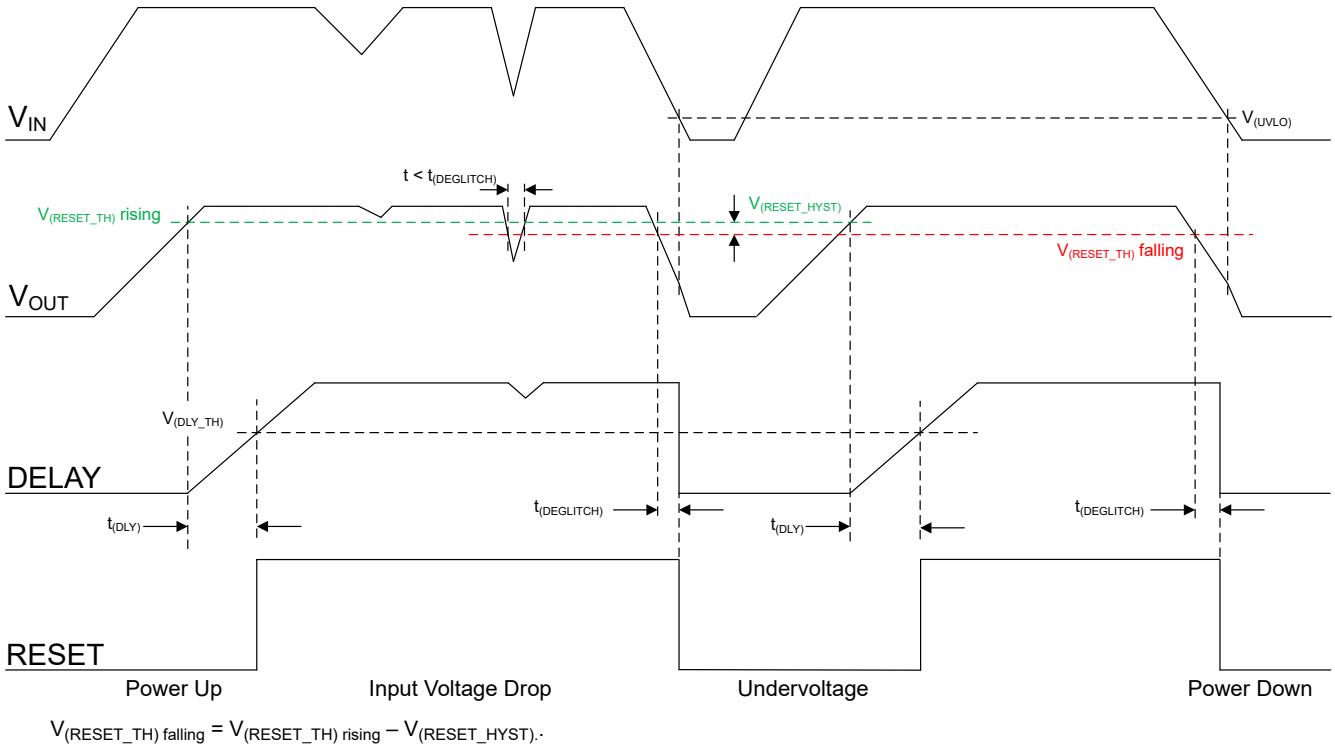


Figure 5-1. Reset Timing Diagram (Legacy Chip)



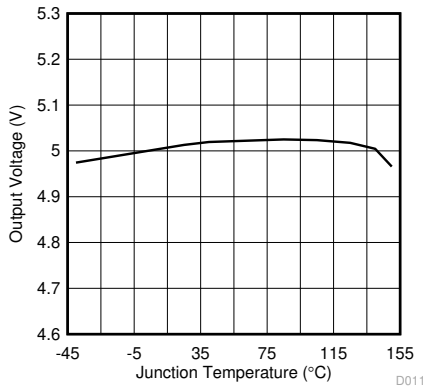
$V_{(RESET_TH)\ falling} = V_{(RESET_TH)\ rising} - V_{(RESET_HYST)}$.

Figure 5-2. Typical Power-Good RESET Timing Diagram (New Chip)

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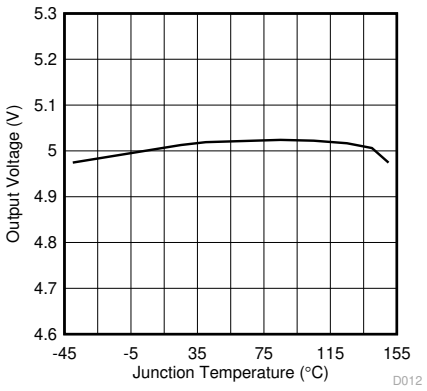
5.7 Typical Characteristics

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



V_{IN} = 6V

Figure 5-3. Output Voltage vs Junction Temperature (Legacy Chip)



V_I = 28V

Figure 5-4. Output Voltage vs Junction Temperature (Legacy Chip)

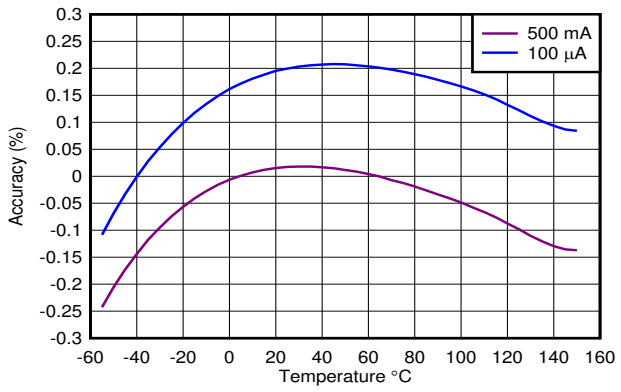


Figure 5-5. Output Accuracy vs Temperature (New Chip)

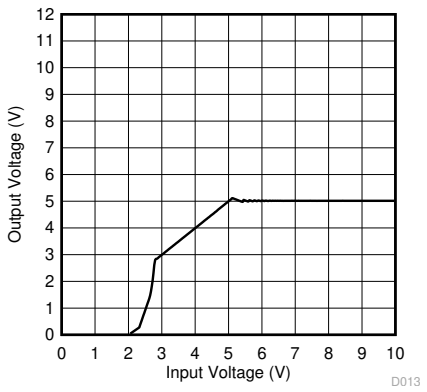
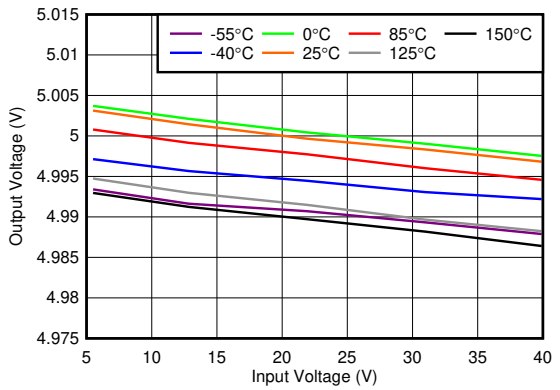
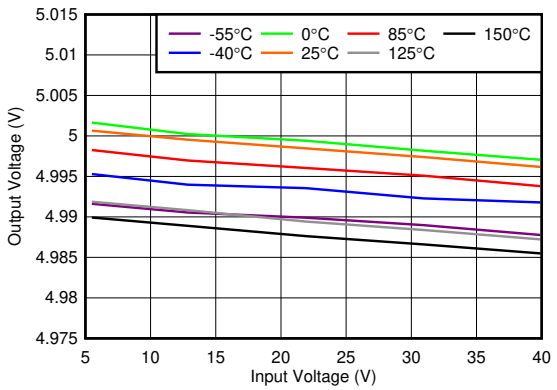


Figure 5-6. Output Voltage vs Input Voltage (Legacy Chip)



V_{OUT} = 5V, I_{OUT} = 150mA

Figure 5-7. Output Line Regulation vs V_{IN} (New Chip)



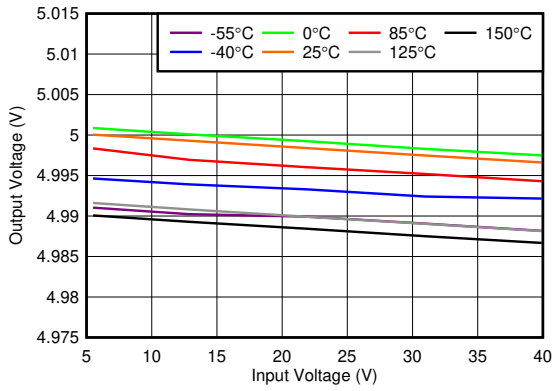
V_{OUT} = 5V, I_{OUT} = 5mA

Figure 5-8. Line Regulation vs V_{IN} (New Chip)

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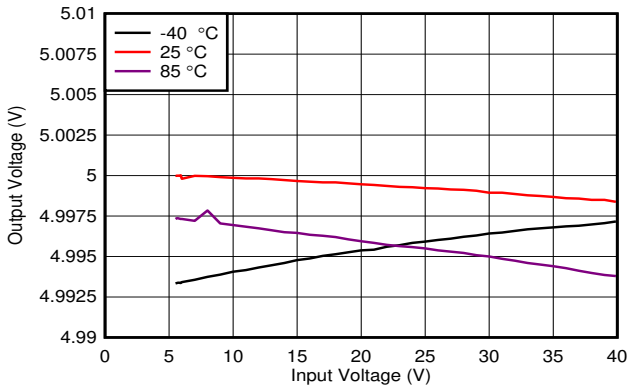
5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



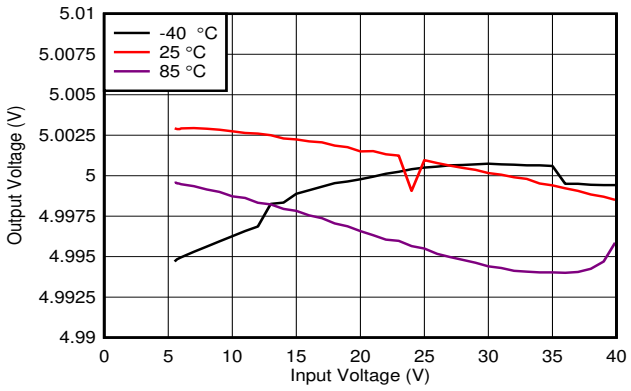
V_{OUT} = 5V, I_{OUT} = 1mA

Figure 5-9. Line Regulation vs V_{IN} (New Chip)



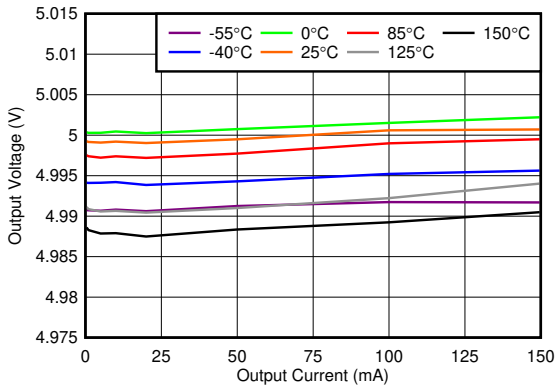
C_{OUT} = 10µF, V_{OUT} = 5V

Figure 5-10. Line Regulation at 50mA (New Chip)



C_{OUT} = 10µF, V_{OUT} = 5V

Figure 5-11. Line Regulation at 100mA (New Chip)



V_{OUT} = 5V

Figure 5-12. Load Regulation vs I_{OUT} (New Chip)

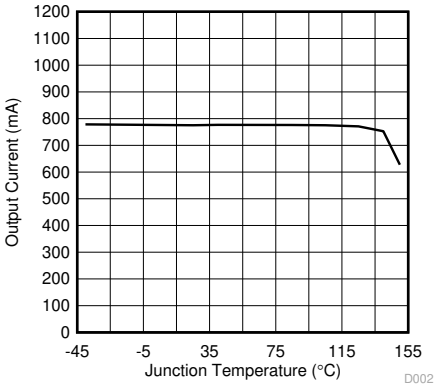
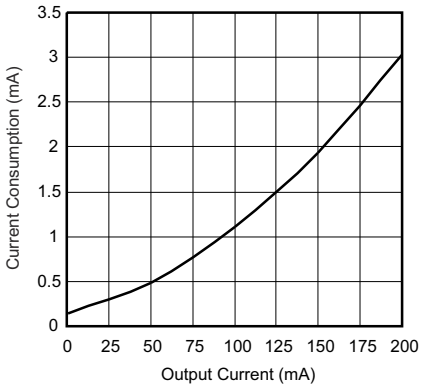


Figure 5-13. Output Current vs Junction Temperature (Legacy Chip)

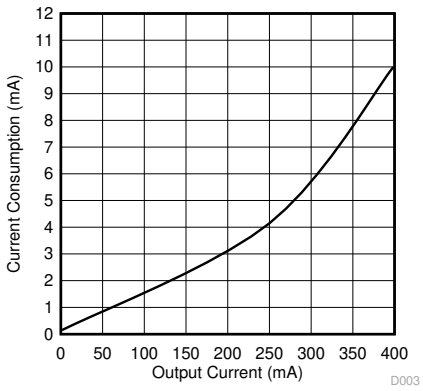


V_I = 13.5V

Figure 5-14. Current Consumption vs Output Current (Legacy Chip)

5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



V_I = 13.5V

Figure 5-15. Current Consumption vs Output Current (Legacy Chip)

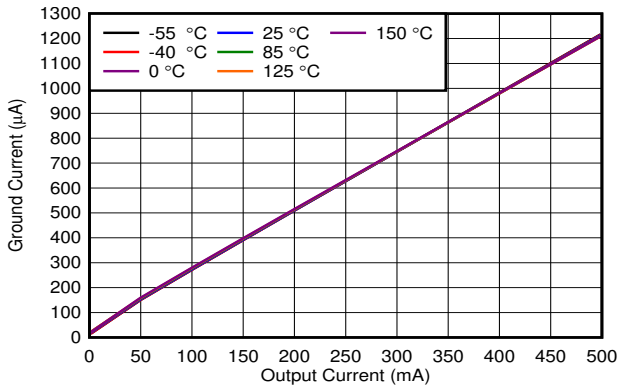


Figure 5-16. Ground Current (I_{GND}) vs I_{OUT} (New Chip)

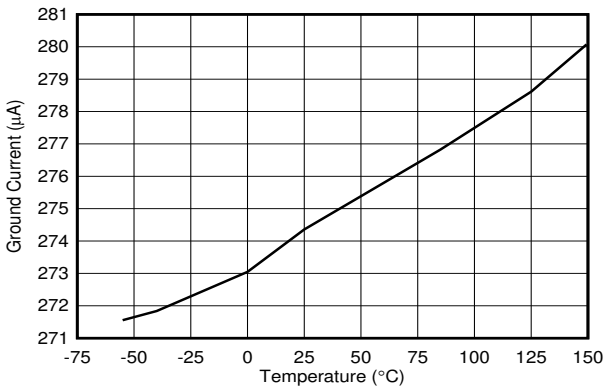


Figure 5-17. Ground Current at 100mA (New Chip)

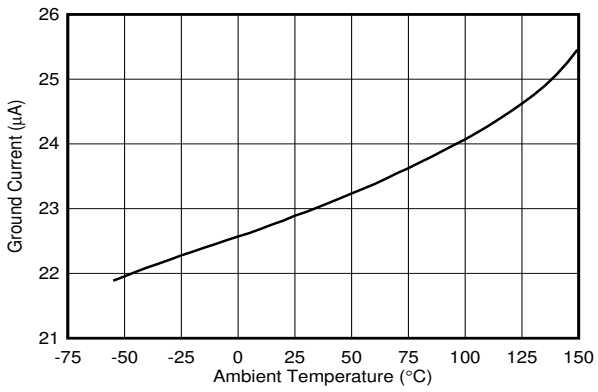
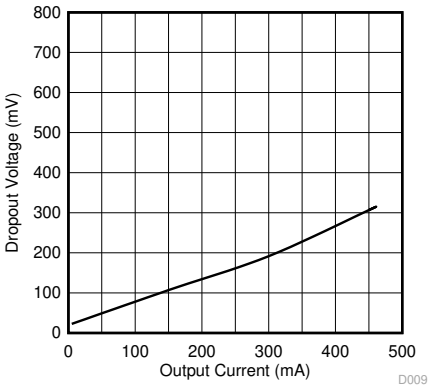
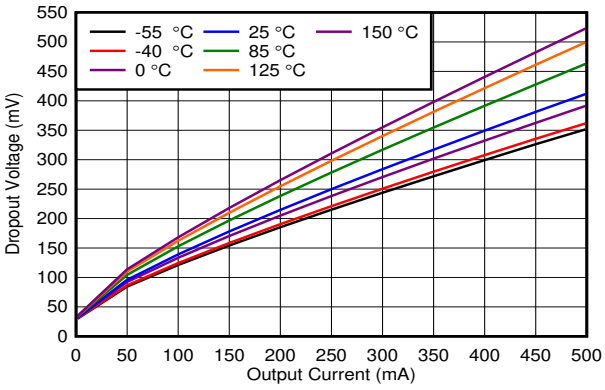


Figure 5-18. Ground Current at 500µA (New Chip)



T_J = 25°C

Figure 5-19. Dropout Voltage (V_{do}) vs Output Current (Legacy Chip)



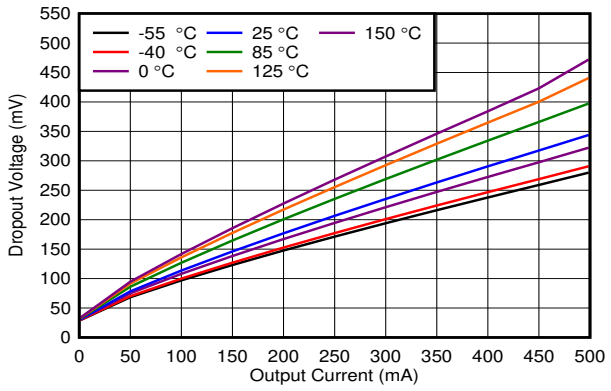
V_{IN} = 3V

Figure 5-20. Dropout Voltage (V_{DO}) vs I_{OUT} (New Chip)

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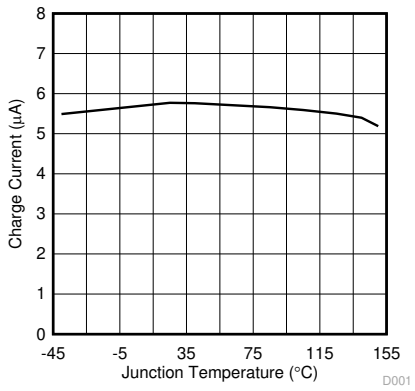
5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



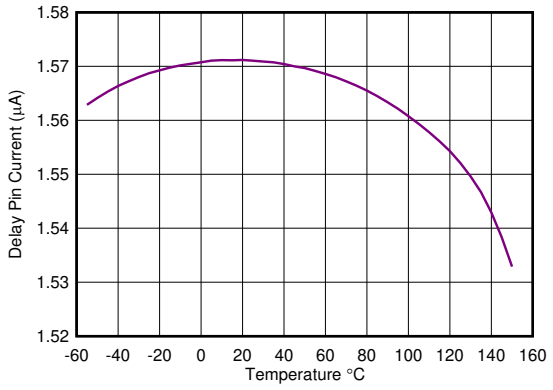
V_{IN} = 20V

Figure 5-21. Dropout Voltage (V_{DO}) vs I_{OUT} (New Chip)



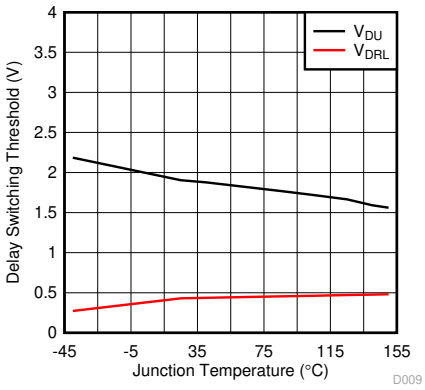
V_I = 13.5V, V_D = 1V

Figure 5-22. Charge Current ($I_{D,C}$) vs Junction Temperature (Legacy Chip)



V_{DELAY} = 1V

Figure 5-23. Delay Pin Current vs Temperature (New Chip)



V_I = 13.5 V

Figure 5-24. Delay Switching Threshold vs Junction Temperature (Legacy Chip)

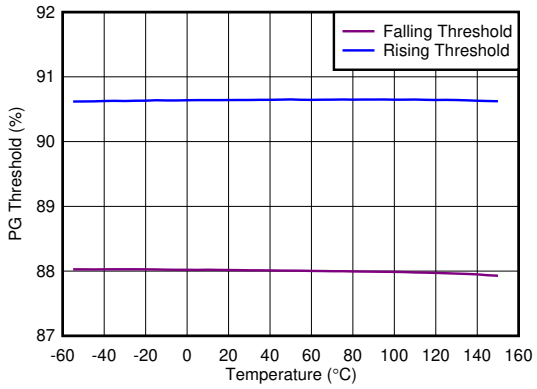
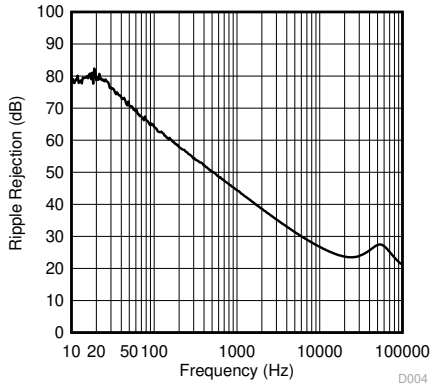


Figure 5-25. RESET (PG) Threshold vs Temperature (New Chip)



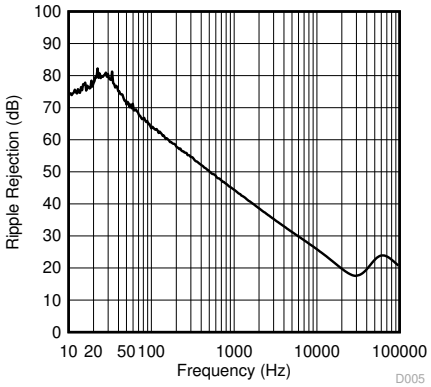
V_{IN} = 13.5V, I_{Load} = 1mA, C_{OUT} = 22µF

Figure 5-26. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

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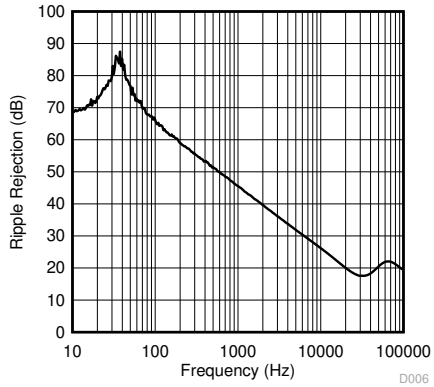
5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



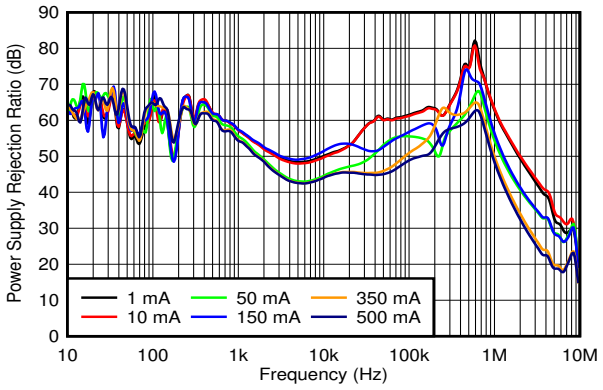
V_{IN} = 13.5V, I_{Load} = 200mA, C_{OUT} = 22µF

Figure 5-27. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)



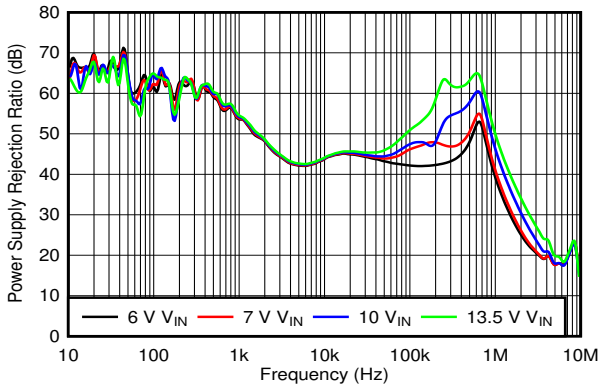
V_{IN} = 13.5V, I_{Load} = 400mA, C_{OUT} = 22µF

Figure 5-28. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)



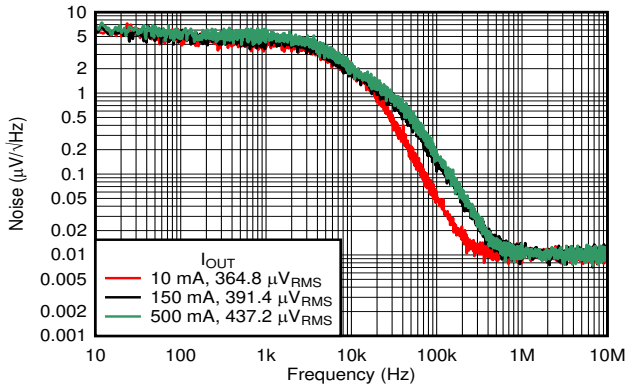
C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 5-29. Power-Supply Ripple Rejection vs Frequency and I_{OUT} (New Chip)



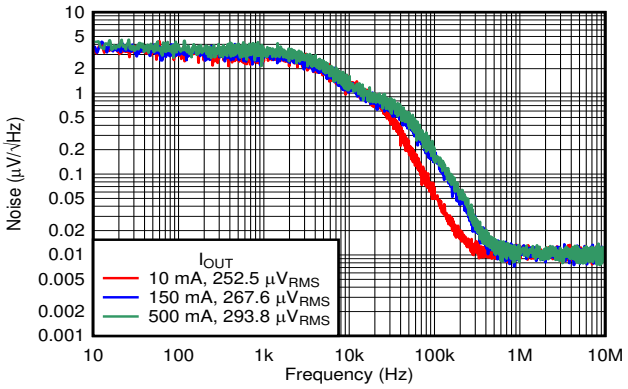
C_{OUT} = 10µF (X7R 50V), I_{OUT} = 500mA, V_{OUT} = 5V

Figure 5-30. Power-Supply Ripple Rejection vs Frequency and V_{IN} (New Chip)



C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 5-31. Noise vs Frequency (New Chip)



C_{OUT} = 10µF (X7R 50V), V_{OUT} = 3.3V

Figure 5-32. Noise vs Frequency (New Chip)

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5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)

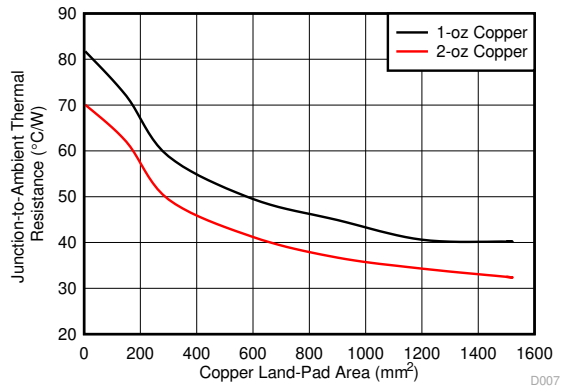


Figure 5-33. Thermal Resistance vs Copper Land Pad Area (JEDEC 51-3 Low-K Board) (Legacy Chip)

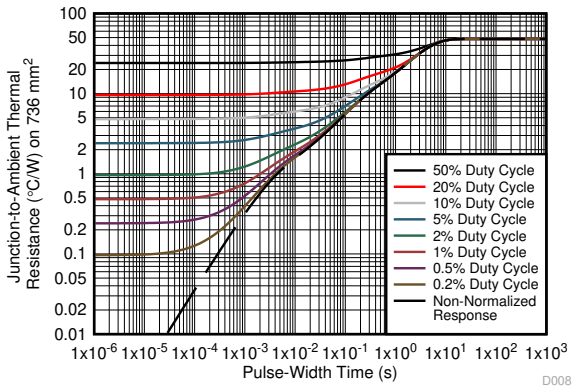


Figure 5-34. Thermal Resistance vs Pulse Duration for Various Duty Cycles (Legacy Chip)

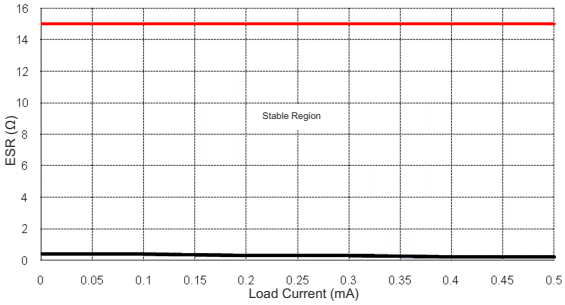


Figure 5-35. ESR Stability vs Load Current (Legacy Chip)

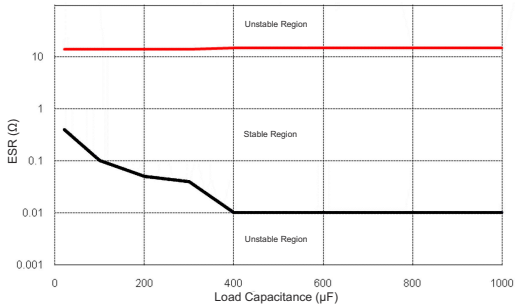


Figure 5-36. ESR Stability vs Load Capacitance (Legacy Chip)

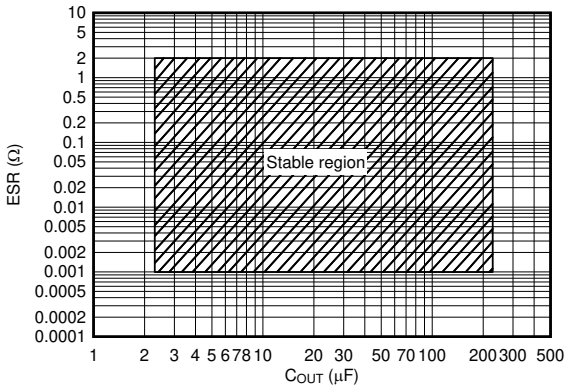
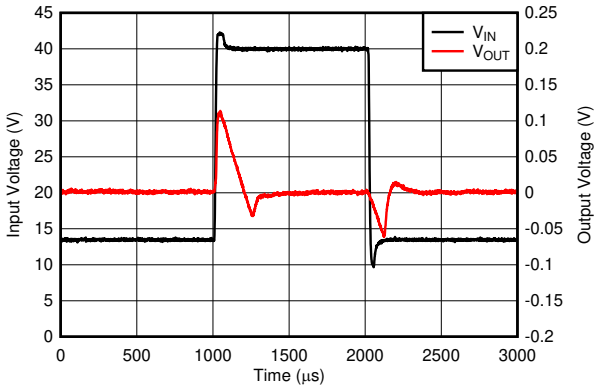


Figure 5-37. Stability, ESR vs C_{OUT} (New Chip)

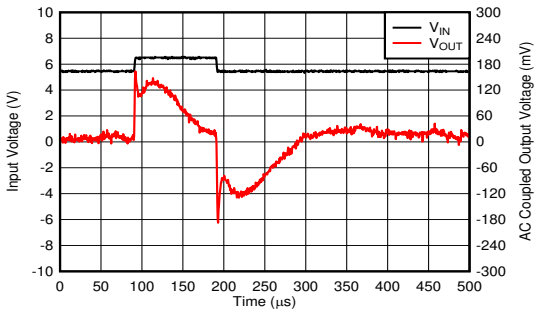


V_{OUT} = 5V, I_{OUT} = 1mA, V_{IN} = 13.5V to 45V, slew rate = 2.7V/µs

Figure 5-38. Line Transients (New Chip)

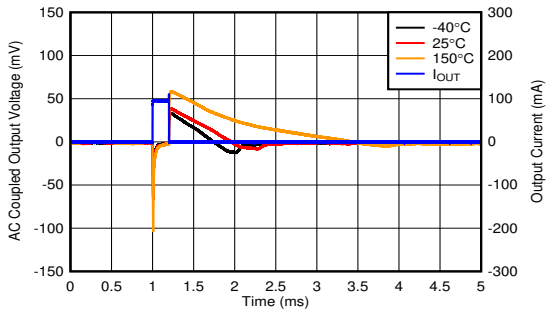
5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



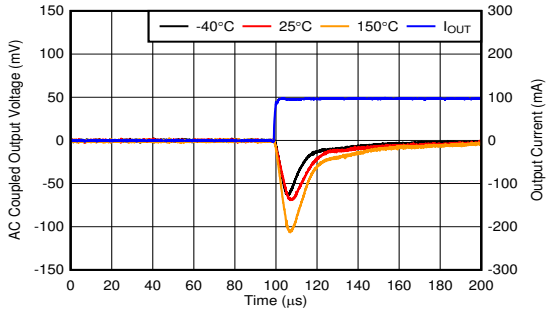
V_{OUT} = 5V, I_{OUT} = 100mA, V_{IN} = 5.5V to 6.5V, rise time = 1µs

Figure 5-39. Line Transients (New Chip)



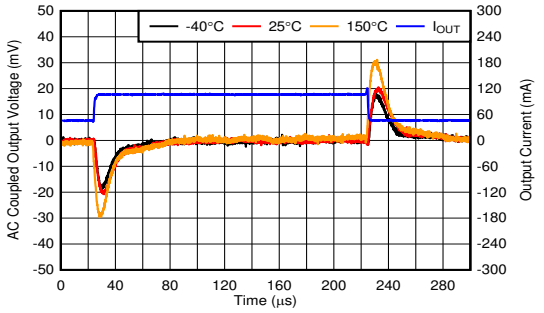
V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-40. Load Transient, No Load to 100mA (New Chip)



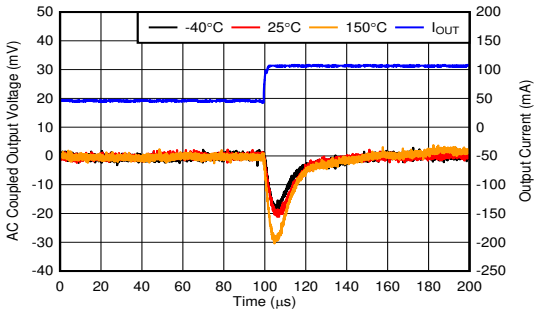
V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-41. Load Transient, No Load to 100mA Rising Edge (New Chip)



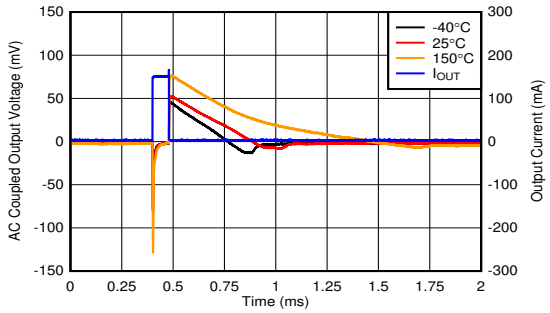
V_{OUT} = 5V, I_{OUT} = 45mA to 105mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-42. Load Transient, 45mA to 105mA (New Chip)



V_{OUT} = 5V, I_{OUT} = 45mA to 105mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-43. Load Transient, 45mA to 105mA Rising Edge (New Chip)



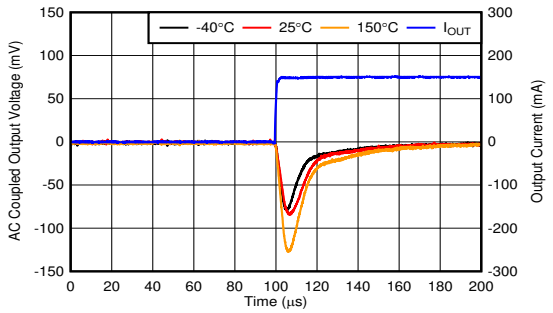
V_{OUT} = 5V, I_{OUT} = 0mA to 150mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-44. Load Transient, No Load to 150mA (New Chip)

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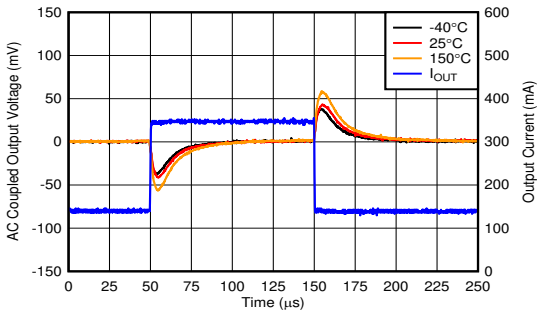
5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



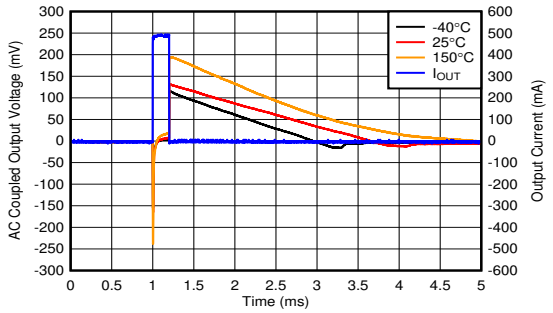
V_{OUT} = 5V, I_{OUT} = 0mA to 150mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-45. Load Transient, No Load to 150mA Rising Edge (New Chip)



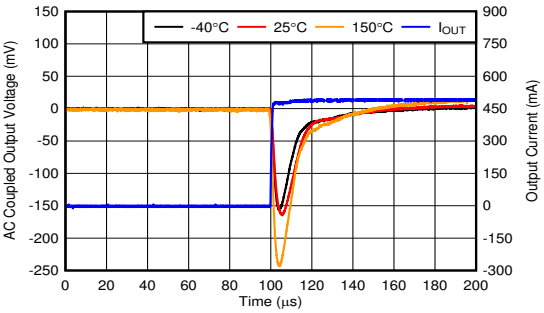
V_{OUT} = 5V, I_{OUT} = 150mA to 350mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-46. Load Transient, 150mA to 350mA (New Chip)



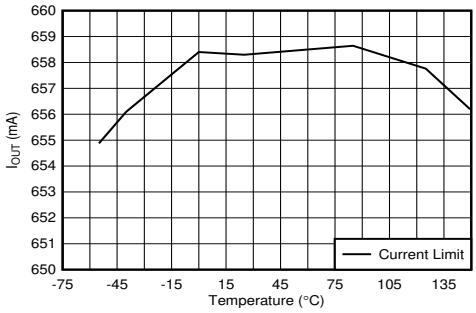
V_{OUT} = 5V, I_{OUT} = 0mA to 500mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-47. Load Transient, No Load to 500mA (New Chip)



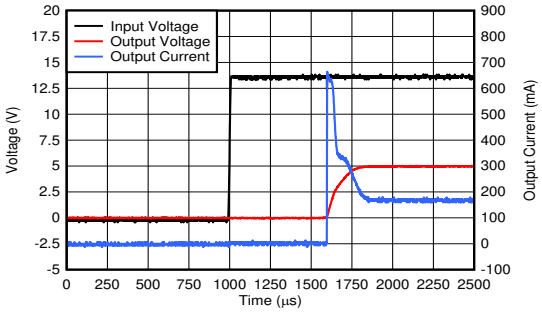
V_{OUT} = 5V, I_{OUT} = 0mA to 500mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-48. Load Transient, No Load to 500mA Rising Edge (New Chip)



V_{IN} = V_{OUT} + 1V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 5-49. Output Current Limit vs Temperature (New Chip)



V_{IN} = 13.5V, V_{OUT} = 5V, I_{OUT} = 150mA, C_{OUT} = 10µF

Figure 5-50. Start-Up Plot Inrush Current

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5.7 Typical Characteristics (continued)

legacy chip: at T_A = 25°C; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)

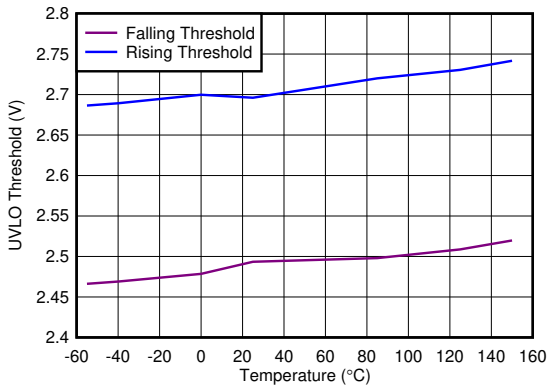


Figure 5-51. Undervoltage Lockout (UVLO) Threshold vs Temperature (New Chip)

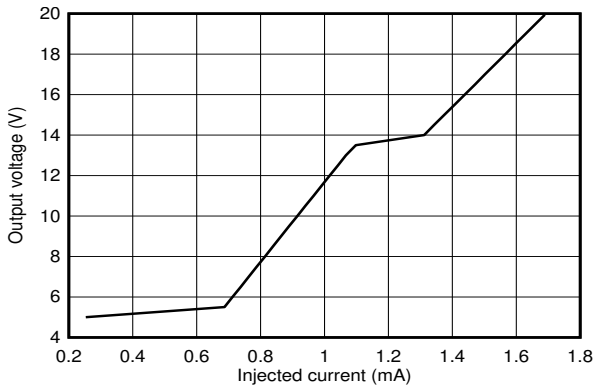


Figure 5-52. Output Voltage vs Injected Current (New Chip)

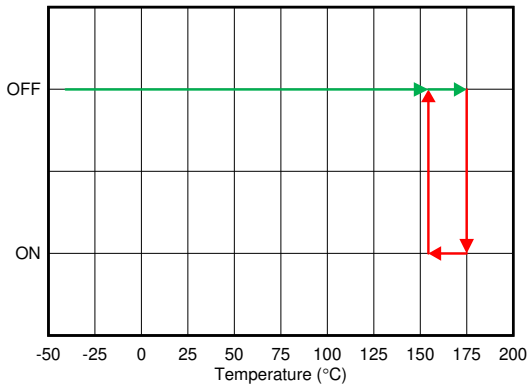


Figure 5-53. Thermal Shutdown (New Chip)

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6 Parameter Measurement Information

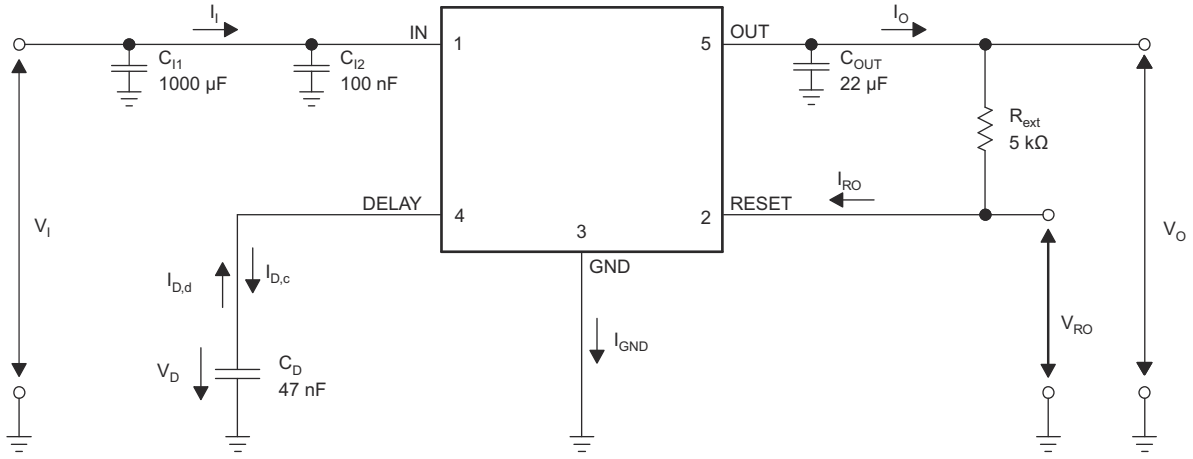


Figure 6-1. Test Circuit (Legacy Chip)

7 Detailed Description

7.1 Overview

The TLE4275-Q1 is a low-dropout linear regulator (LDO) with improved transient performance that allows for quick responses to changes in line or load conditions. The device (new chip) also features a novel output overshoot reduction feature that minimizes output overshoot during cold-crank conditions.

The integrated RESET (power-good) and delay features allow the system to notify down-stream components when power is good and assist in sequencing requirements. The device generates a reset (power-good) signal for an output voltage, $V_{OUT,rt}$, of 4.5V (typical) (new chip). Program the reset delay time with an external delay capacitor.

During normal operation, the device has a tight DC accuracy (new chip) of ±0.85% over line, load, and temperature. The increased accuracy allows for the powering of sensitive analog loads or sensors.

7.2 Functional Block Diagrams

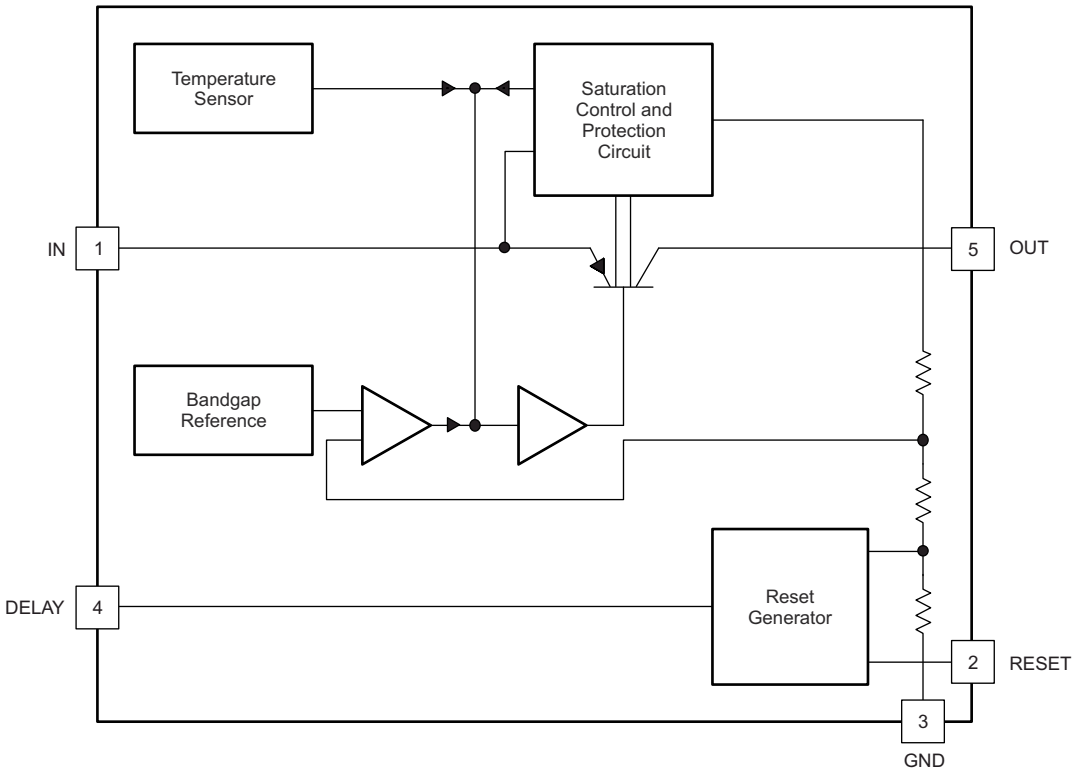


Figure 7-1. Functional Block Diagram (Legacy Chip)

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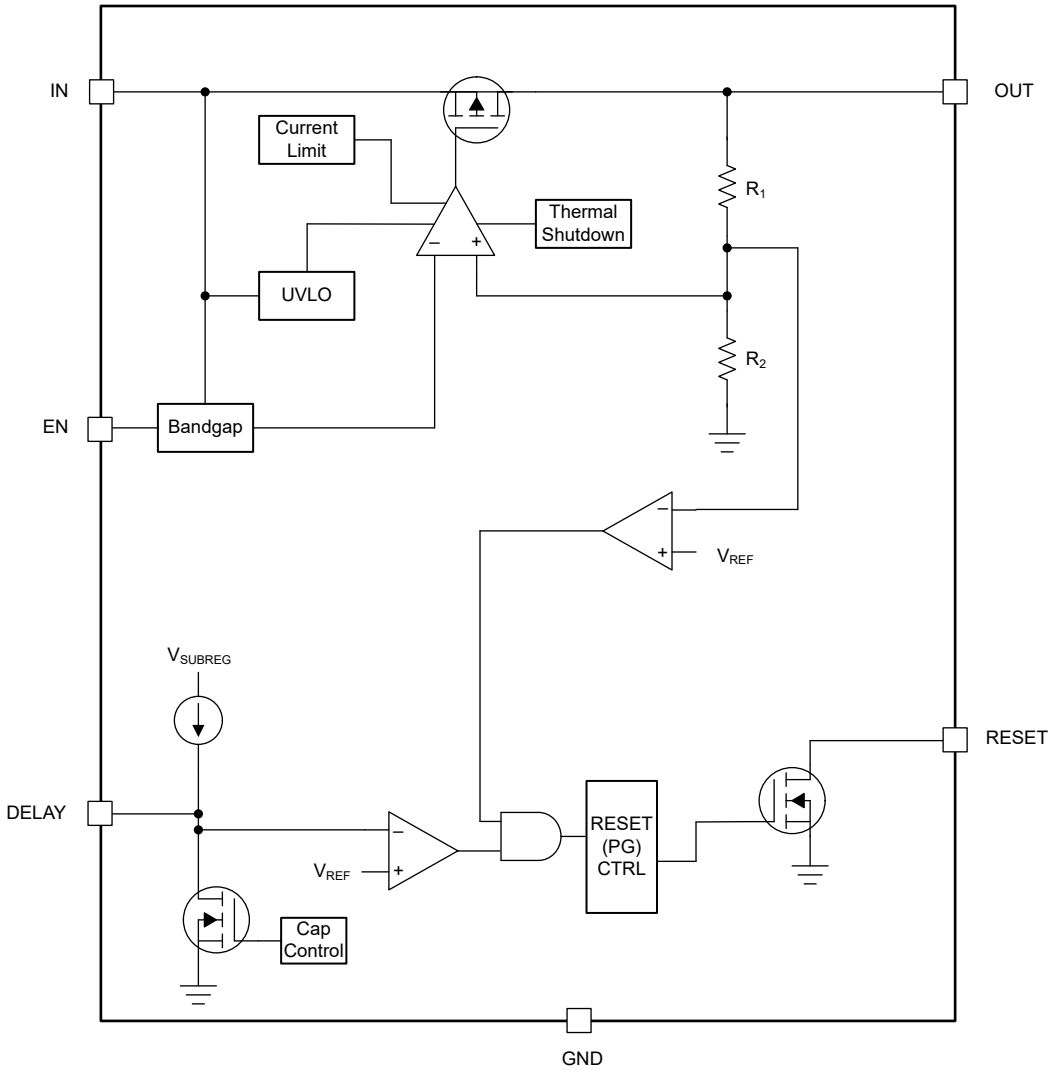


Figure 7-2. Functional Block Diagram (New Chip)

7.3 Feature Description

7.3.1 Power-Good Reset (RESET)

The power-good reset (RESET) pin is an open-drain output connected to a regulated supply through an external pullup resistor. The maximum pullup voltage is listed as V_{RESET} in the *Recommended Operating Conditions* table. For the RESET pin to have a valid output, make sure the voltage on the IN pin is greater than $V_{UVLO(RISING)}$, as listed in the *Electrical Characteristics*. When V_{OUT} exceeds $V_{RESET(TH,\ RISING)}$, the PG output is high impedance and the PG pin voltage pulls up to the connected regulated supply. When the regulated output falls below $V_{RESET(TH,\ FALLING)}$, the open-drain output turns on and pulls the RESET output low. If output voltage monitoring is not needed, leave the PG pin floating or connected to ground.

By connecting a pullup resistor to an external supply, any downstream device receives the power-good reset (RESET) as a logic signal available for sequencing. Make sure the external pullup supply voltage results in a valid logic signal for the receiving device.

7.3.2 Adjustable Power-Good RESET Delay Timer (DELAY)

The power-good reset delay period is a function of the external capacitor on the DELAY pin. The adjustable delay configures the amount of time required before the RESET pin becomes high. This delay is configured by connecting an external capacitor from this pin to GND. Figure 7-3 shows the typical timing diagram for the power-good delay pin. If the DELAY pin is left floating, the power-good delay is $t_{(DLY_FIX)}$. For more information on how to program the RESET delay, see the *Setting the Adjustable Power-Good Reset Delay* section.

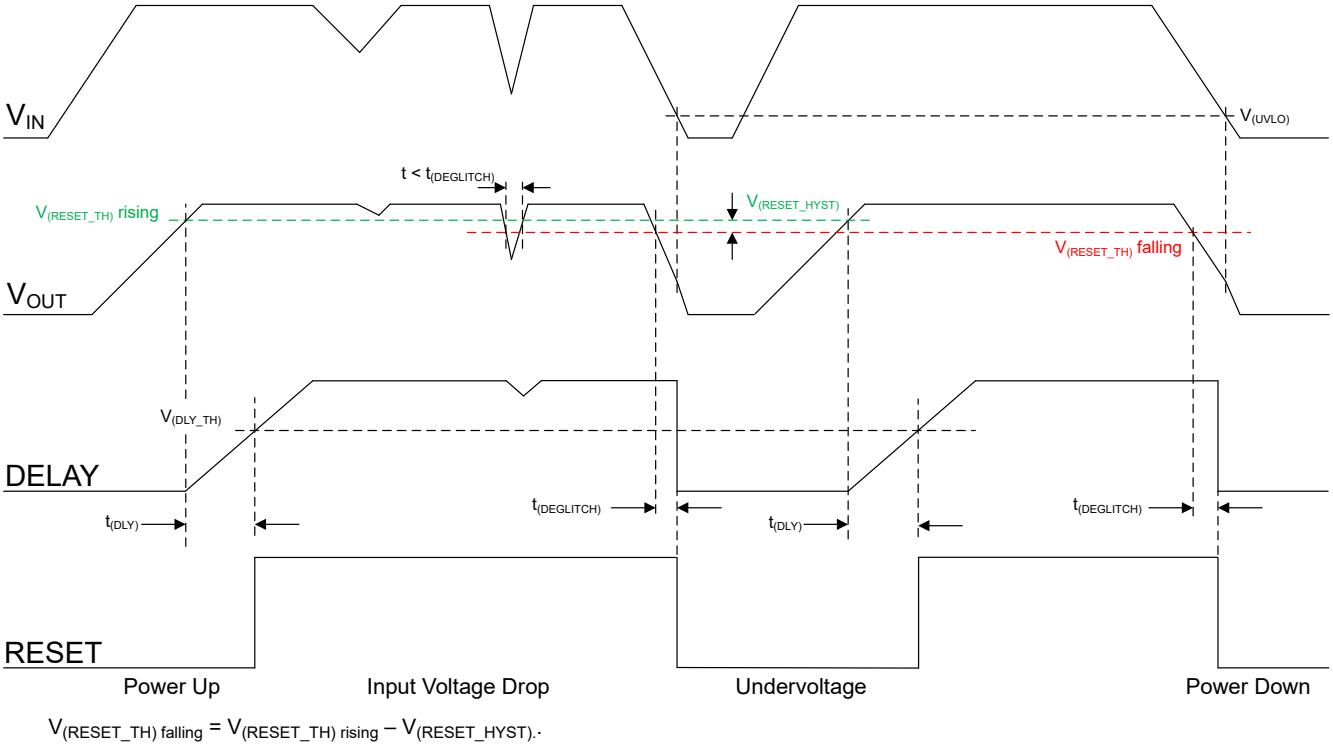


Figure 7-3. Typical Power-Good Reset Timing Diagram

7.3.2.1 Setting the Adjustable Power-Good Reset Delay

The power-good reset delay time is set in two ways: either by floating the DELAY pin or by connecting a capacitor from this pin to GND. When the DELAY pin is floating, the time defaults to $t_{(DLY_FIX)}$. The delay time is set by the following equation if a capacitor is connected between the DELAY pin and GND.

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$$t = t_{(DLY_FIX)} + C_{DELAY}\left(\frac{V_{DLY(TH)}}{I_{DLY(CHARGE)}}\right) \quad (1)$$

7.3.3 Undervoltage Lockout

The device (new chip) has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. This circuit allows a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 7-4 shows a diagram of the current limit.

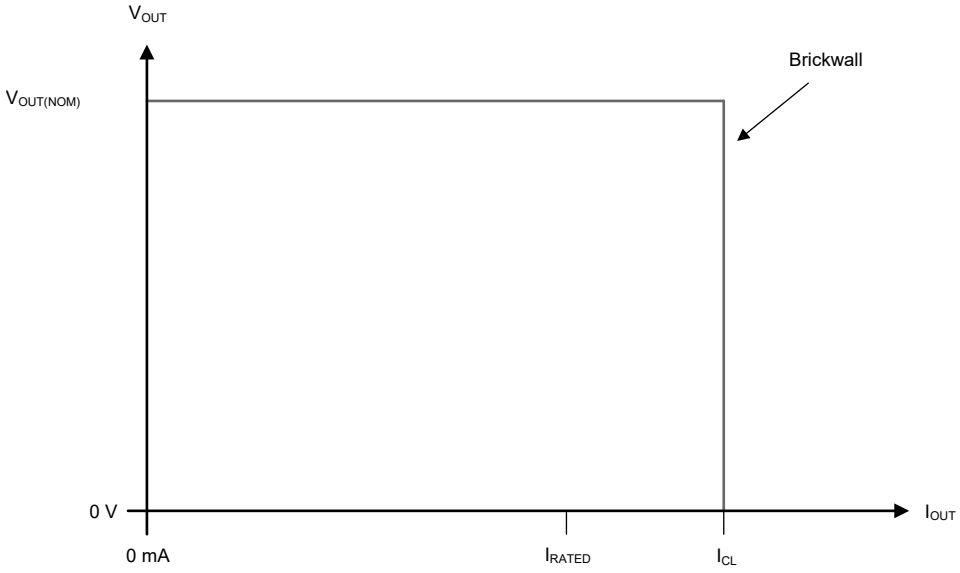


Figure 7-4. Current Limit

7.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational

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specifications. Although the device internal protection circuitry is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

Table 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. However, make sure all other conditions are met for normal operation. In this mode, the output voltage tracks the input voltage. In dropout, the device transient performance becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout potentially result in large output-voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start up. Dropout occurs when dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$, the output voltage overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During this time, the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

Shutdown the output of the device by forcing the input voltage below the UVLO falling threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

8.1.1.1 Legacy Chip Capacitor Selection

For the legacy chip, the input capacitor (C_{IN}) compensates for line fluctuation. Using a resistor of approximately 1Ω in series with C_{IN} dampens the oscillation of input inductivity and input capacitance. The output capacitor (C_{OUT}) stabilizes the regulation circuit. The output is stable at C_{OUT} ≥ 22µF and ESR ≤ 5Ω, which are within the operating temperature range.

8.1.1.2 New Chip Capacitor Selection

8.1.1.2.1 Output Capacitor

The new chip version of the TLE4275-Q1 requires an output capacitor of 2.2µF or larger (1µF or larger capacitance) for stability. An equivalent series resistance (ESR) between 0.001Ω and 2Ω is also required. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220µF.

8.1.1.2.2 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (2)$$

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8.1.3 Reverse Current

Excessive reverse current damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occurs are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

8.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct thermal plane sizing. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (3)$$

Note

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A temperature. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the ambient air temperature. The following equations shows this relationship:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance.

8.1.4.1 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (see Figure 8-1), PCB, and copper-spreading area. $R_{\theta JA}$ is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the junction-to-case (bottom) thermal resistance.

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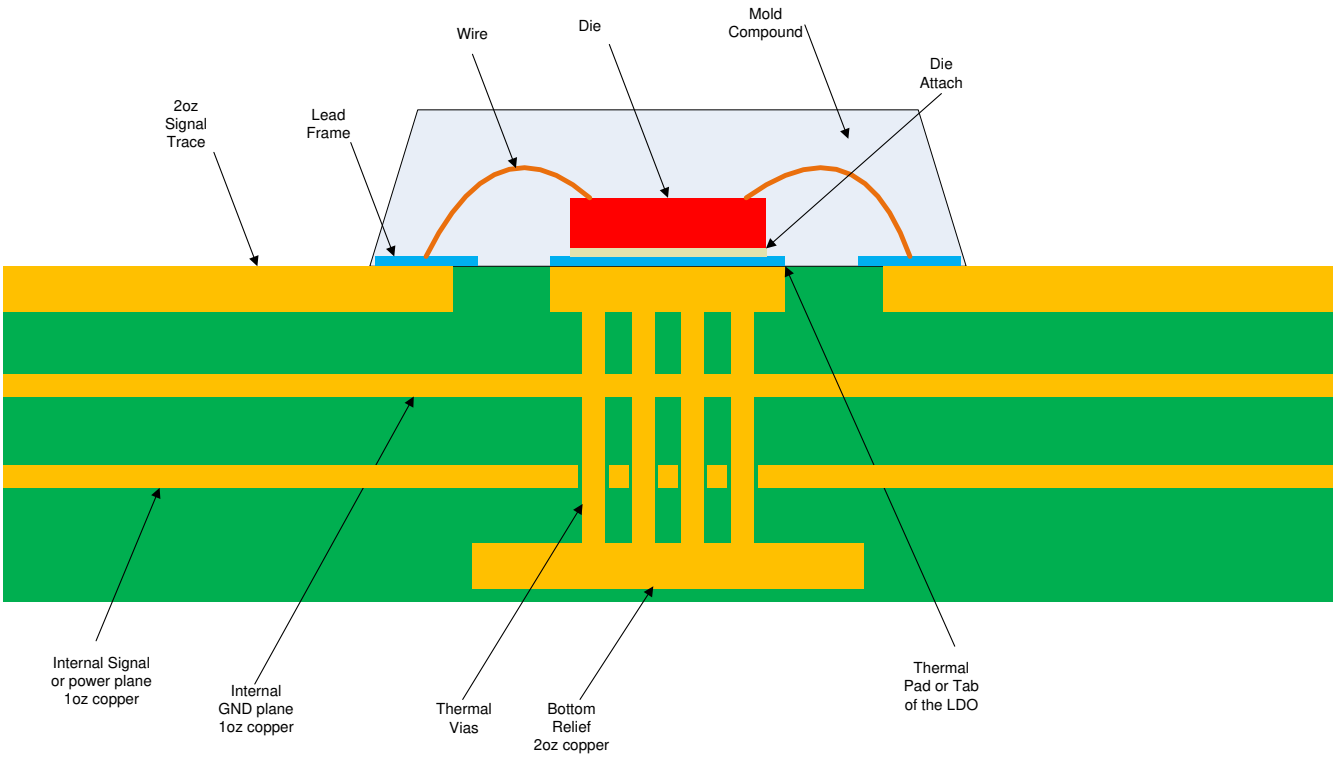


Figure 8-1. JEDEC Standard 2s2p PCB

Figure 8-2 and Figure 8-3 (for new chip) illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6mm × 101.6mm × 1.6mm PCB of two and four layers. For the 4-layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 3×4 (KVU package) array of thermal vias with a 300µm drill diameter and 25µm copper plating is located beneath the device thermal pad. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

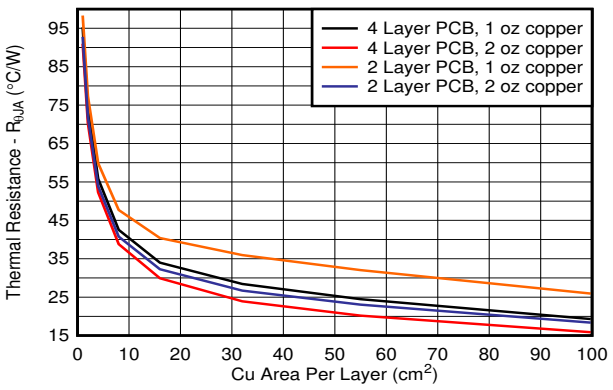


Figure 8-2. $R_{\theta JA}$ vs Copper Area (KVU Package)

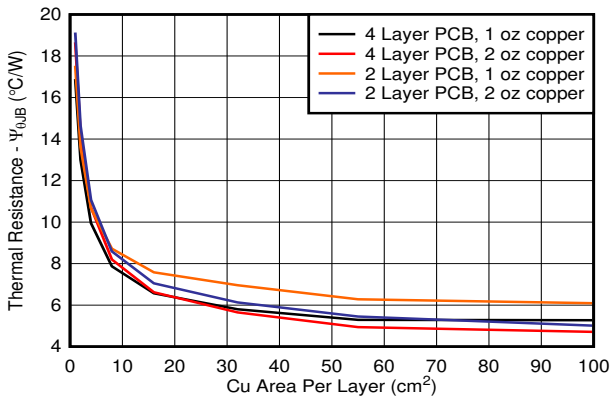


Figure 8-3. ψ_{JB} vs Copper Area (KVU Package)

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8.1.4.2 Power Dissipation Versus Ambient Temperature

Figure 8-4 is based off of a JESD51-7 4-layer, high-K board. The allowable power dissipation was estimated using the following equation. Improve thermal dissipation in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation is improved by up to 50%. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note for further information

$$T_A + R_{\theta JA} x\, P_D \leq 150\,°C \tag{5}$$

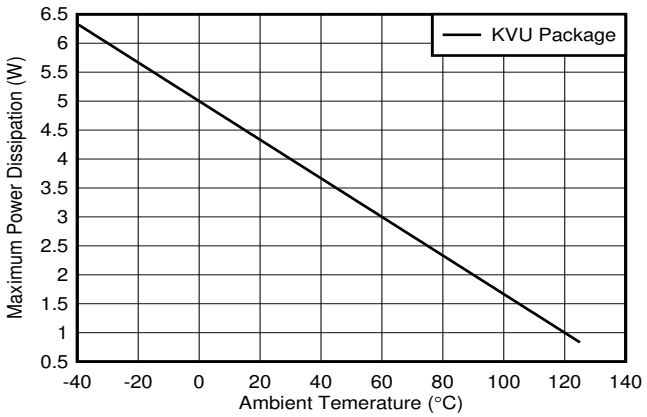


Figure 8-4. TLE4275-Q1 (KVU) Allowable Power Dissipation

8.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics. Use these metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{6}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{7}$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

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8.1.6 Setting the Adjustable Power-Good Reset Delay

The power-good reset delay time is set in two ways: either by floating the DELAY pin or by connecting a capacitor from this pin to GND. When the DELAY pin is floating, the time defaults to $t_{(DLY_FIX)}$. The delay time is set by the following equation if a capacitor is connected between the DELAY pin and GND.

$$t = t_{(DLY_FIX)} + C_{DELAY}\left(\frac{V_{DLY(TH)}}{I_{DLY(CHARGE)}}\right) \quad (8)$$

8.2 Typical Application

Figure 8-5 shows a typical application circuit for the TLE4275-Q1 (new chip). Use a low-ESR ceramic capacitor with an X5R or X7R dielectric.

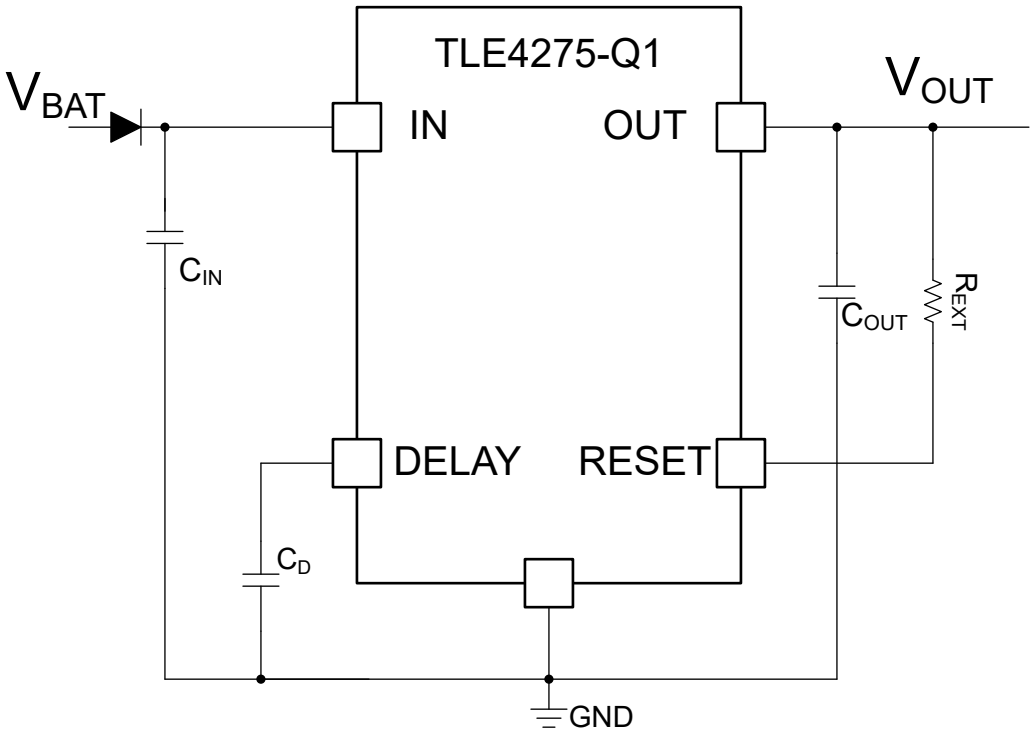


Figure 8-5. Typical Application Diagram (New Chip)

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6.0V to 40V
Output voltage	5V
Output current rating	350mA
Output capacitor range	10µF
DELAY capacitor range	100pF to 500nF

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8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Output capacitor
- Power-up reset delay time

8.2.2.1 Input Capacitor

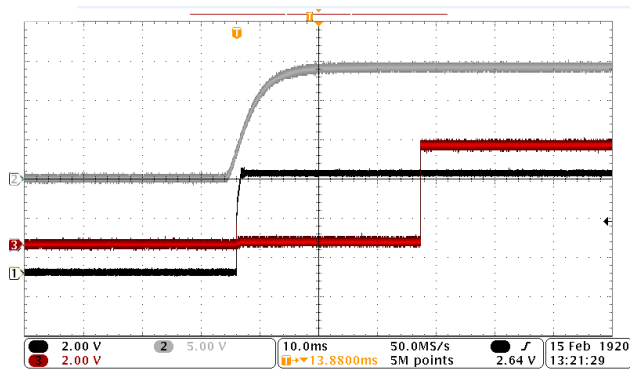
The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1µF. Make sure the voltage rating is greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. For the new chip, the capacitor value range is between 2.2µF and 200µF and the ESR range is between 1mΩ and 2Ω. For this design, a low ESR, 10µF ceramic capacitor was used to improve transient performance.

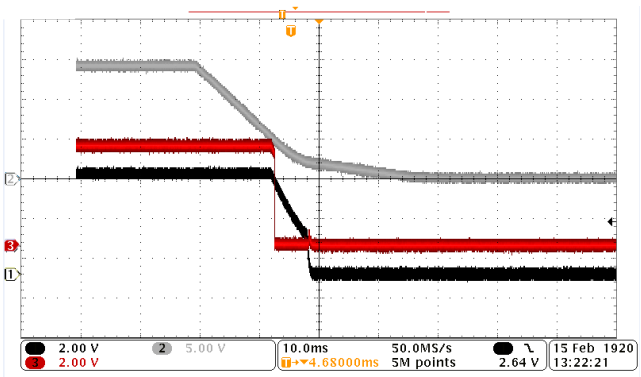
8.2.3 Application Curves

legacy chip: I_{OUT} = 200mA, C_{IN} = 22µF, and C_{OUT} = 10µF; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)



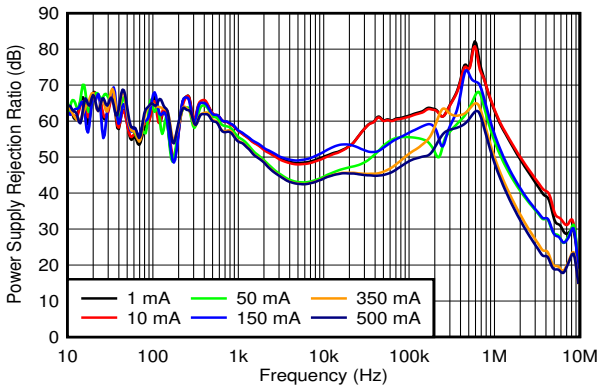
Channel 1 = V_{OUT}, channel 2 = V_{IN}, channel 3 = V_{RESET}

Figure 8-6. Power-Up Waveform (Legacy Chip)



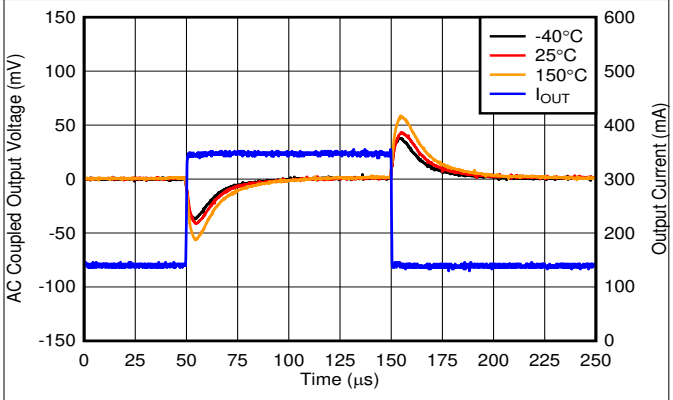
Channel 1 = V_{OUT}, channel 2 = V_{IN}, channel 3 = V_{RESET}

Figure 8-7. Power-Down Waveform (Legacy Chip)



C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 8-8. Power-Supply Ripple Rejection vs Frequency and I_{OUT} (New Chip)



V_{OUT} = 5V, I_{OUT} = 150mA to 350mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 8-9. Load Transient, 150mA to 350mA (New Chip)

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8.2.3 Application Curves (continued)

legacy chip: I_{OUT} = 200mA, C_{IN} = 22µF, and C_{OUT} = 10µF; new chip: specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted)

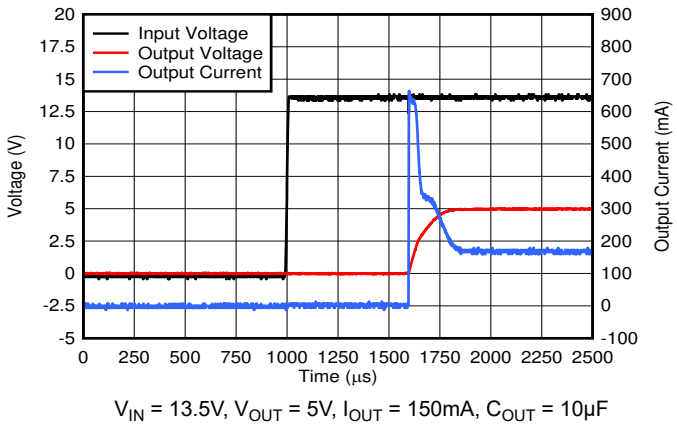


Figure 8-10. Start-Up Plot Inrush Current

8.3 Power Supply Recommendations

For the legacy chip, the device is designed to operate from an input voltage supply range between 4V and 40V. Make sure this input supply is well regulated. If the input supply is several inches from the TLE4275-Q1, add a 47µF electrolytic capacitor and a ceramic bypass capacitor at the input.

For the new chip, the device is designed to operate from an input voltage supply range between 3V and 40V. Make sure this input supply is well regulated. If the input supply is several inches from the TLE4275-Q1, add a 22µF electrolytic capacitor and a ceramic bypass capacitor at the input.

8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board. Place these components as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other. Use wide, component-side, copper surface connections for these components. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage and shields noise. This reference plane behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

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8.4.2 Layout Examples

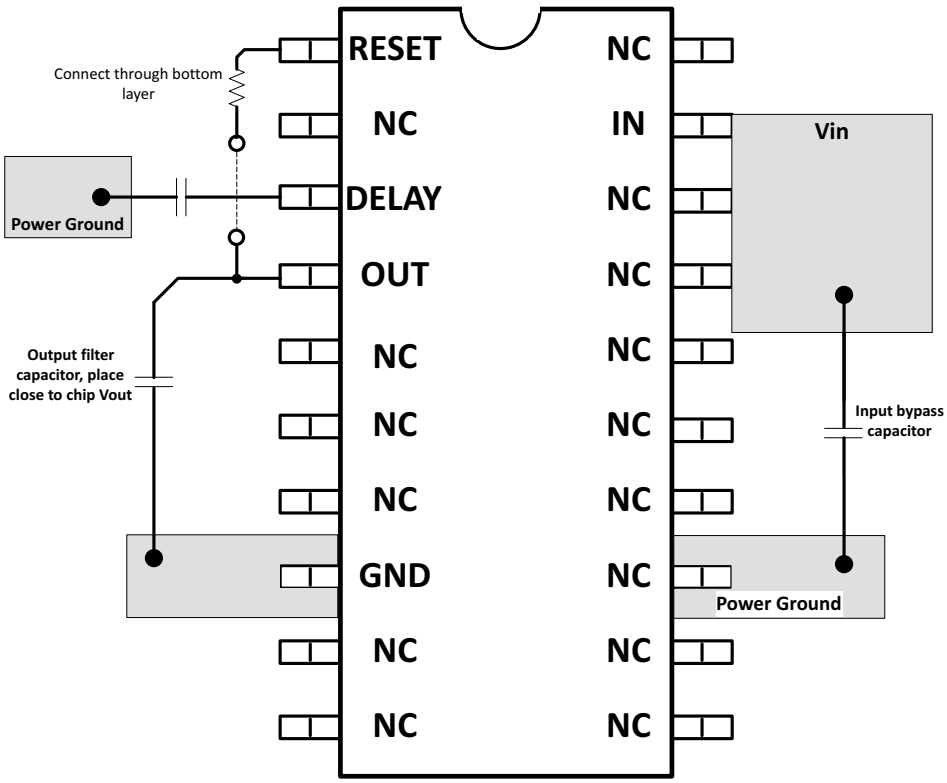


Figure 8-11. TLE4275-Q1 HTSSOP Layout Design Example

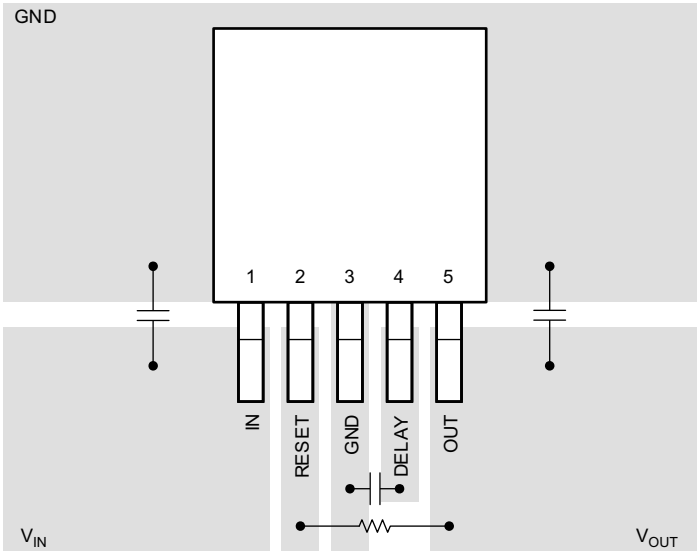


Figure 8-12. TLE4275-Q1 TO-263 Layout Design Example

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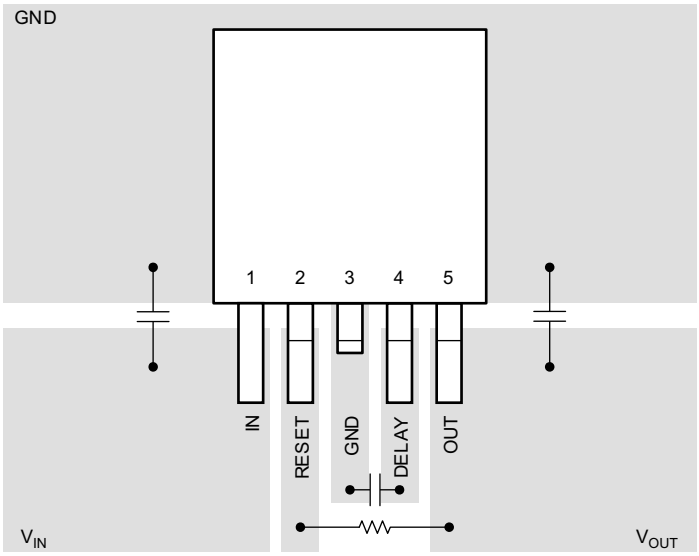


Figure 8-13. TLE4275-Q1 TO-252 Layout Design Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TLE4275Q**yyy**RQ1	**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **R** is the reel designator size.**Q1** indicates that this device is an automotive grade (AEC-Q100) device. The device ships with either legacy or new silicon. The silicon is identified by the fab source on the packaging label. (CSO: RFB = new chip; CSO: SFAB = legacy chip). Performance associated with the new and legacy chip is distinguished as such throughout the data sheet.

(1) For the most current package and ordering information see the *Package Option Addendum* at the end of this document, or visit the device product folder on www.ti.com.

9.1.2 Development Support

For the PSpice model, see the TPS7B86-Q1 PSpice Transient Model.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TLE4275-Q1 Low Temperature Stability* application note (legacy chip)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (November 2014) to Revision J (May 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added new chip devices to document	1
• Changed *Features*, *Applications*, and *Description* sections	1
• Changed *Pin Functions* table	4
• Changed the X-axis title of the *ESR Stability vs Load Current* graph	10
• Changed *ESR Stability vs Load Current* characteristic curve	10
• Added *Device Nomenclature* section	34

Changes from Revision H (March 2013) to Revision I (November 2014)	Page
• Added *Applications, Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE4275QKTTRM3Q1	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TLE4275Q
TLE4275QKTTRQ1	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TLE4275Q
TLE4275QKTTRQ1.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TLE4275Q
TLE4275QKVURM3Q1	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLE4275Q
TLE4275QKVURQ1	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLE4275Q
TLE4275QKVURQ1.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	TLE4275Q
TLE4275QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLE4275Q
TLE4275QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLE4275Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

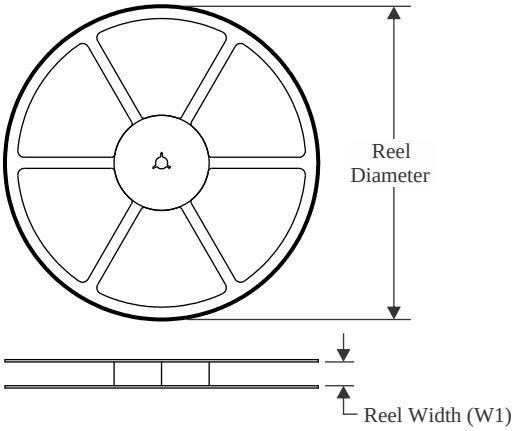
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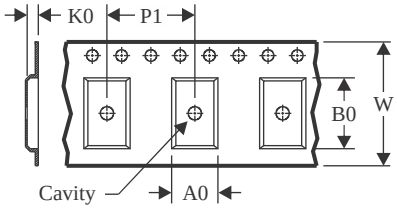
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

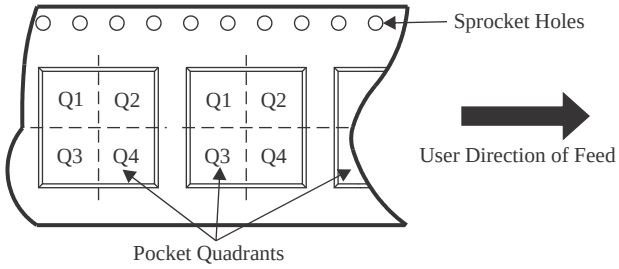


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

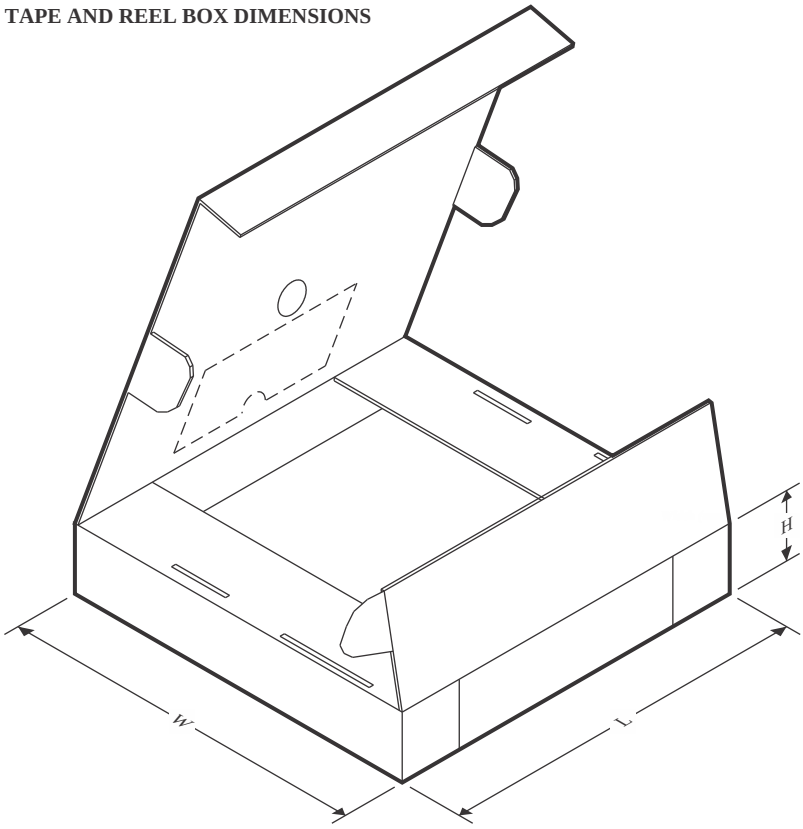
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE4275QKTTRM3Q1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TLE4275QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TLE4275QKVURM3Q1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLE4275QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLE4275QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE4275QKTTRM3Q1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TLE4275QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TLE4275QKVURM3Q1	TO-252	KVU	5	2500	340.0	340.0	38.0
TLE4275QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TLE4275QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

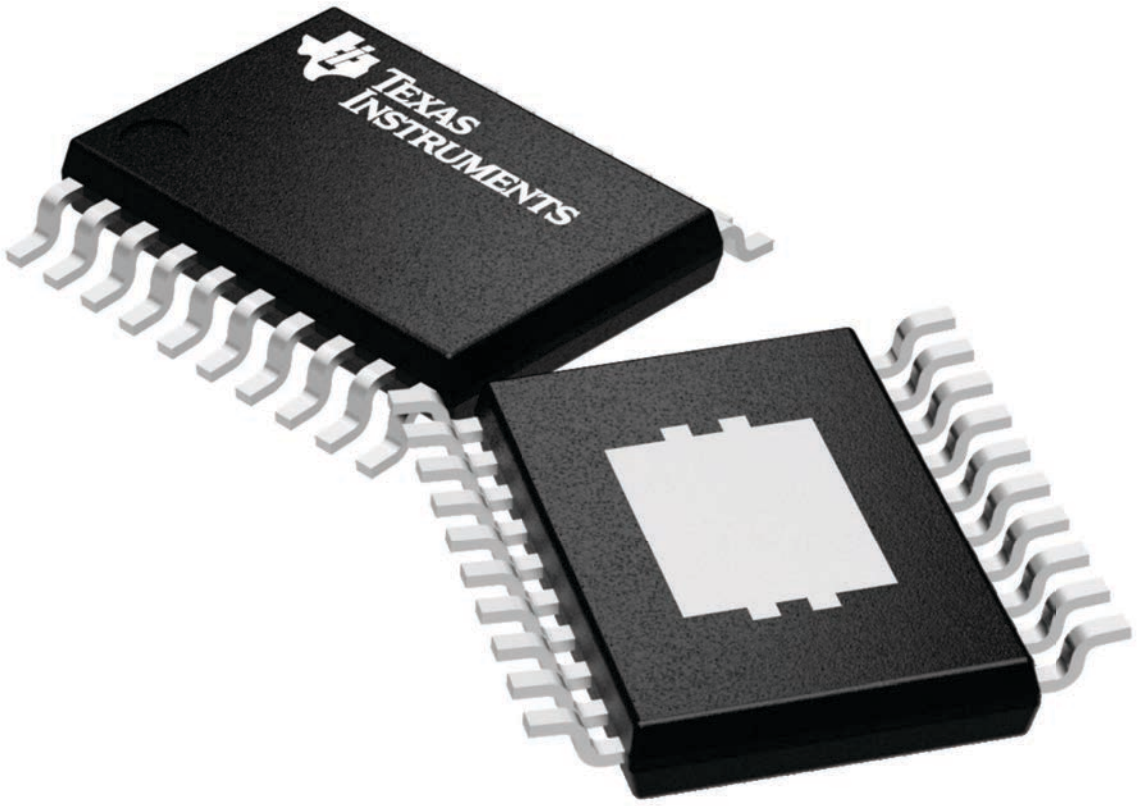
PWP 20

HTSSOP - 1.2 mm max height

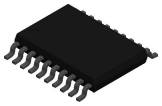
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

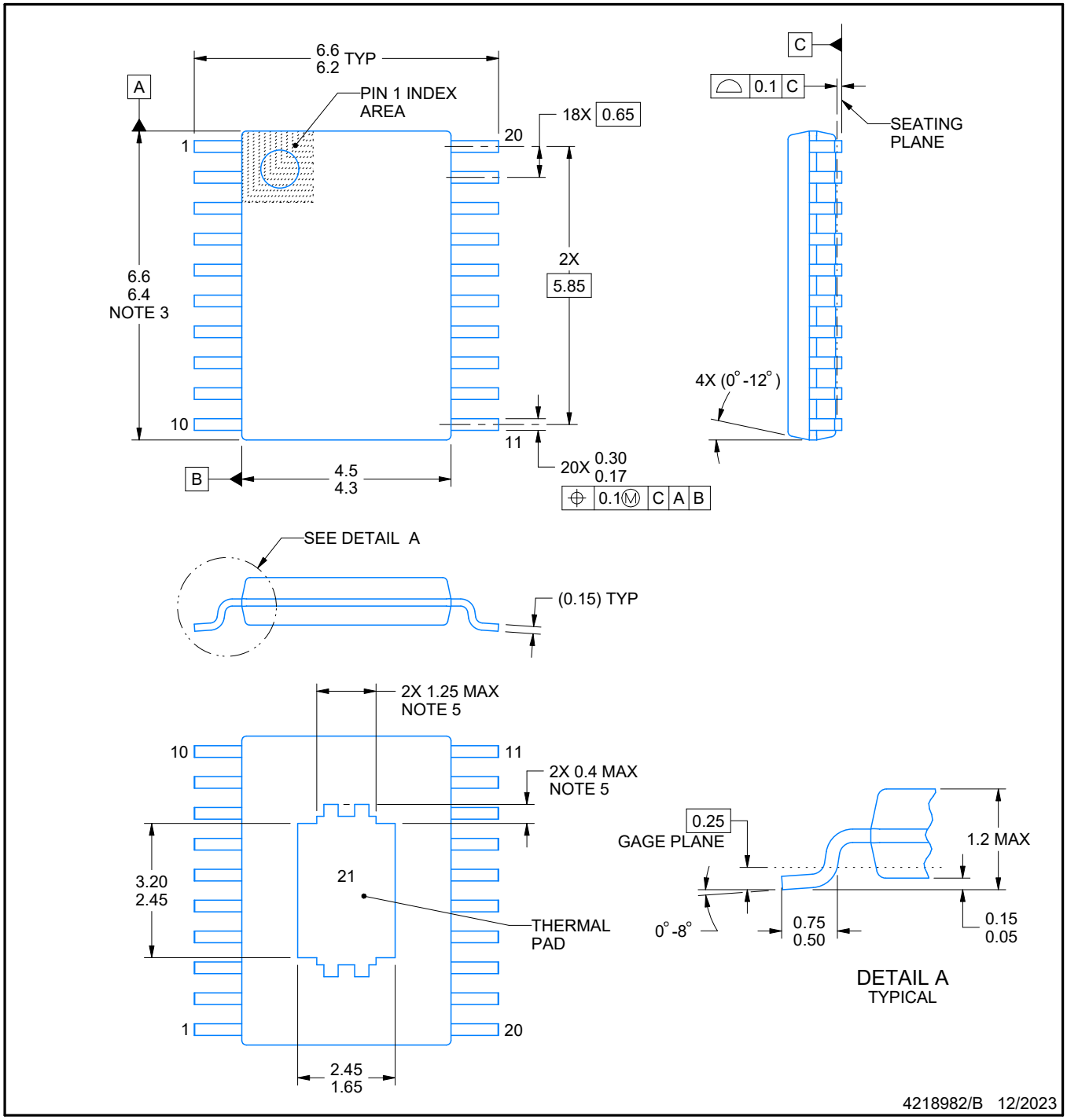


PACKAGE OUTLINE

PWP0020N

PowerPAD™ TSSOP - 1.2 mm max height

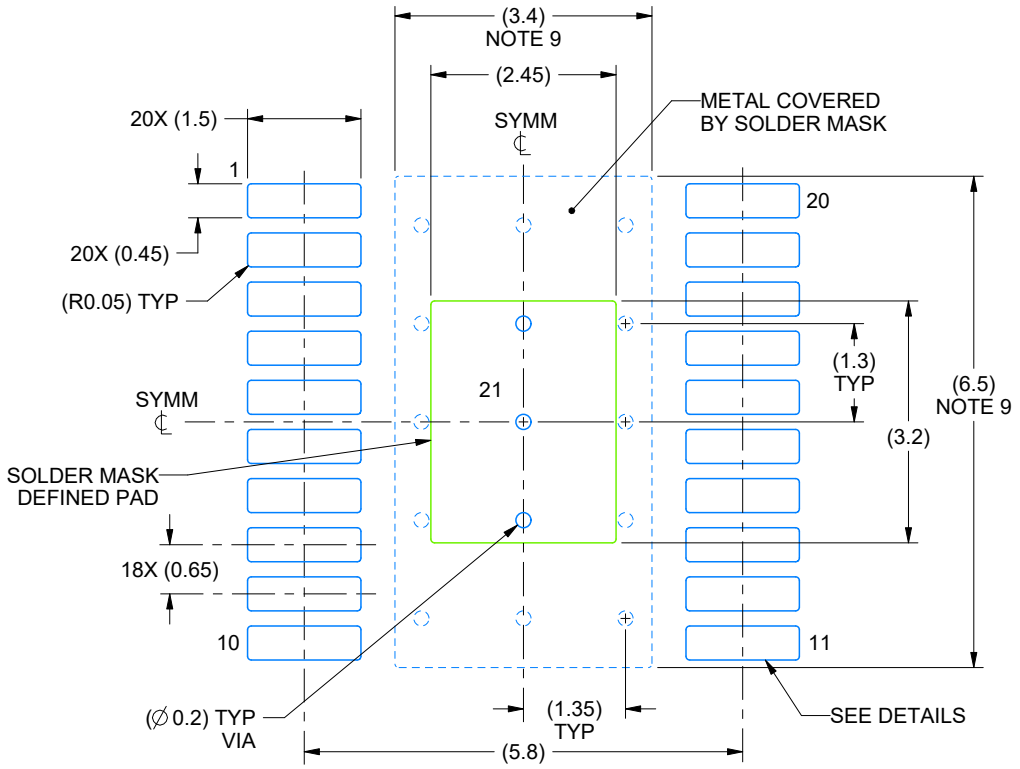
SMALL OUTLINE PACKAGE



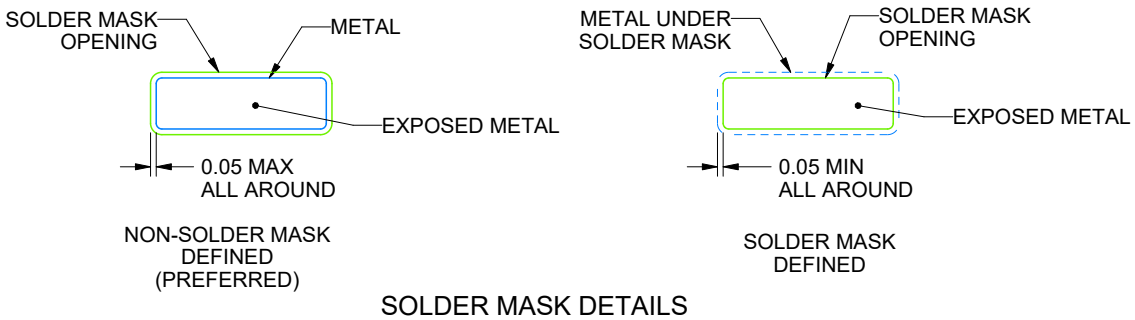
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

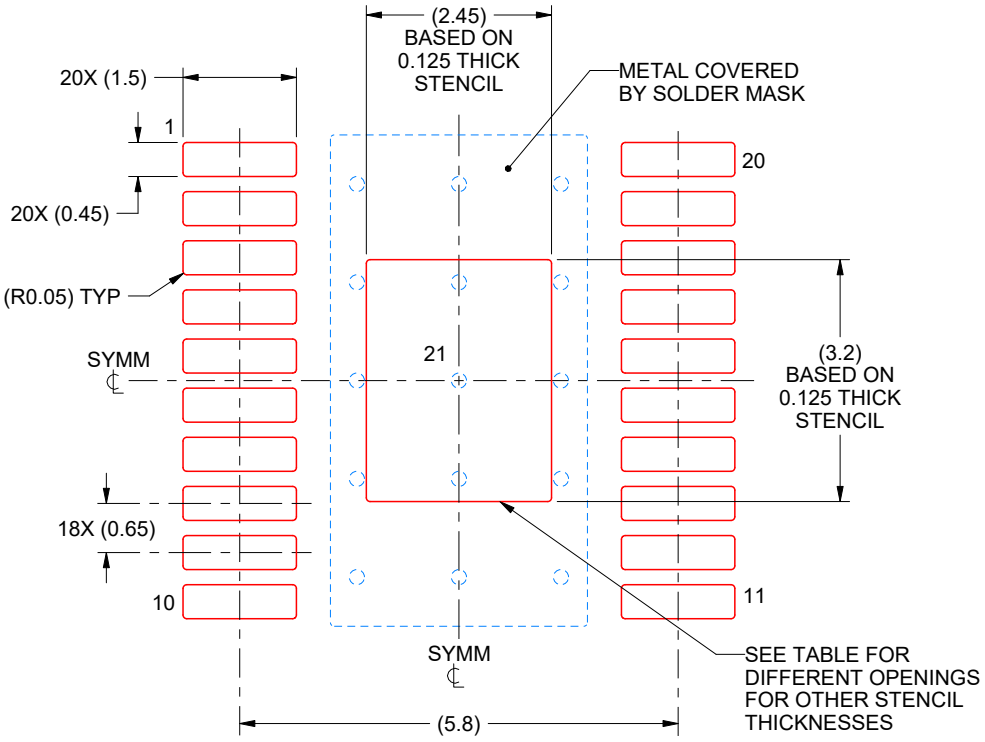


SOLDER MASK DETAILS

4218982/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

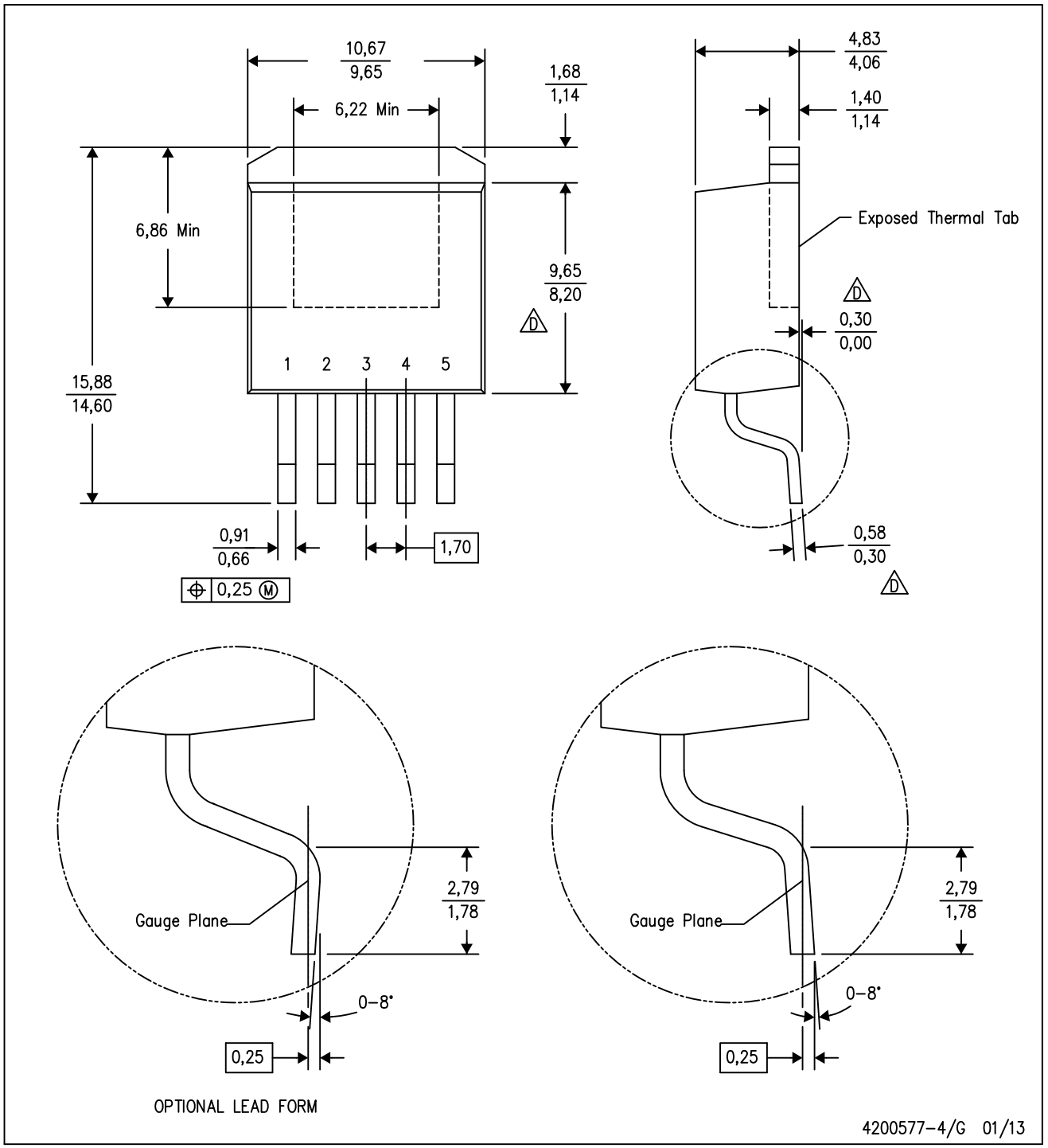
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.74 X 3.58
0.125	2.5 X 3.2 (SHOWN)
0.15	2.24 X 2.92
0.175	2.07 X 2.70

4218982/B 12/2023

NOTES: (continued)

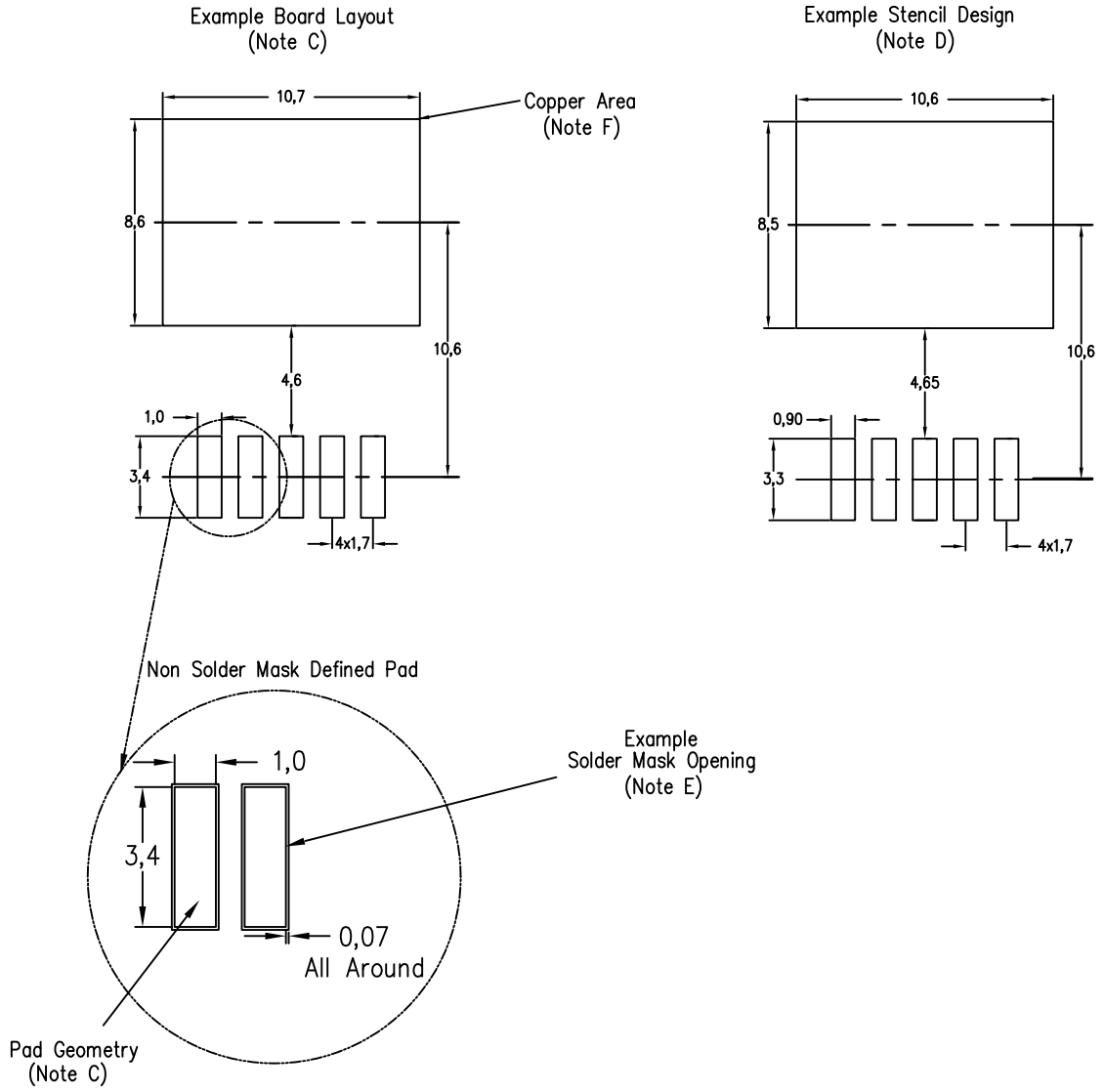
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



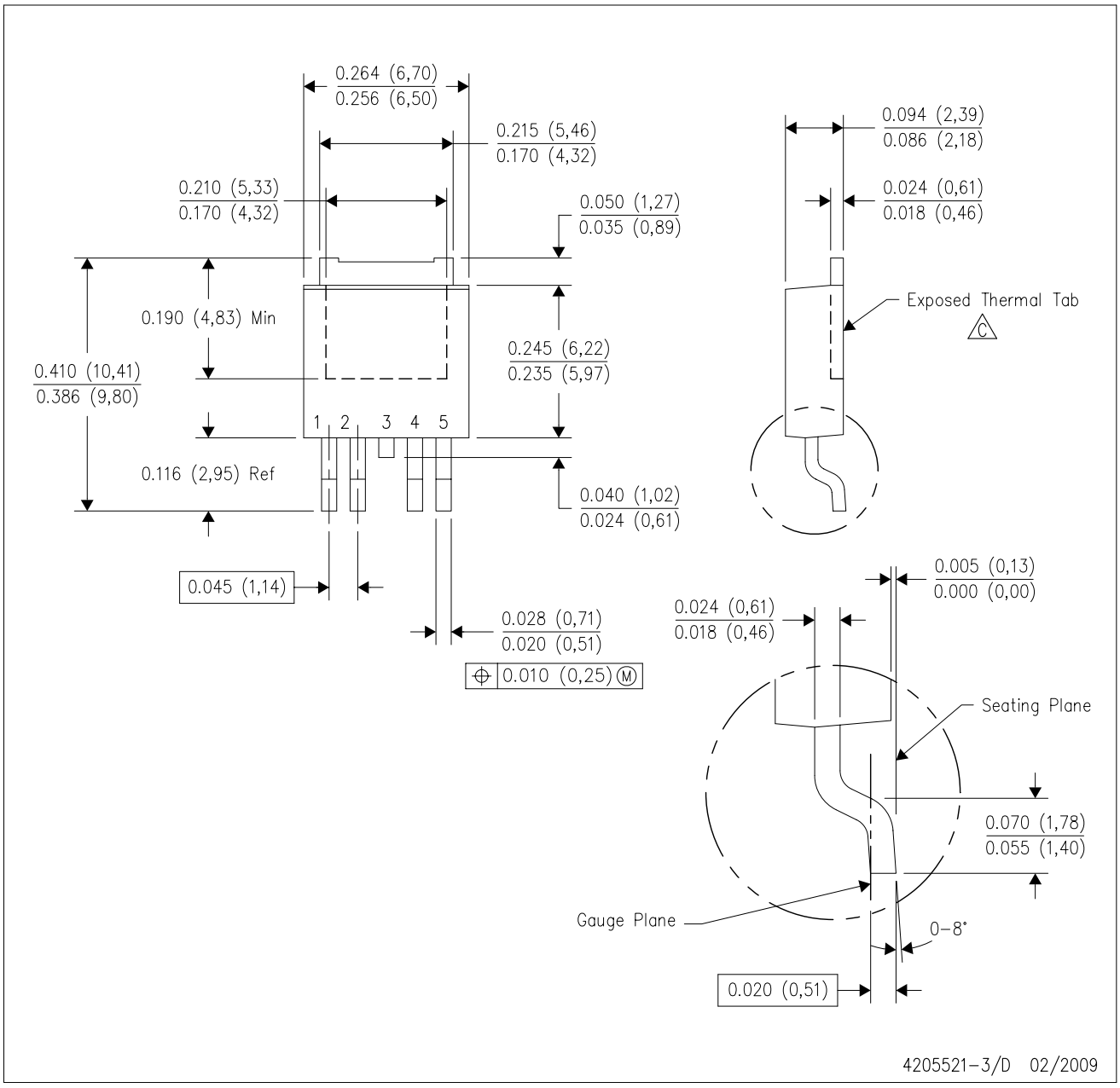
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

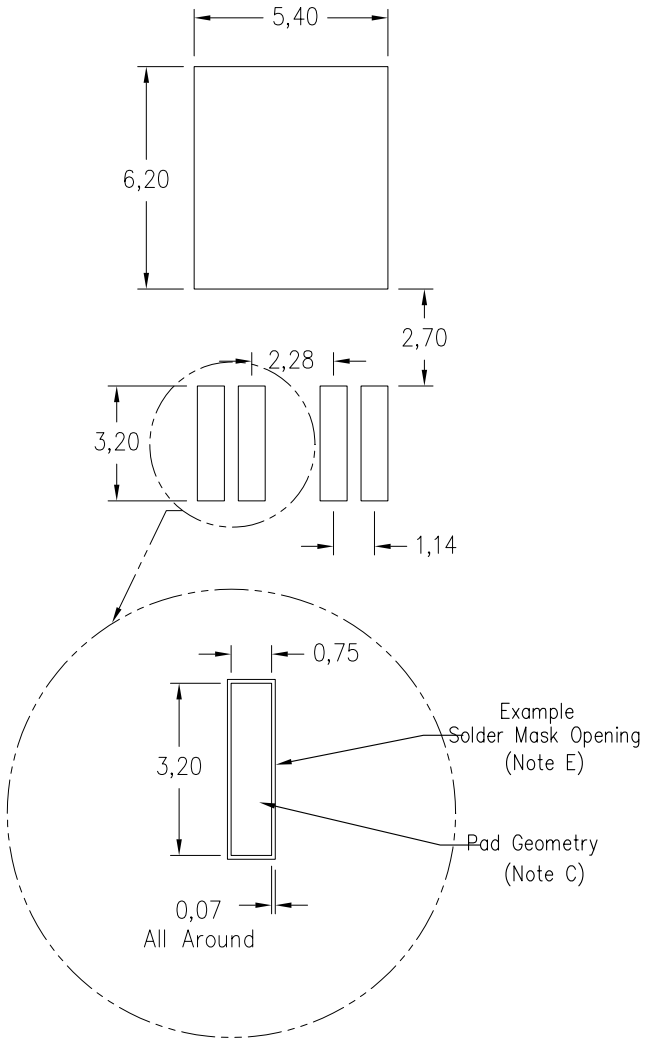
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



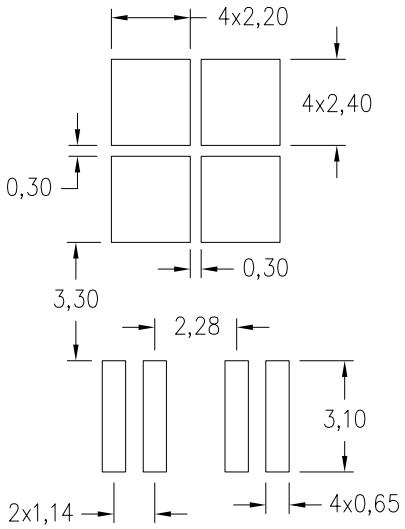
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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