Dual-Output Low Dropout Voltage Regulators with Power-Up Sequencing for Split-Voltage DSP Systems

Check for Samples: TPS70145, TPS70148, TPS70151, TPS70158, TPS70102

FEATURES

- Dual Output Voltages for Split-Supply Applications
- Selectable Power-Up Sequencing for DSP Applications
- Output Current Range of 500mA on Regulator 1 and 250mA on Regulator 2
- Fast Transient Response
- Voltage Options: 3.3V/2.5V, 3.3V/1.8V, 3.3V/1.5V, 3.3V/1.2V, and Dual Adjustable Outputs
- Open Drain Power-On Reset with 120ms Delay
- Open Drain Power Good for Regulator 1
- Ultra Low 190μA (typ) Quiescent Current
- 1μA Input Current During Standby
- Low Noise: 65μV_{RMS} Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- Two Manual Reset Inputs
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 20-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection

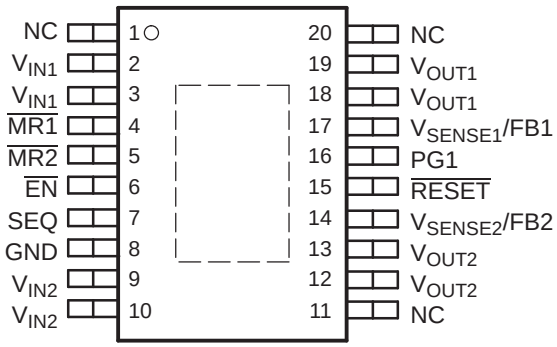
DESCRIPTION

TPS701xx family devices are designed to provide a complete power management solution for the TMS320™ DSP family, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes the TPS701xx family ideal for any TMS320 DSP applications with power sequencing requirements. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit, manual reset inputs, and an enable function, provide a complete system solution.

The TPS701xx family of voltage regulators offer very low dropout voltage and dual outputs with power-up sequence control, which is designed primarily for DSP applications. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 10μF low ESR capacitors.

These devices have fixed 3.3V/2.5V, 3.3V/1.8V, 3.3V/1.5V, 3.3V/1.2V, and adjustable/adjustable voltage options. Regulator 1 can support up to 500mA, and regulator 2 can support up to 250mA. Separate voltage inputs allow the designer to configure the source power.

PWP PACKAGE
(TOP VIEW)

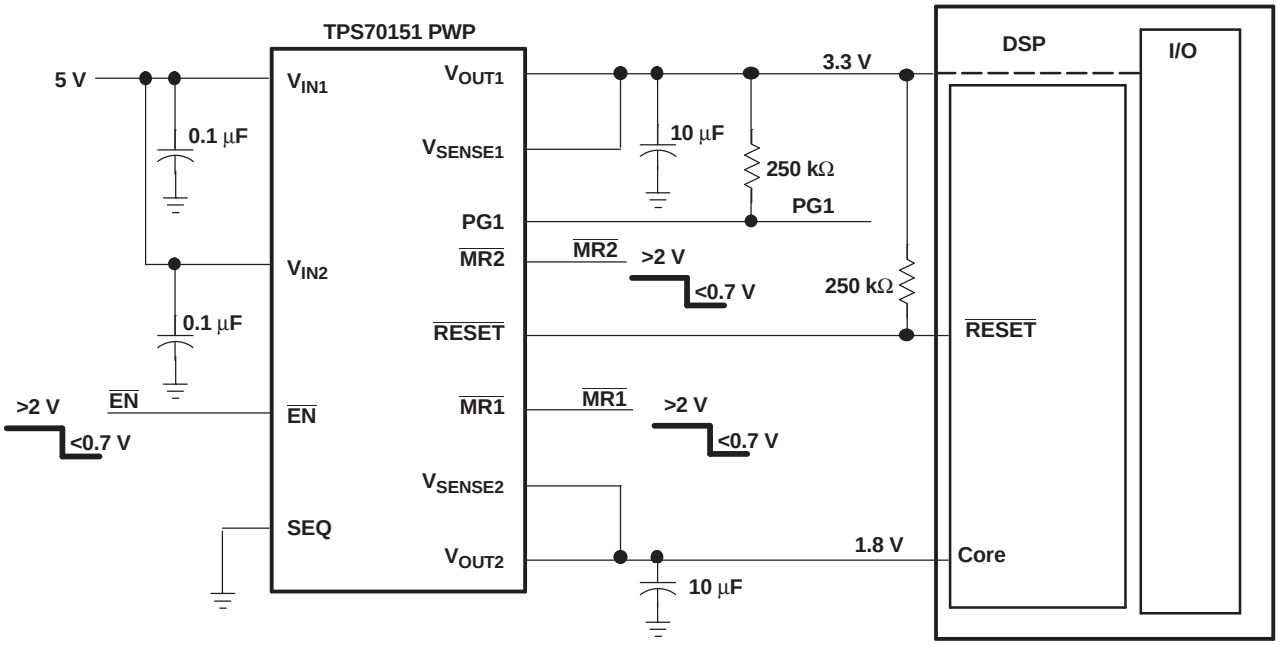


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Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 170mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 230µA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to $\overline{EN}$ (enable) shuts down both regulators, reducing the input current to 1µA at T_J = +25°C.

The device is enabled when the $\overline{EN}$ pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the V_{SENSE1} and V_{SENSE2} pins, respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (for example, an overload condition), V_{OUT1} is turned off. Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. The SEQ pin is connected to an internal pull-up current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage conditions at V_{OUT1}, which can be used to implement an SVS for the circuitry supplied by regulator 1.

The TPS701xx features a $\overline{RESET}$ (SVS, POR, or Power-On Reset). $\overline{RESET}$ output initiates a reset in DSP systems and related digital applications in the event of an undervoltage condition. $\overline{RESET}$ indicates the status of V_{OUT2} and both manual reset pins ($\overline{MR1}$ and $\overline{MR2}$). When V_{OUT2} reaches 95% of its regulated voltage and $\overline{MR1}$ and $\overline{MR2}$ are in the logic high state, $\overline{RESET}$ goes to a high impedance state after a 120ms delay. $\overline{RESET}$ goes to the logic low state when the V_{OUT2} regulated output voltage is pulled below 95% (for example, an overload condition) of its regulated voltage. To monitor V_{OUT1}, the PG1 output pin can be connected to $\overline{MR1}$ or $\overline{MR2}$.

The device has an undervoltage lockout (UVLO) circuit that prevents the internal regulators from turning on until V_{IN1} reaches 2.5V.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	VOLTAGE (V)(2) V_{OUT1}	VOLTAGE (V)(2) V_{OUT2}	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE (T_J)	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS70102	Adjustable	Adjustable	HTSSOP-20 (PWP)	-40°C to +125°C	TPS70102PWP	Tube, 70
					TPS70102PWPR	Tape and Reel, 2000
TPS70145	3.3 V	1.2 V	HTSSOP-20 (PWP)	-40°C to +125°C	TPS70145PWP	Tube, 70
					TPS70145PWPR	Tape and Reel, 2000
TPS70148	3.3 V	1.5 V	HTSSOP-20 (PWP)	-40°C to +125°C	TPS70148PWP	Tube, 70
					TPS70148PWPR	Tape and Reel, 2000
TPS70151	3.3 V	1.8 V	HTSSOP-20 (PWP)	-40°C to +125°C	TPS70151PWP	Tube, 70
					TPS70151PWPR	Tape and Reel, 2000
TPS70158	3.3 V	2.5 V	HTSSOP-20 (PWP)	-40°C to +125°C	TPS70158PWP	Tube, 70
					TPS70158PWPR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.
(2) For fixed 1.20V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	TPS701xx	UNIT
Input voltage range: V_{IN1}, V_{IN2} (2)	–0.3 to +7	V
Voltage range at $\overline{EN}$	–0.3 to +7	V
Output voltage range (V_{OUT1}, V_{SENSE1})	5.5	V
Output voltage range (V_{OUT2}, V_{SENSE2})	5.5	V
Maximum $\overline{RESET}$, PG1 voltage	7	V
Maximum $\overline{MR1}$, $\overline{MR2}$, and SEQ voltage	V_{IN1}	V
Peak output current	Internally limited	—
Continuous total power dissipation	See Thermal Information Table	—
Junction temperature range, T_J	–40 to +150	°C
Storage temperature range, T_{stg}	–65 to +150	°C
ESD rating, HBM	2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are tied to network ground.

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THERMAL INFORMATION

THERMAL METRIC(1) (2)		TPS701xx PWP (20 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	74.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	43.1	
θ_{JB}	Junction-to-board thermal resistance	19.7	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	17.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

Over operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_I (1)(regulator 1 and 2)	2.7	6	V
Output current, I_O (regulator 1)	0	500	mA
Output current, I_O (regulator 2)	0	250	mA
Output voltage range (for adjustable option)	1.22	5.5	V
Operating junction temperature, T_J	–40	+125	°C

(1) To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN1} or V_{IN2} = $V_{OUT(nom)}$ + 1V, I_O = 1mA, $\overline{EN}$ = 0V, C_O = 33μF, (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage(1), (2)	Reference voltage	2.7V < V_I < 6V, T_J = +25°C	FB connected to V_O		1.22		V
			2.7V < V_I < 6V,	FB connected to V_O	1.196		1.244	
		1.2V Output	2.7V < V_I < 6V,	T_J = +25°C		1.2		
			2.7V < V_I < 6V,		1.176		1.224	
		1.5V Output	2.7V < V_I < 6V,	T_J = +25°C		1.5		
			2.7V < V_I < 6V,		1.47		1.53	
		1.8V Output	2.7V < V_I < 6V,	T_J = +25°C		1.8		
			2.7V < V_I < 6V,		1.764		1.836	
		2.5V Output	2.7V < V_I < 6V,	T_J = +25°C		2.5		
			2.7V < V_I < 6V,		2.45		2.55	
		3.3V Output	2.7V < V_I < 6V,	T_J = +25°C		3.3		
			2.7V < V_I < 6V,		3.234		3.366	
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN}$ = 0V(1)			(2)	T_J = +25°C		190		μA
			(2)				230	
Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 (3)			V_O + 1V < V_I ≤ 6V,	T_J = +25°C(1)		0.01%		V
			V_O + 1V < V_I ≤ 6V	(1)			0.1%	
Load regulation for $V_{OUT\ 1}$ and V_{OUT2}			T_J = +25°C	(2)		1		mV

(1) Minimum input operating voltage is 2.7V or $V_{O(typ)}$ + 1V, whichever is greater. Maximum input voltage = 6V, minimum output current = 1mA.
(2) I_O = 1mA to 250mA for Regulator 1 and 1mA to 125mA for Regulator 2.
(3) If V_O < 1.8V then V_{Imax} = 6V, V_{Imin} = 2.7V: $\text{Line Reg. (mV)} = (\%/V) \times V_O \frac{(V_{Imax} - 2.7V)}{100} \times 1000$

If V_O > 2.5V then V_{Imax} = 6V, V_{Imin} = V_O + 1V: $\text{Line Reg. (mV)} = (\%/V) \times V_O \frac{(V_{Imax} - (V_O + 1V))}{100} \times 1000$

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN1} or V_{IN2} = $V_{OUT(nom)}$ + 1V, I_O = 1mA, $\overline{EN}$ = 0V, C_O = 33µF, (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_n	Output noise voltage	Regulator 1	BW 300Hz to 50kHz,	C_O = 33µF, T_J = +25°C		65		μV_{RMS}
		Regulator 2				65		
Output current limit		Regulator 1	V_{OUT} = 0V			1.6	1.9	A
		Regulator 2				0.750	1	
Thermal shutdown junction temperature						+150		°C
I_I (standby)	Standby current	Regulator 1	$\overline{EN}$ = V_I,	T_J = +25°C			1	µA
			$\overline{EN}$ = V_I				3	
		Regulator 2	$\overline{EN}$ = V_I,	T_J = +25°C			1	µA
			$\overline{EN}$ = V_I				3	
PSRR	Power-supply ripple rejection		f = 1kHz, C_O = 33µF,	T_J = +25°C(1)		60		dB
RESET Terminal								
Minimum input voltage for valid $\overline{RESET}$			I_{RESET} = 300µA,	$V_{(RESET)}$ ≤ 0.8V		1.0	1.3	V
Trip threshold voltage			V_O decreasing		92%	95%	98%	V_{OUT}
Hysteresis voltage			Measured at V_O			0.5%		V_{OUT}
$t_{\overline{(RESET)}}$			RESET pulse duration		80	120	160	ms
$t_{r\ \overline{(RESET)}}$			Rising edge deglitch			30		µs
Output low voltage			V_I = 3.5V,	$I_{O(RESET)}$ = 1mA		0.15	0.4	V
Leakage current			$V_{(RESET)}$ = 6V				1	µA
PG1 Terminal								
Minimum input voltage for valid PG1			$I_{(PG1)}$ = 300µA,	$V_{(PG1)}$ ≤ 0.8V		1.0	1.3	V
Trip threshold voltage			V_O decreasing		92%	95%	98%	V_{OUT}
Hysteresis voltage			Measured at V_O			0.5%		V_{OUT}
$t_{r(PG1)}$			Rising edge deglitch			30		µs
Output low voltage			V_I = 2.7V,	$I_{O(PG1)}$ = 1mA		0.15	0.4	V
Leakage current			$V_{(PG1)}$ = 6V				1	µA
EN Terminal								
High level $\overline{EN}$ input voltage					2			V
Low level $\overline{EN}$ input voltage							0.7	V
Input current ($\overline{EN}$)					–1		1	µA
Falling edge deglitch			Measured at V_O			140		µs
SEQ Terminal								
High level SEQ input voltage					2			V
Low level SEQ input voltage							0.7	V
SEQ pull-up current source						6		µA
$\overline{MR1}$ / $\overline{MR2}$ Terminals								
High level input voltage					2			V
Low level input voltage							0.7	V
Pull-up current source						6		µA
V_{OUT2} Terminal								
V_{OUT2} UV comparator: Positive-going input threshold voltage of V_{OUT2} UV comparator					80% V_O	83% V_O	86% V_O	V
V_{OUT2} UV comparator: Hysteresis						0.5% V_O		mV
V_{OUT2} UV comparator: Falling edge deglitch			V_{SENSE_2} decreasing below threshold			140		µs
Peak output current			2ms pulse width			375		mA

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN1} or V_{IN2} = $V_{OUT(nom)}$ + 1V, I_O = 1mA, $\overline{EN}$ = 0V, C_O = 33µF, (unless otherwise noted).

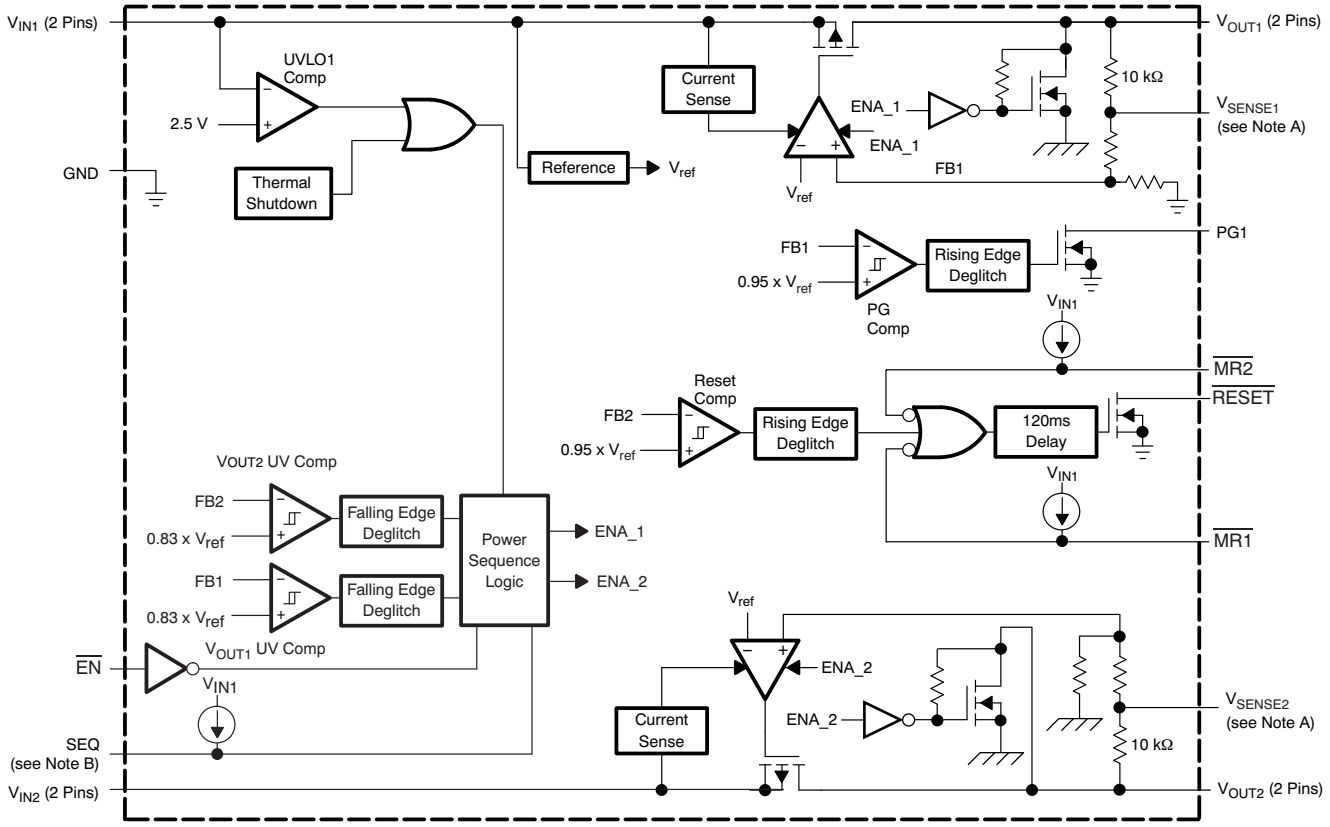
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Discharge transistor current	V_{OUT2} = 1.5V		7.5		mA
V_{OUT1} Terminal					
V_{OUT1} UV comparator: Positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
V_{OUT1} UV comparator: Hysteresis			0.5% V_O		mV
V_{OUT1} UV comparator: Falling edge deglitch	V_{SENSE_1} decreasing below threshold		140		µs
V_{OUT1} Terminal, *continued*					
Dropout voltage(4)	I_O = 500mA, T_J = +25°C V_{IN1} = 3.2V		170		mV
Dropout voltage(4)	I_O = 500mA, V_{IN1} = 3.2V			275	mV
Peak output current(4)	2ms pulse width		750		mA
Discharge transistor current	V_{OUT1} = 1.5V		7.5		mA
V_{IN1} UVLO threshold		2.4		2.65	V
FB Terminal					
Input current: TPS70102	FB = 1.8V		1		µA

(4) Input voltage (V_{IN1} or V_{IN2}) = $V_{O(typ)}$ – 100mV. For 1.5V, 1.8V and 2.5V regulators, the dropout voltage is limited by input voltage range. The 3.3V regulator input is set to 3.2V to perform this test.

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DEVICE INFORMATION

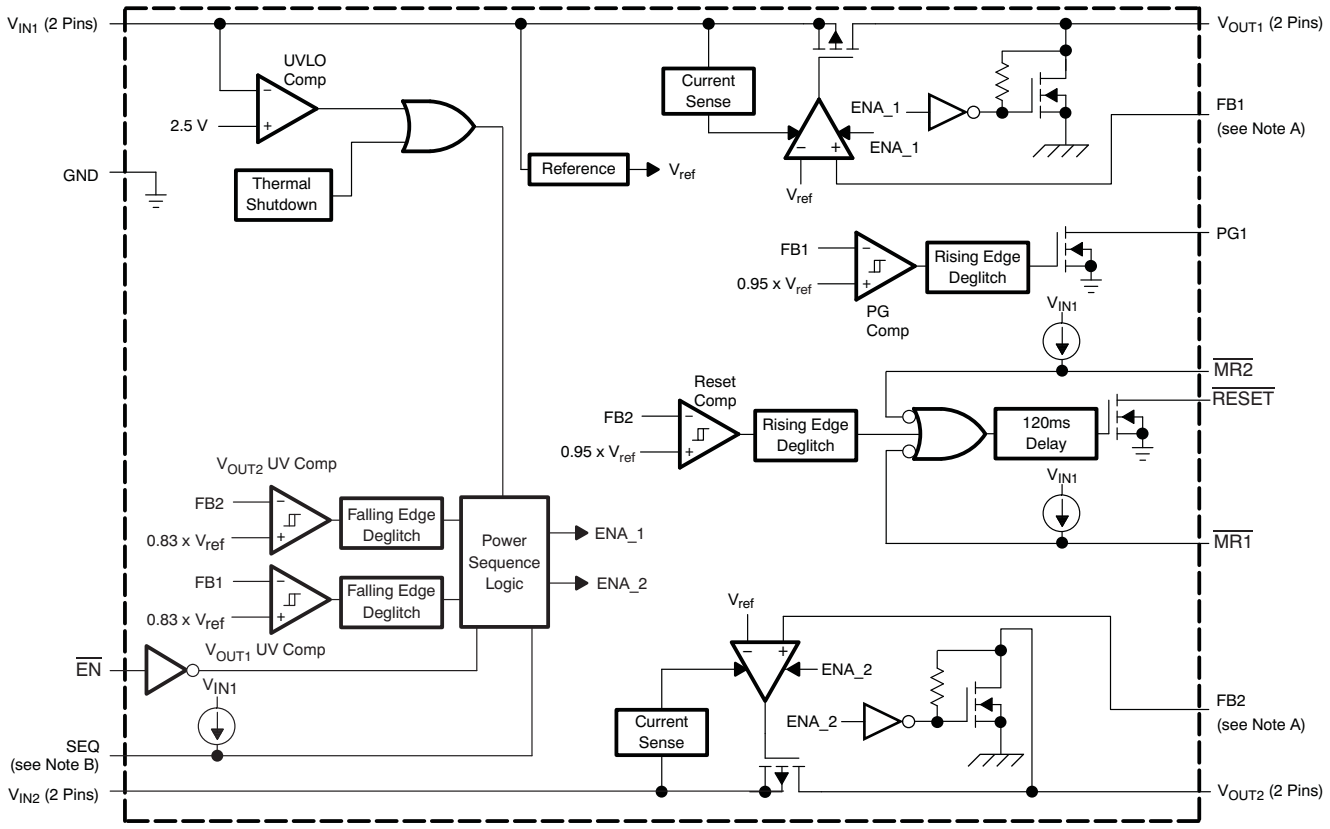
Fixed Voltage Version



A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT} as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the ***Application Information*** section.

B. If the SEQ terminal is floating at the input, V_{OUT2} powers up first.

Adjustable Voltage Version

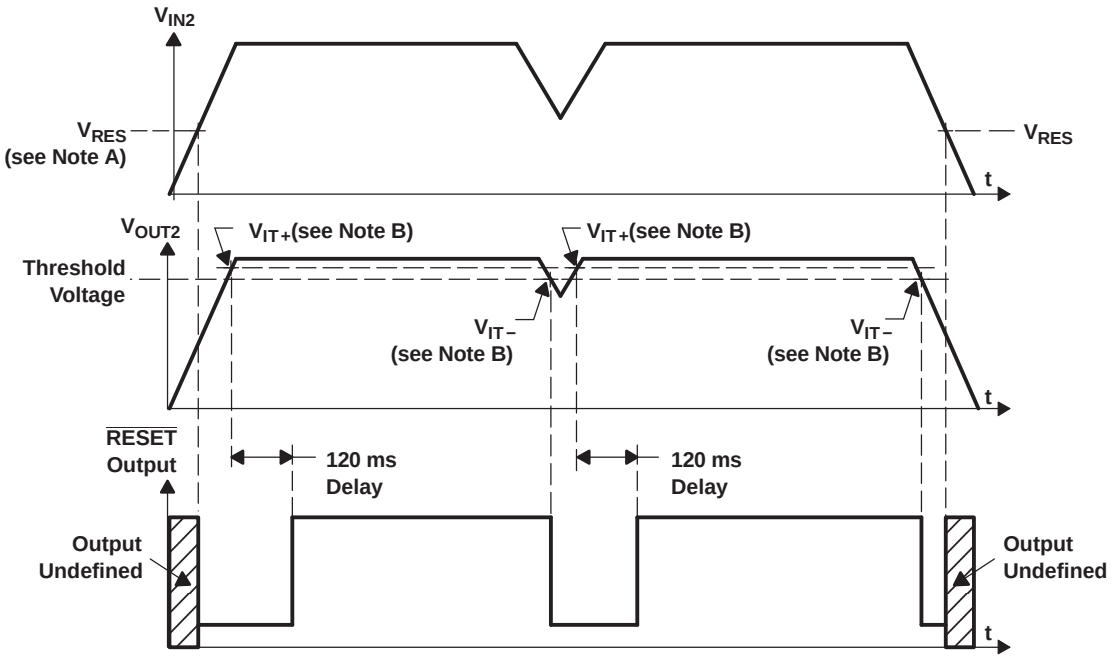


A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the ***Application Information*** section.

B. If the SEQ terminal is floating at the input, V_{OUT2} powers up first

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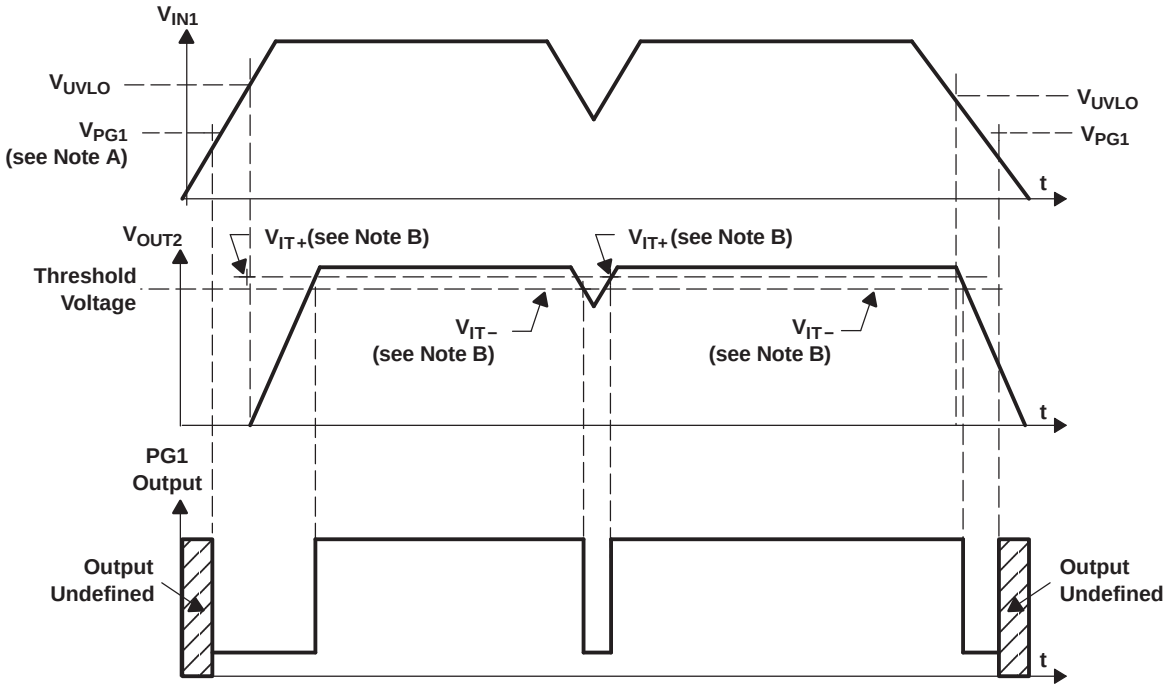
$\overline{\text{RESET}}$ Timing Diagram (with V_{IN1} Powered Up)



NOTES: A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{RES} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} −Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

PG1 Timing Diagram



NOTES: A. V_{PG1} is the minimum input voltage for a valid PG1. The symbol V_{PG1} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT} −Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

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Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	6	I	Active low enable
GND	8	—	Ground
$\overline{MR1}$	4	I	Manual reset input 1, active low, pulled up internally
$\overline{MR2}$	5	I	Manual reset input 2, active low, pulled up internally
NC	1, 11, 20	—	No connection
PG1	16	O	Open drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage
$\overline{RESET}$	15	O	Open drain output, SVS (power-on reset) signal, active low
SEQ	7	I	Power-up sequence control: SEQ = High, V_{OUT2} powers up first; SEQ = Low, V_{OUT1} powers up first, SEQ terminal pulled up internally.
V_{IN1}	2, 3	I	Input voltage of regulator 1
V_{IN2}	9, 10	I	Input voltage of regulator 2
V_{OUT1}	18, 19	O	Output voltage of regulator 1
V_{OUT2}	12, 13	O	Output voltage of regulator 2
V_{SENSE2}/FB2	14	I	Regulator 2 output voltage sense/regulator 2 feedback for adjustable
V_{SENSE1}/FB1	17	I	Regulator 1 output voltage sense/regulator 1 feedback for adjustable

Detailed Description

The TPS701xx low dropout regulator family provides dual regulated output voltages for DSP applications that require high-performance power management solutions. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This architecture reduces the component cost and board space while increasing total system reliability. The TPS701xx family has an enable feature that puts the device in sleep mode reducing the input currents to less than 3μA. Other features are integrated SVS (Power-On Reset, $\overline{RESET}$) and Power Good (PG1) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

The TPS701xx, unlike many other LDOs, feature very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS701xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage=driven, operating current is low and stable over the full load range.

Pin Functions

Enable

The $\overline{EN}$ terminal is an input that enables or shuts down the device. If $\overline{EN}$ is at a voltage high signal, the device is in shutdown mode. When $\overline{EN}$ goes to voltage low, the device is enabled.

Sequence

The SEQ terminal is an input that programs which output voltage (V_{OUT1} or V_{OUT2}) is turned on first. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} turns on first and V_{OUT1} remains off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time, V_{OUT1} is turned on. If V_{OUT2} is pulled below 83% (for example, in an overload condition) V_{OUT1} is turned off. These terminals have a 6-μA pullup current to V_{IN1}.

Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} is turned on first. For detailed timing diagrams, refer to Figure 40 through Figure 44.

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Power-Good

The PG1 is an open drain, active high output terminal that indicates the status of the V_{OUT1} regulator. When the V_{OUT1} reaches 95% of its regulated voltage, PG1 will go to a high impedance state. It will go to a low impedance state when it is pulled below 95% (for example, during an overload condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pull-up resistor.

Manual Reset Pins ($\overline{MR1}$ and $\overline{MR2}$)

$\overline{MR1}$ and $\overline{MR2}$ are active low input terminals used to trigger a reset condition. When either $\overline{MR1}$ or $\overline{MR2}$ is pulled to logic low, a POR ($\overline{RESET}$) will occur. These terminals have a 6μA pull-up current to V_{IN1}.

Sense (V_{SENSE1}, V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, sense connects to high-impedance, wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way to minimize or avoid noise pickup. Adding RC networks between the V_{SENSE} terminals and V_{OUT} terminals to filter noise is not recommended because these networks can cause the regulators to oscillate.

FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize or avoid noise pickup. Adding RC networks between the FB terminals and V_{OUT} terminals to filter noise is not recommended because these networks cause the regulators to oscillate.

$\overline{RESET}$ Indicator

The TPS701xx features a $\overline{RESET}$ (SVS, POR, or Power-On Reset). $\overline{RESET}$ can be used to drive power-on reset circuitry or a low-battery indicator. $\overline{RESET}$ is an active low, open drain output that indicates the status of the V_{OUT2} regulator and both manual reset pins ($\overline{MR1}$ and $\overline{MR2}$). When V_{OUT2} exceeds 95% of its regulated voltage, and $\overline{MR1}$ and $\overline{MR2}$ are in the high impedance state, $\overline{RESET}$ will go to a high-impedance state after 120ms delay. $\overline{RESET}$ will go to a low-impedance state when V_{OUT2} is pulled below 95% (for example, an overload condition) of its regulated voltage. To monitor V_{OUT1}, the PG1 output pin can be connected to $\overline{MR1}$ or $\overline{MR2}$. The open drain output of the $\overline{RESET}$ terminal requires a pullup resistor. If $\overline{RESET}$ is not used, it can be left floating.

V_{IN1} and V_{IN2}

V_{IN1} and V_{IN2} are input to the regulators. **Internal bias voltages are powered by V_{IN1}.**

V_{OUT1} and V_{OUT2}

V_{OUT1} and V_{OUT2} are output terminals of the LDO.

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TYPICAL CHARACTERISTICS

Table 2. Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	Figure 1 to Figure 3
		vs Temperature	Figure 4 to Figure 7
	Ground current	vs Junction temperature	Figure 8
PSRR	Power-supply rejection ratio	vs Frequency	Figure 9 to Figure 12
	Output spectral noise density	vs Frequency	Figure 13 to Figure 16
Z_O	Output impedance	vs Frequency	Figure 17 to Figure 20
	Dropout voltage	vs Temperature	Figure 21 and Figure 22
		vs Input voltage	Figure 23 and Figure 24
	Load transient response		Figure 25 and Figure 26
	Line transient response		Figure 27 and Figure 28
V_O	Output voltage and enable voltage	vs Time (start-up)	Figure 29 and Figure 30
	Equivalent series resistance	vs Output current	Figure 31 to Figure 38
	Test circuit for typical regions of stability (equivalent series resistance) performance		Figure 39

TPS70151
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

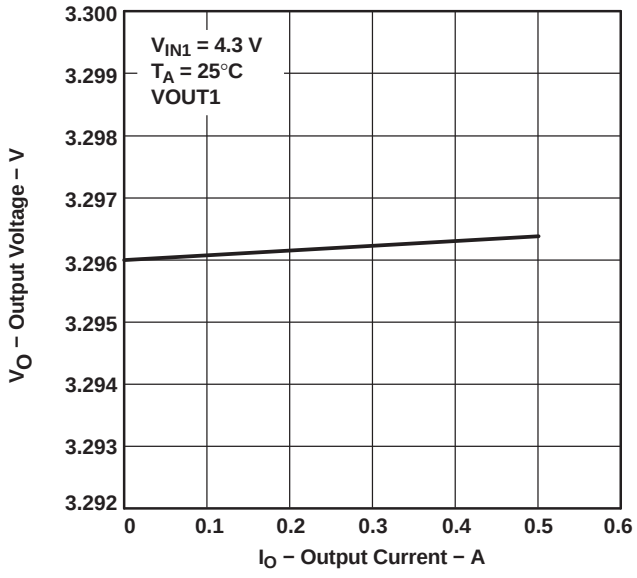


Figure 1.

TPS70151
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

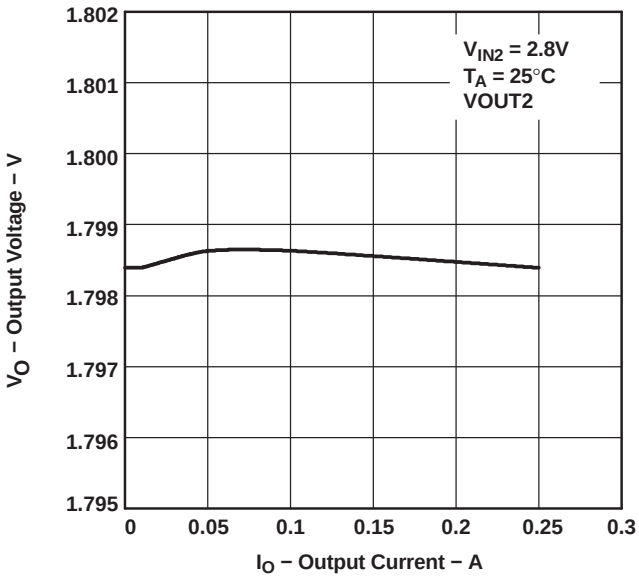


Figure 2.

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TPS70145
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

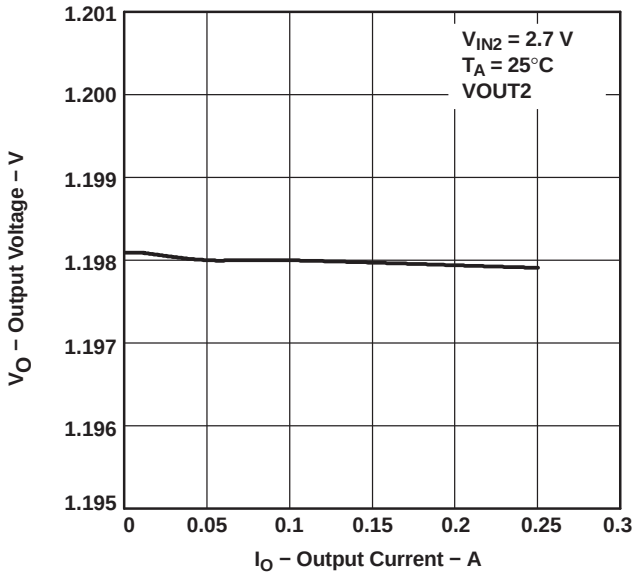


Figure 3.

TPS70151
OUTPUT VOLTAGE
vs
TEMPERATURE

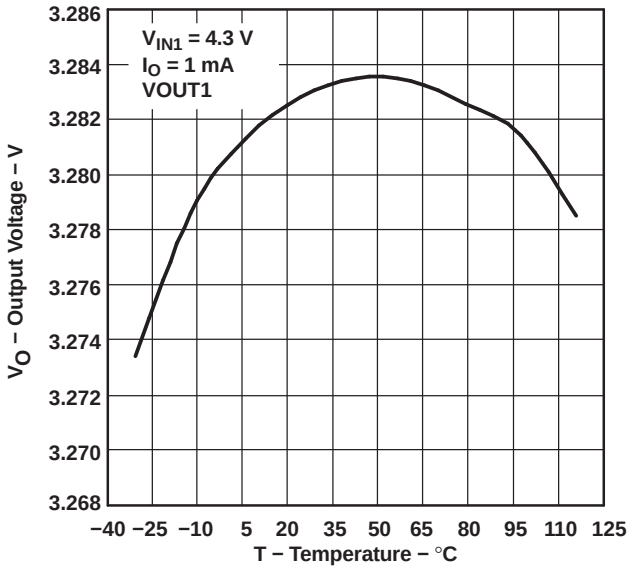


Figure 4.

TPS70151
OUTPUT VOLTAGE
vs
TEMPERATURE

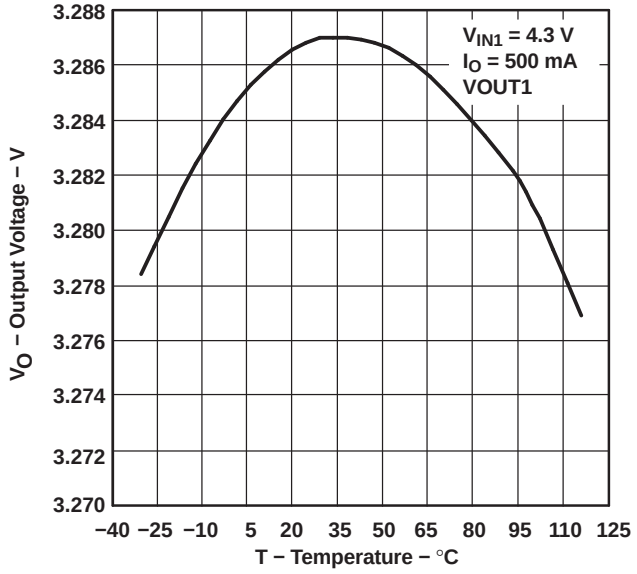


Figure 5.

TPS70151
OUTPUT VOLTAGE
vs
TEMPERATURE

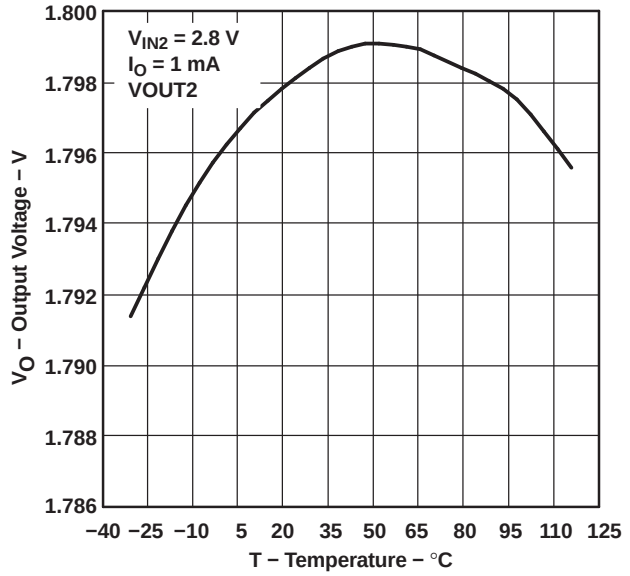


Figure 6.

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TPS70151
OUTPUT VOLTAGE
vs
TEMPERATURE

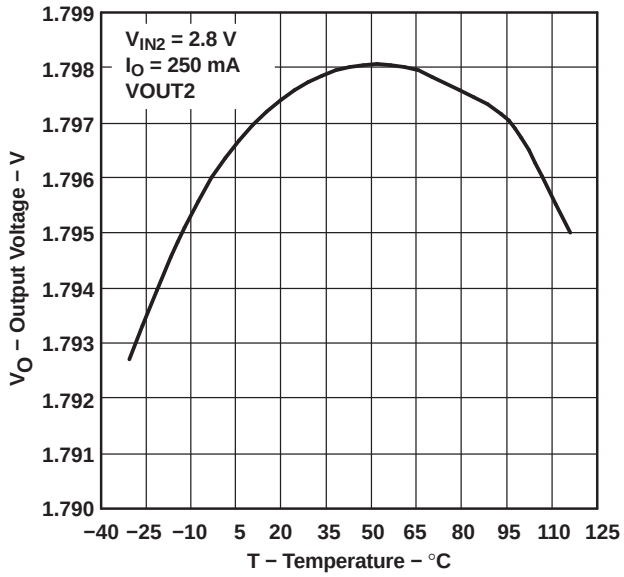


Figure 7.

GROUND CURRENT
vs
JUNCTION TEMPERATURE

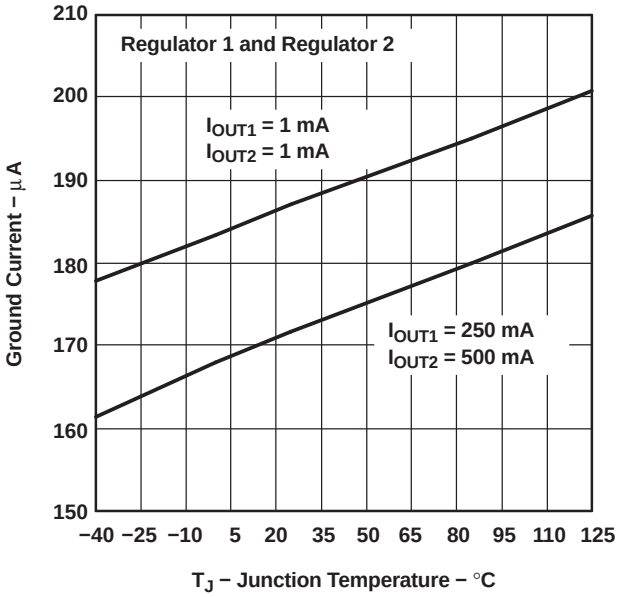


Figure 8.

TPS70151
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

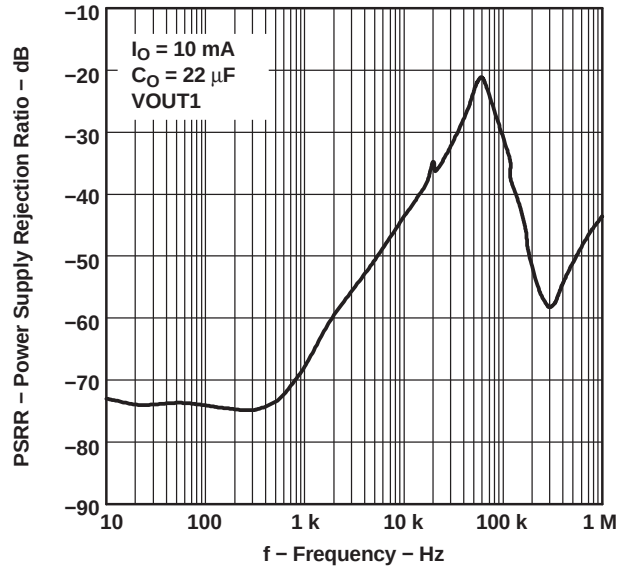


Figure 9.

TPS70151
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

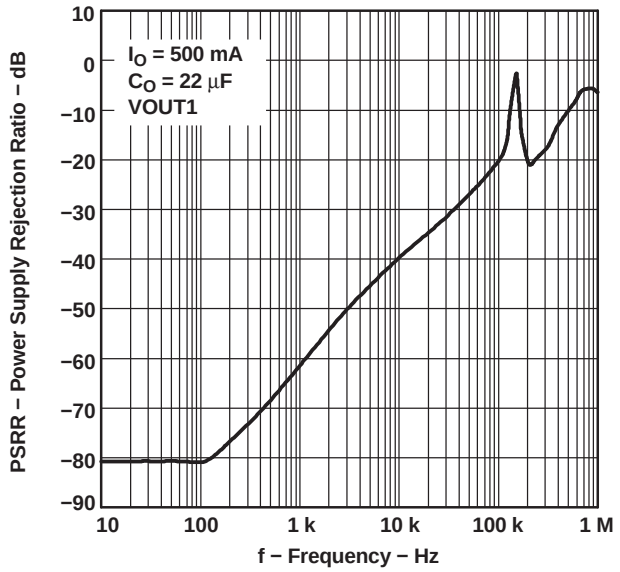


Figure 10.

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TPS70151
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

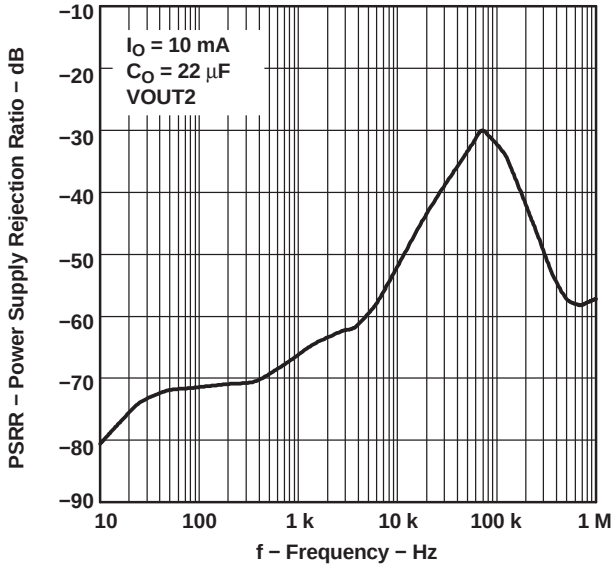


Figure 11.

TPS70151
POWER-SUPPLY REJECTION RATIO
vs
FREQUENCY

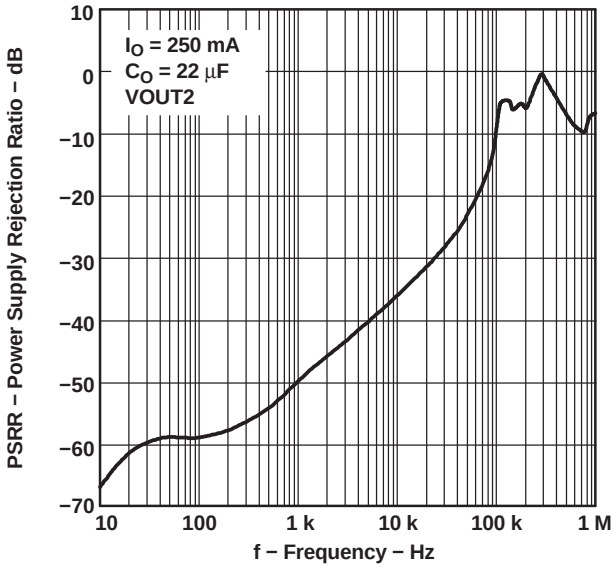


Figure 12.

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

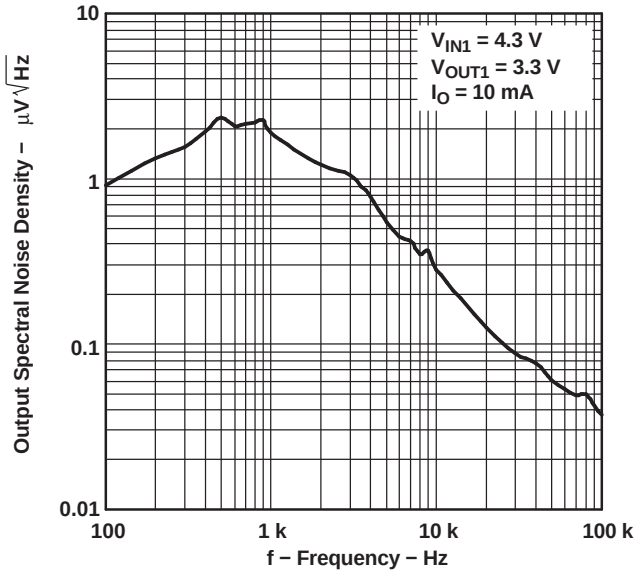


Figure 13.

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

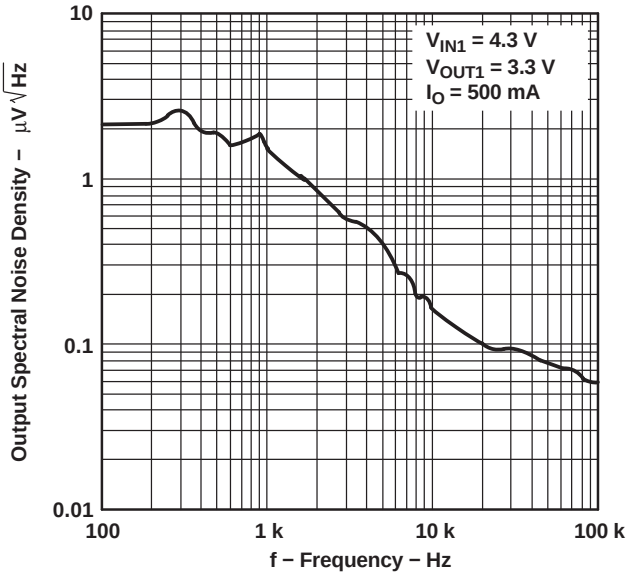


Figure 14.

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OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

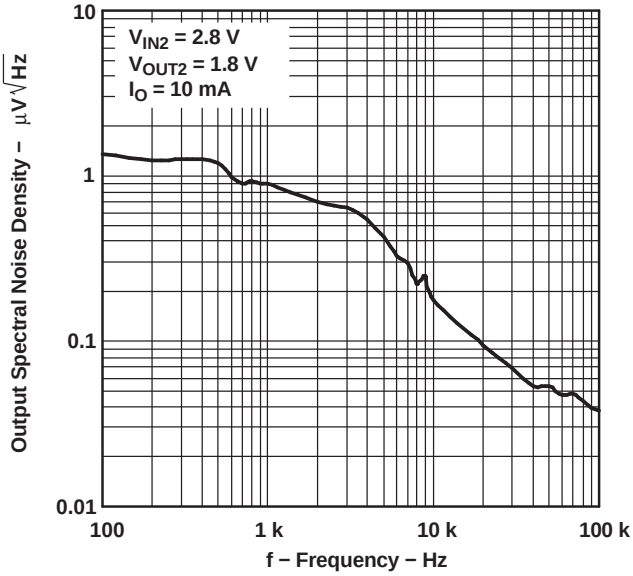


Figure 15.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

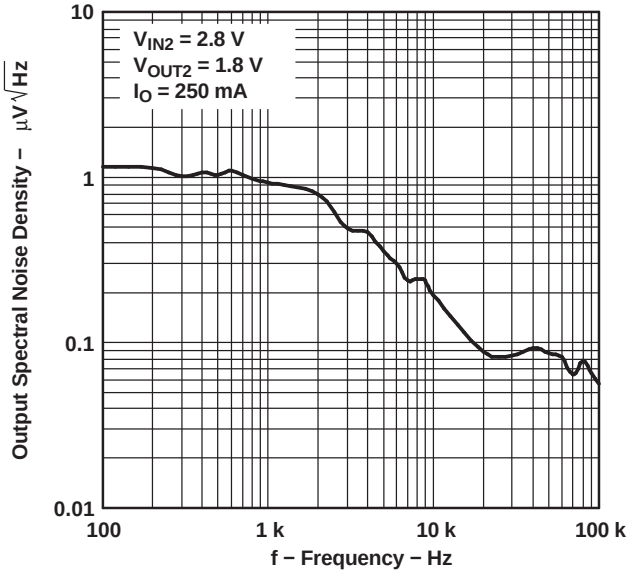


Figure 16.

OUTPUT IMPEDANCE vs FREQUENCY

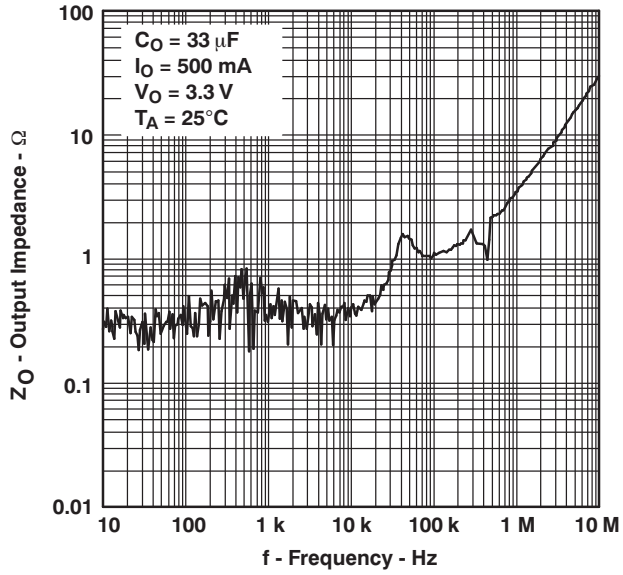


Figure 17.

OUTPUT IMPEDANCE vs FREQUENCY

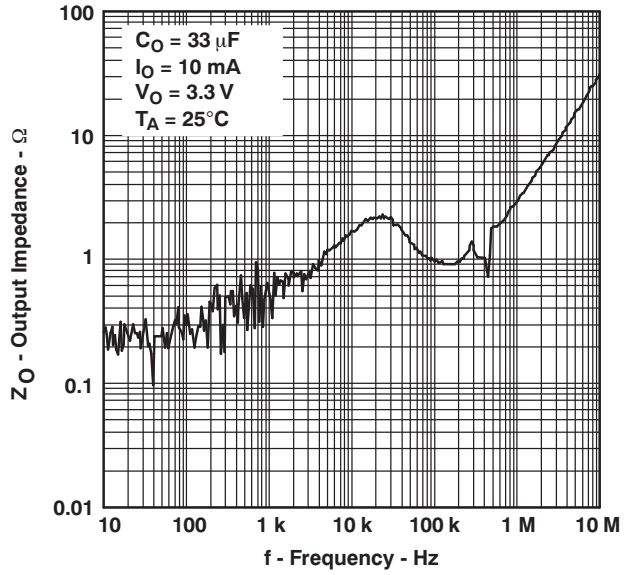


Figure 18.

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OUTPUT IMPEDANCE vs FREQUENCY

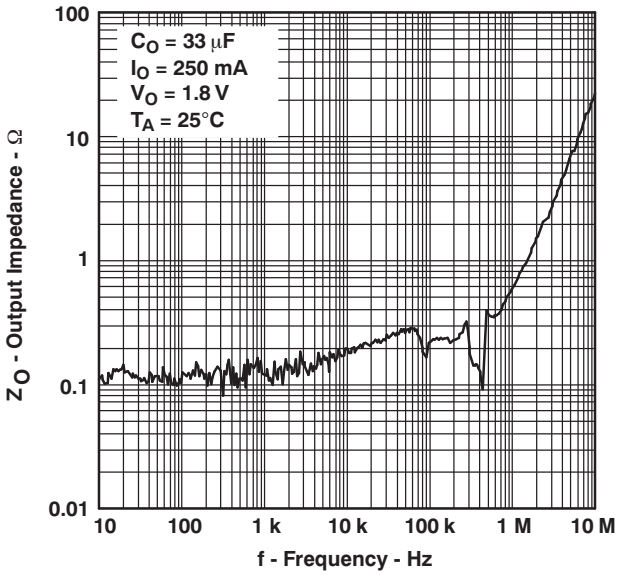


Figure 19.

OUTPUT IMPEDANCE vs FREQUENCY

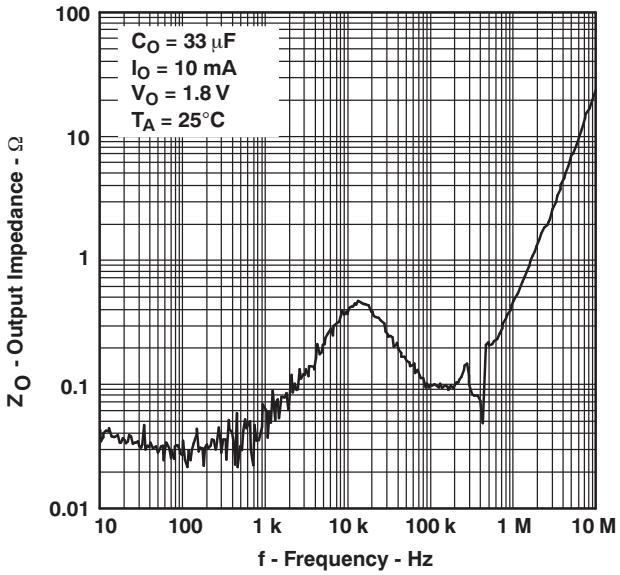


Figure 20.

DROPOUT VOLTAGE vs TEMPERATURE

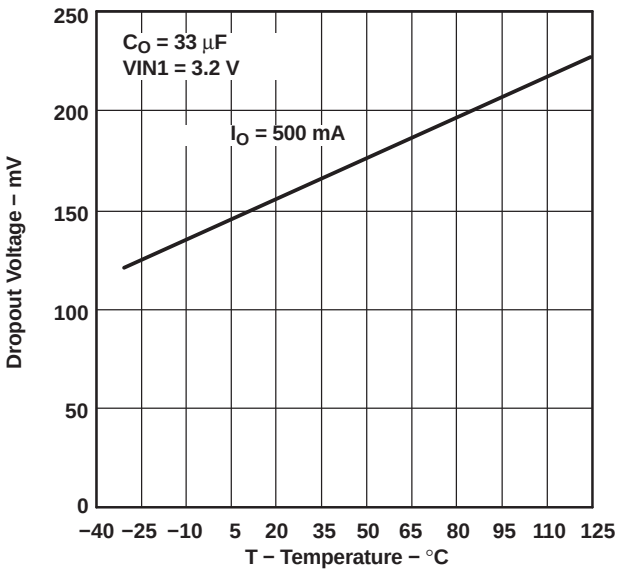


Figure 21.

DROPOUT VOLTAGE vs TEMPERATURE

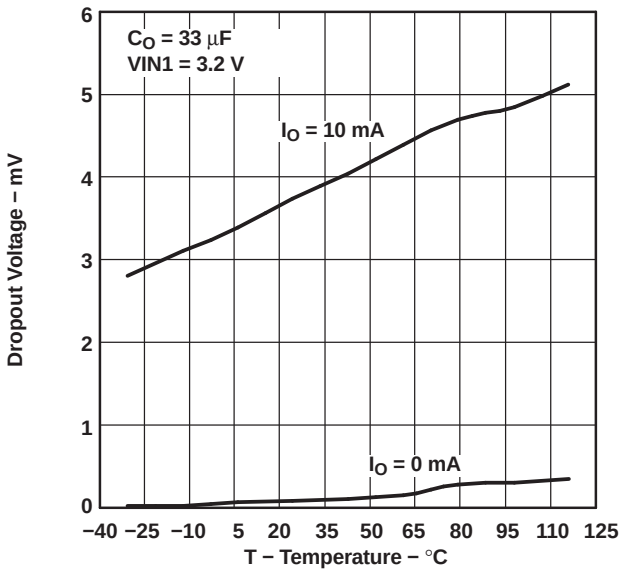


Figure 22.

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TPS70102
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

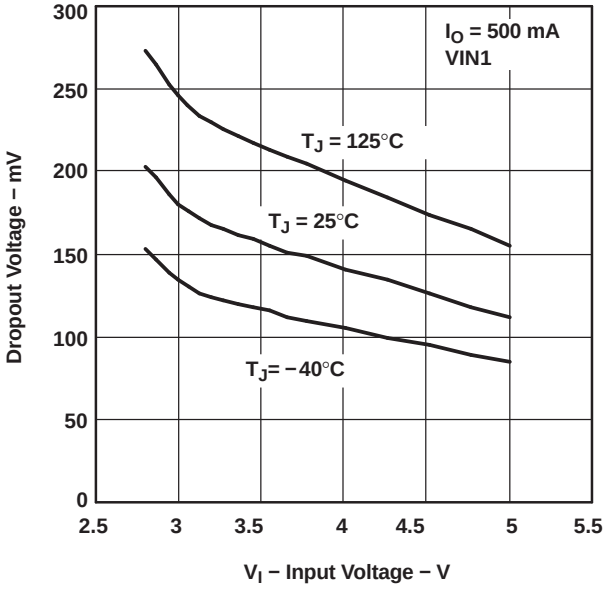


Figure 23.

TPS70102
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

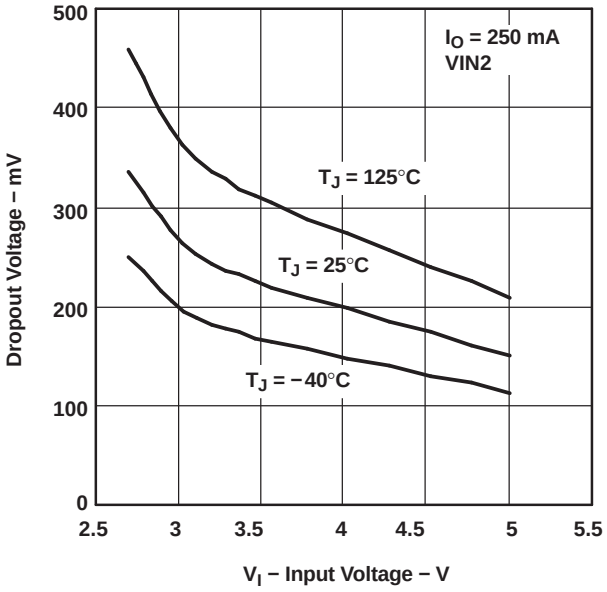


Figure 24.

LOAD TRANSIENT RESPONSE

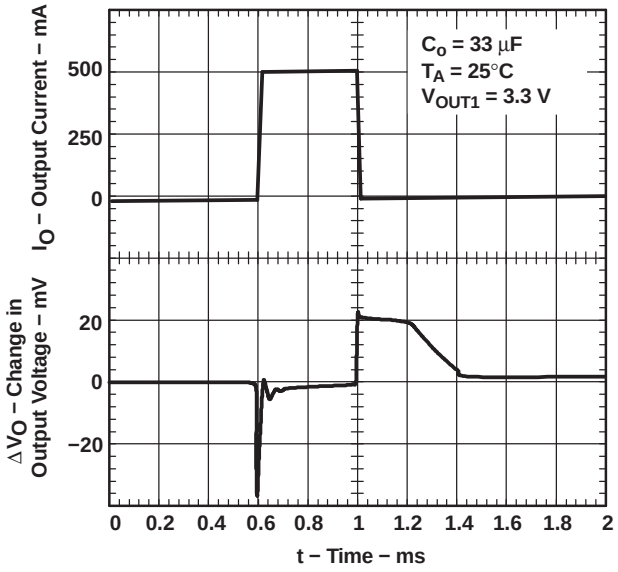


Figure 25.

LOAD TRANSIENT RESPONSE

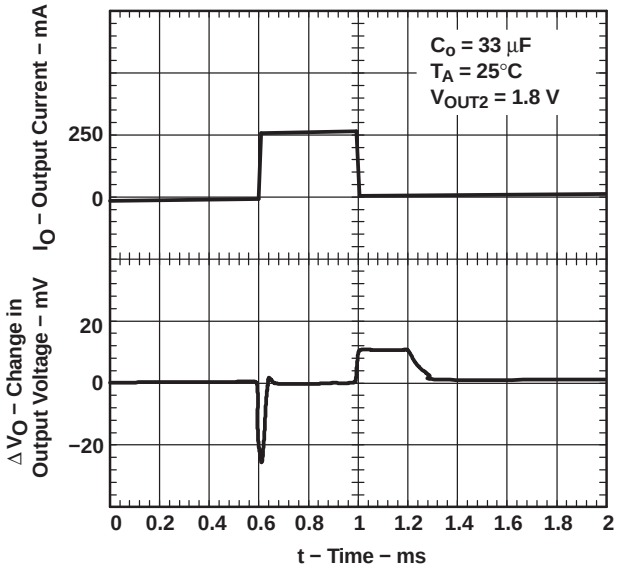


Figure 26.

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LINE TRANSIENT RESPONSE

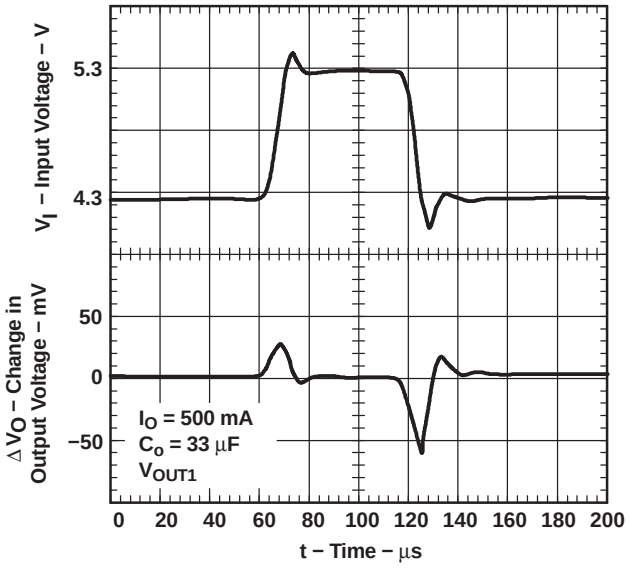


Figure 27.

LINE TRANSIENT RESPONSE

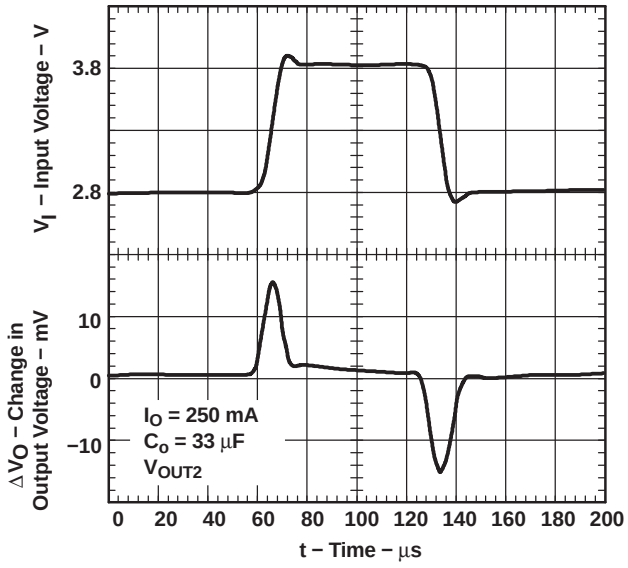


Figure 28.

OUTPUT VOLTAGE AND ENABLE VOLTAGE
vs
TIME (START-UP)

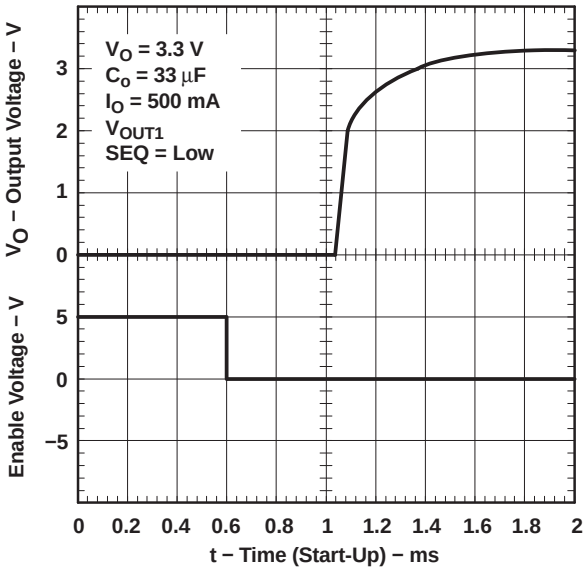


Figure 29.

OUTPUT VOLTAGE AND ENABLE VOLTAGE
vs
TIME (START-UP)

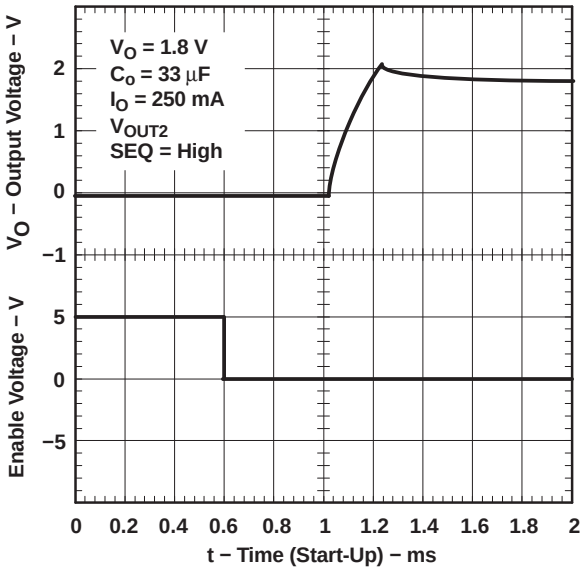


Figure 30.

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TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

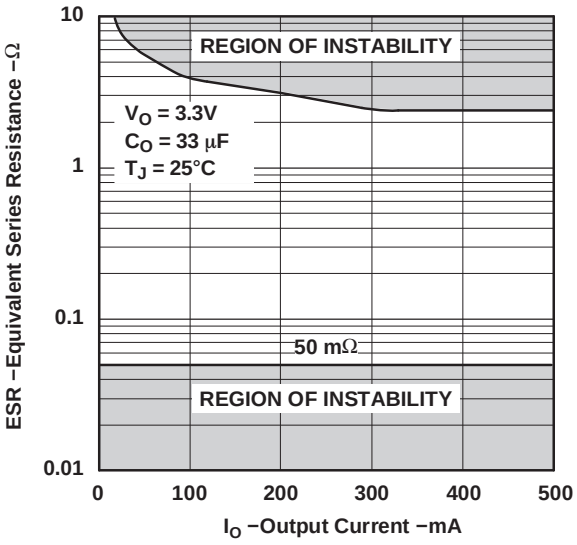


Figure 31.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

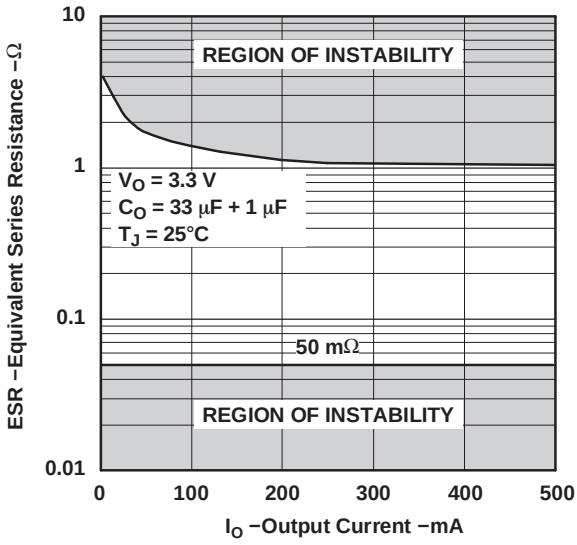


Figure 32.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

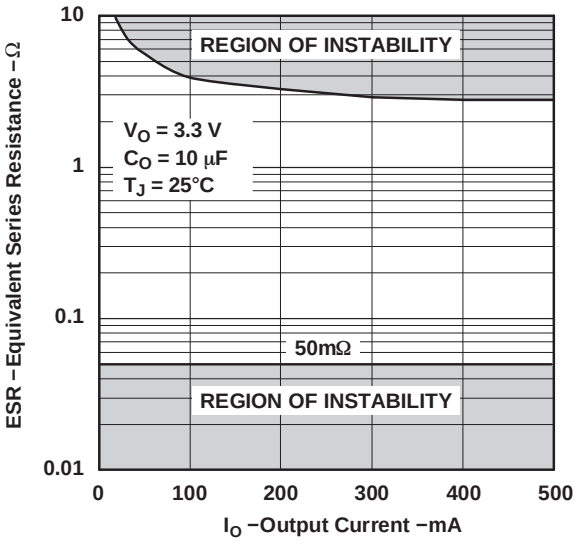


Figure 33.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

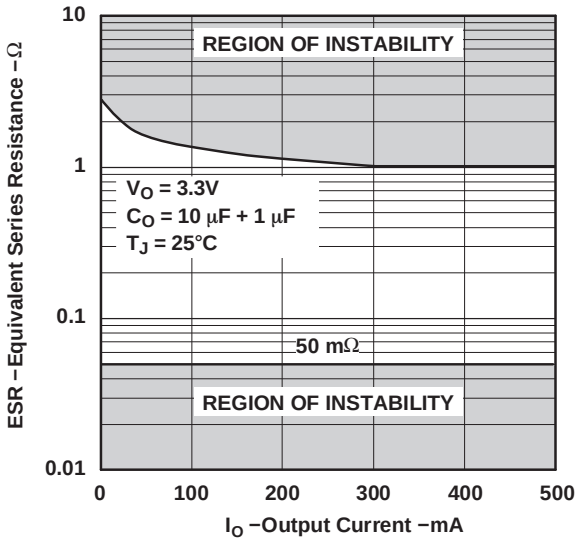


Figure 34.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

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TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

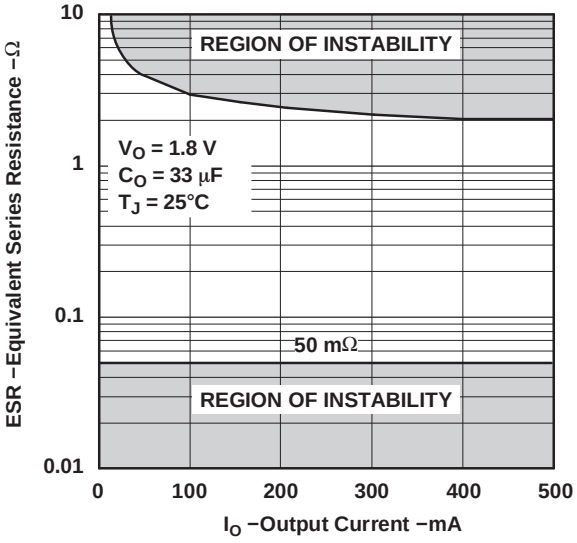


Figure 35.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

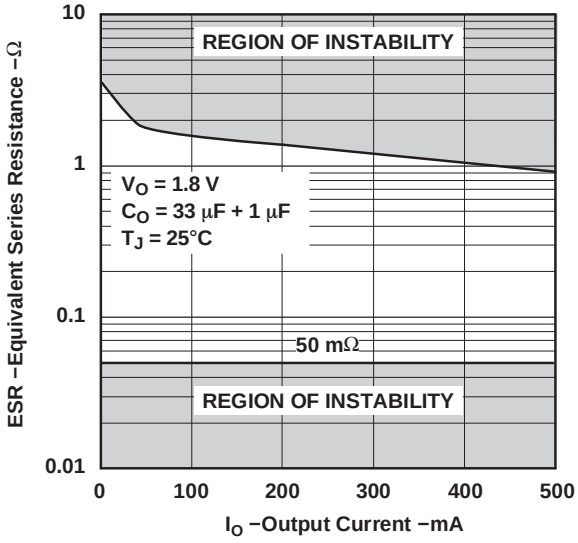


Figure 36.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

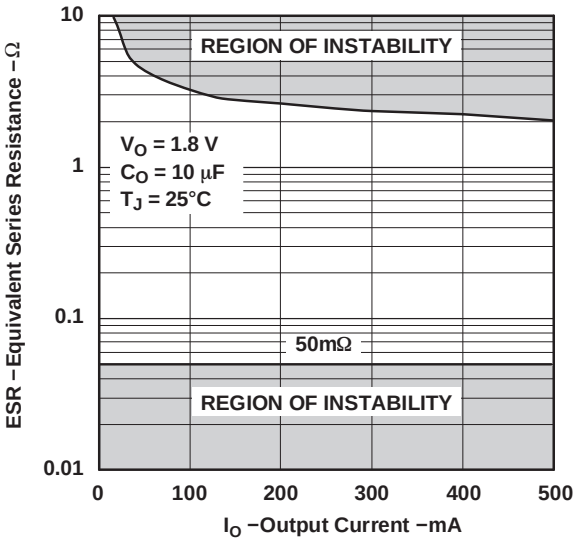


Figure 37.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

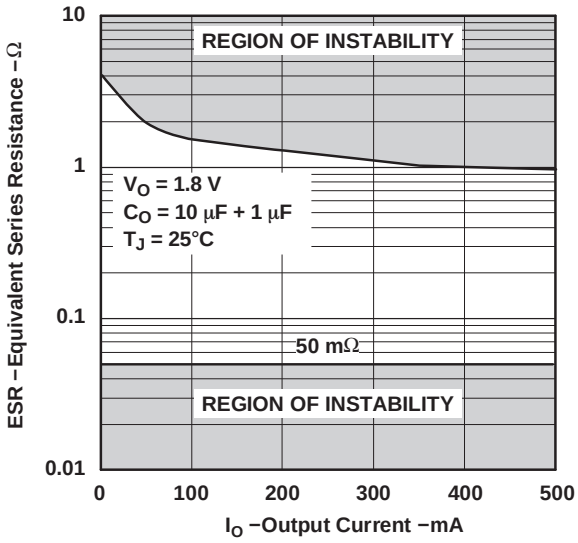


Figure 38.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

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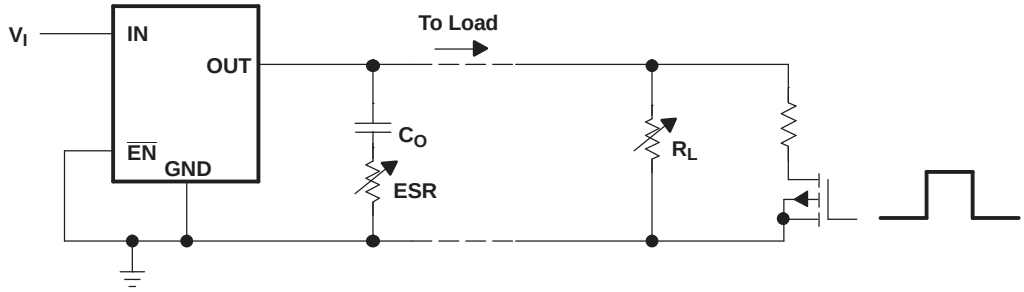


Figure 39. Test Circuit for Typical Regions of Stability

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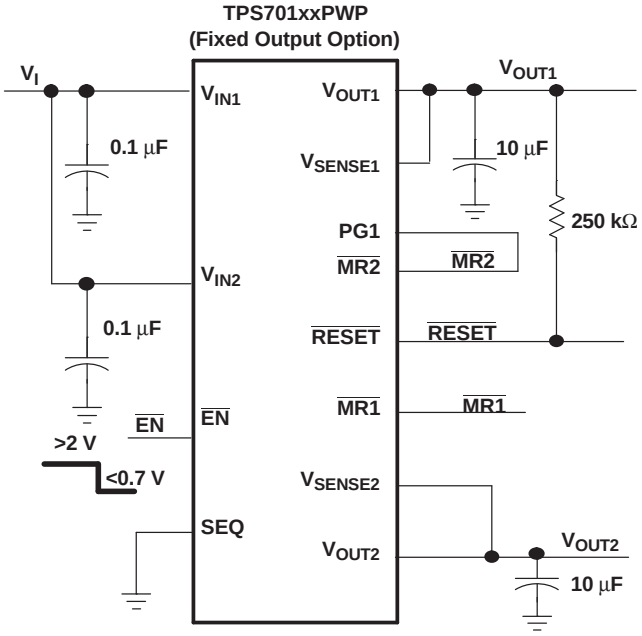
APPLICATION INFORMATION

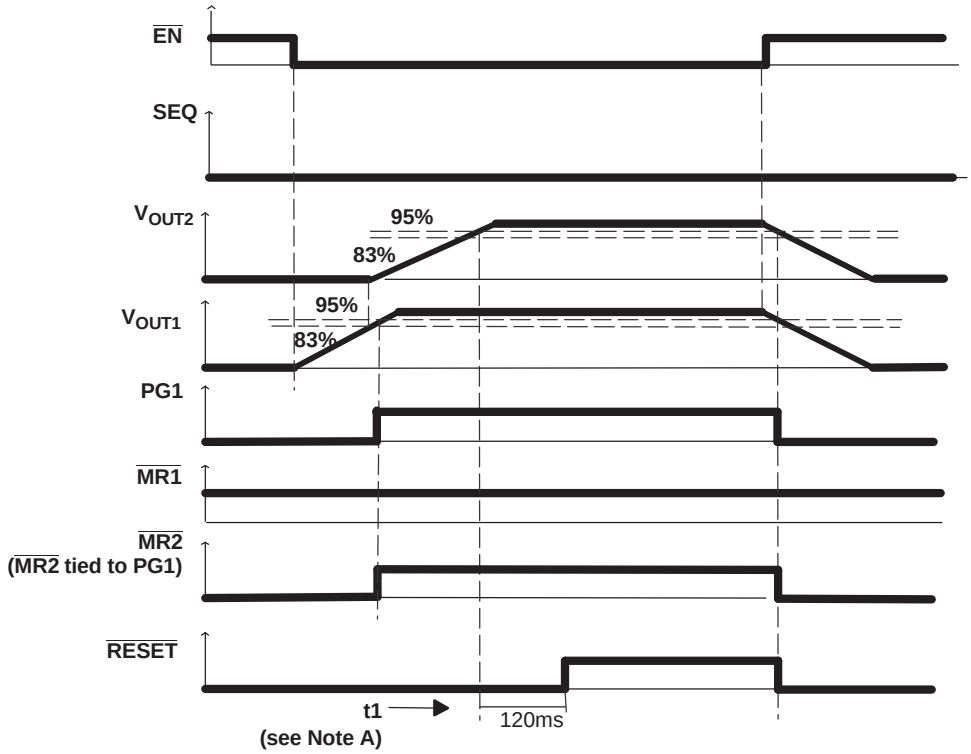
Sequencing Timing Diagrams

This section provides a number of timing diagrams showing how this device functions in different configurations.

Application condition: $\overline{MR2}$ is tied to PG1, V_{IN1} and V_{IN2} are tied to the same input voltage, the SEQ pin is tied to logic low and the device is toggled with the enable ($\overline{EN}$) function.

When the device is enabled ($\overline{EN}$ is pulled low), V_{OUT1} turns on first and V_{OUT2} remains off until V_{OUT1} reaches approximately 83% of its regulated output voltage. At that time, V_{OUT2} is turned on. When V_{OUT1} reaches 95% of its regulated output, PG1 turns on (active high). Since $\overline{MR2}$ is connected to PG1 for this application, it follows PG1. When V_{OUT2} reaches 95% of its regulated voltage, $\overline{RESET}$ switches to high voltage level after a 120ms delay (see Figure 40).



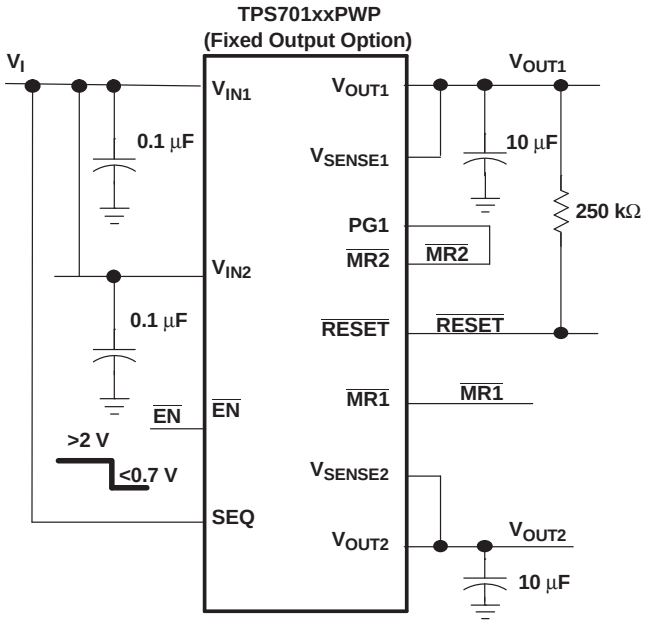


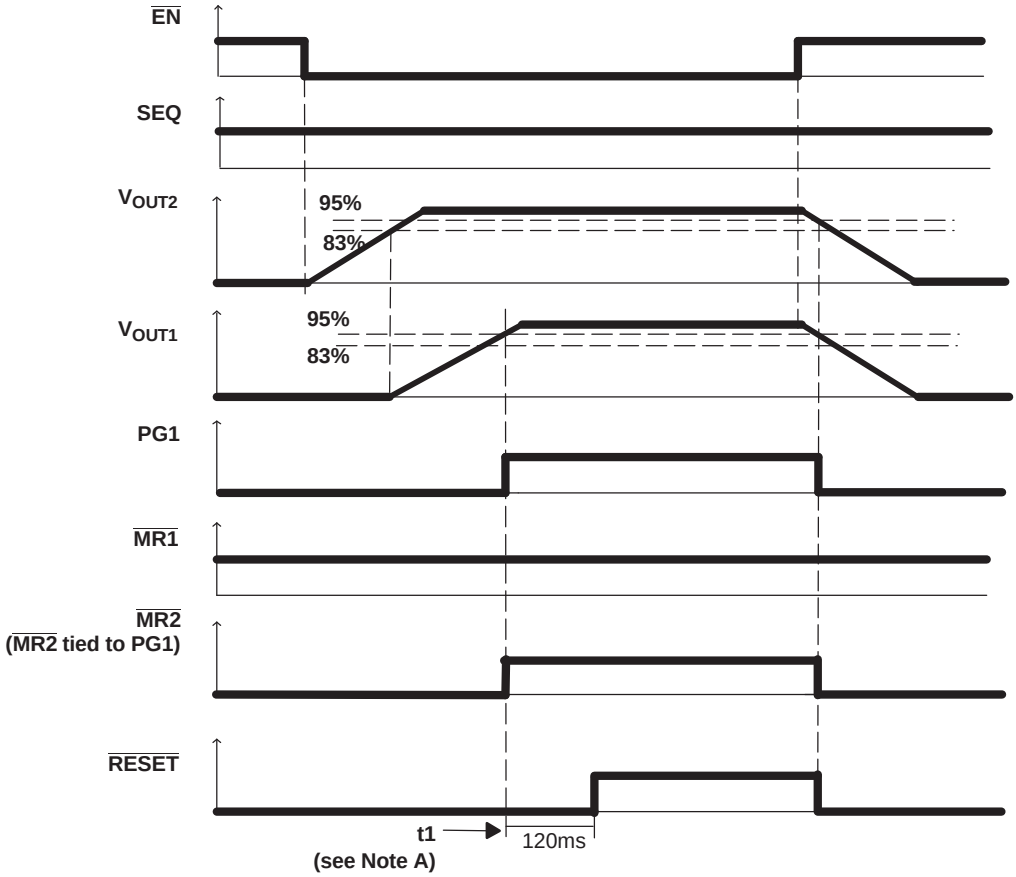
NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

Figure 40. Timing when SEQ = Low

Application condition: $\overline{MR2}$ is tied to PG1, V_{IN1} and V_{IN2} are tied to the same input voltage, the SEQ pin is tied to logic high and the device is toggled with the enable ($\overline{EN}$) function.

When the device is enabled ($\overline{EN}$ is pulled low), V_{OUT2} begins to power up. When it reaches 83% of its regulated voltage, V_{OUT1} begins to power up. PG1 turns on when V_{OUT1} reaches 95% of its regulated voltage, and since $\overline{MR2}$ and PG1 are tied together, $\overline{MR2}$ follows PG1. When V_{OUT1} reaches 95% of its regulated voltage, $\overline{RESET}$ switches to high voltage level after a 120ms delay (see Figure 41).





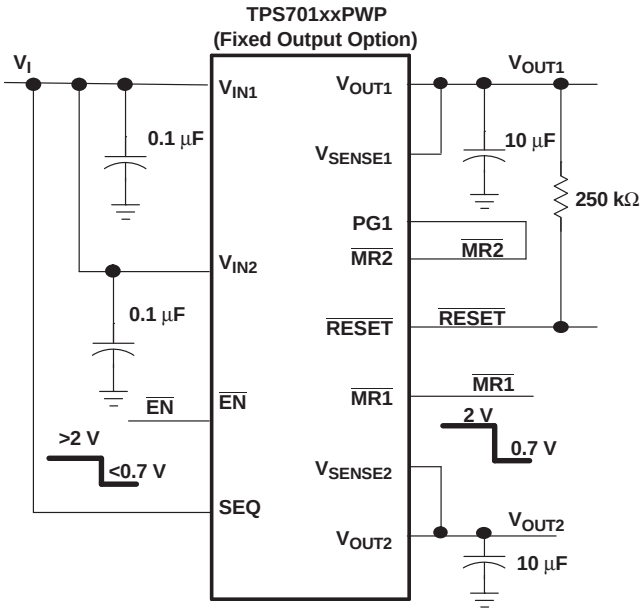
NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

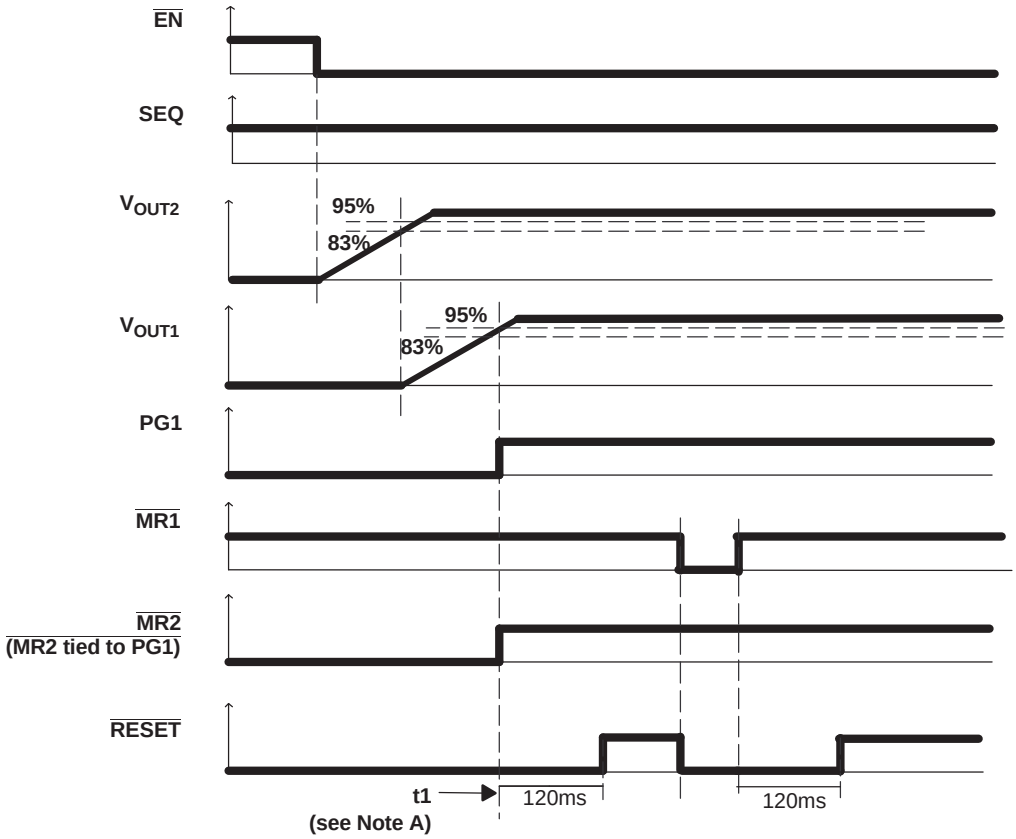
Figure 41. Timing when SEQ = High

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Application condition: $\overline{MR2}$ is tied to PG1, V_{IN1} and V_{IN2} are tied to the same input voltage, the SEQ pin is tied to logic high and $\overline{MR1}$ is toggled.

When the device is enabled ($\overline{EN}$ is pulled low), V_{OUT2} begins to power up. When it reaches 83% of its regulated voltage, V_{OUT1} begins to power up. PG1 turns on when V_{OUT1} reaches to 95% of its regulated voltage, and since $\overline{MR2}$ and PG1 are tied together, $\overline{MR2}$ follows PG1. When V_{OUT1} reaches 95% of its regulated voltage, the $\overline{RESET}$ switches to high voltage level after a 120ms delay. When $\overline{MR1}$ is pulled low, it causes $\overline{RESET}$ to go low, but the regulators remains in regulation (see Figure 42).



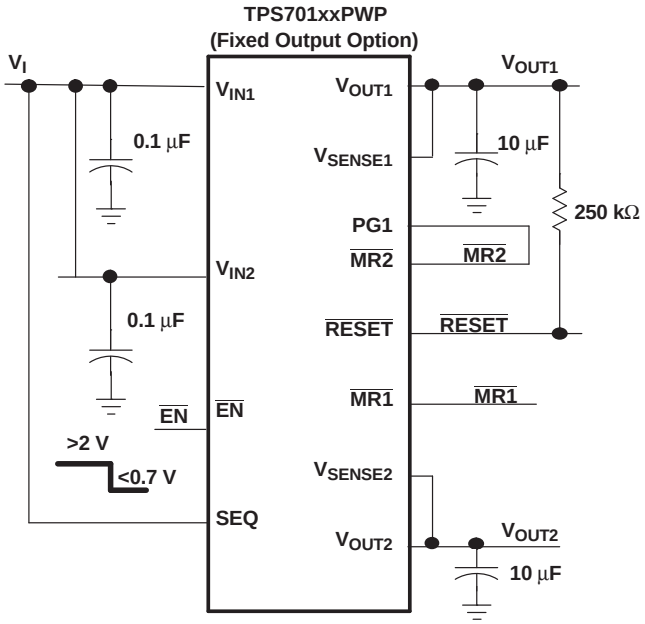


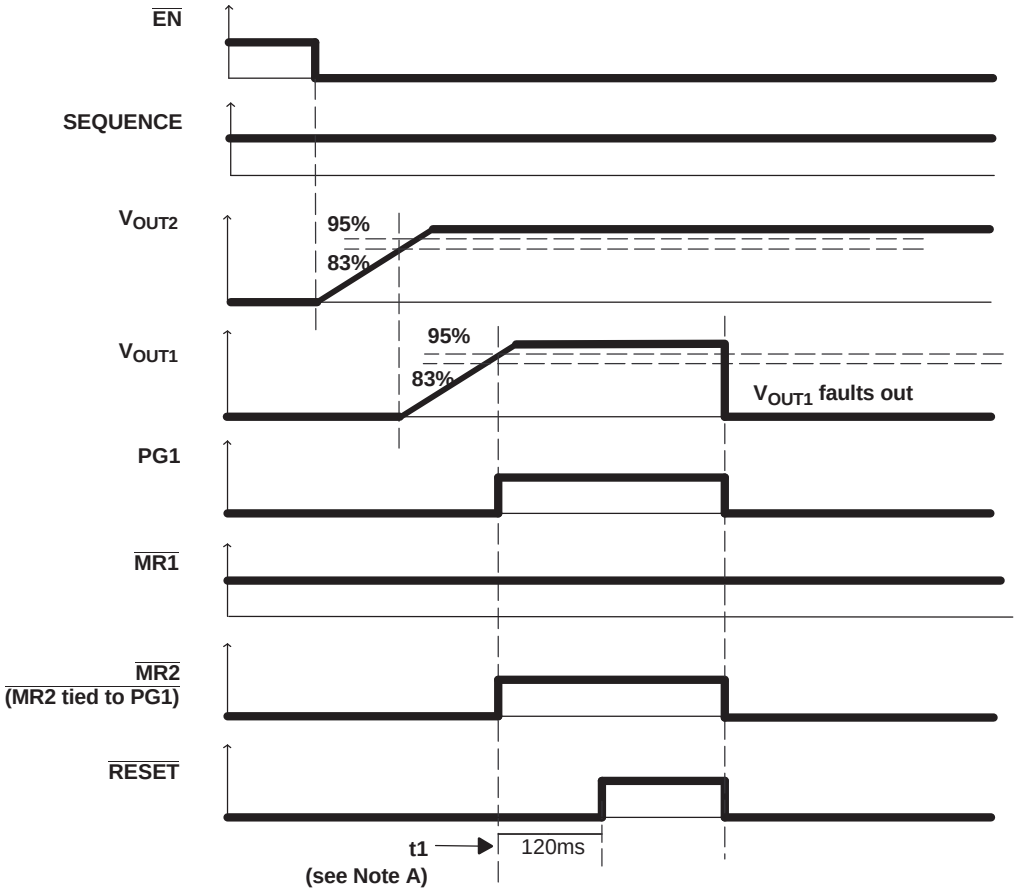
NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

Figure 42. Timing when $\overline{MR1}$ is Toggled

Application condition: $\overline{MR2}$ is tied to PG1, V_{IN1} and V_{IN2} are tied to the same input voltage, the SEQ pin is tied to logic high and V_{OUT1} faults out.

V_{OUT2} begins to power up when the device is enabled ($\overline{EN}$ is pulled low). When V_{OUT2} reaches 83% of its regulated voltage, then V_{OUT1} begins to power up. When V_{OUT1} reaches 95% of its regulated voltage, PG1 turns on and $\overline{RESET}$ switches to high voltage level after a 120ms delay. When V_{OUT1} faults out, V_{OUT2} remains powered on because the SEQ pin is high. PG1 is tied to $\overline{MR2}$ and both change state to logic low. $\overline{RESET}$ is driven by $\overline{MR2}$ and goes to logic low when V_{OUT1} faults out (see Figure 43).





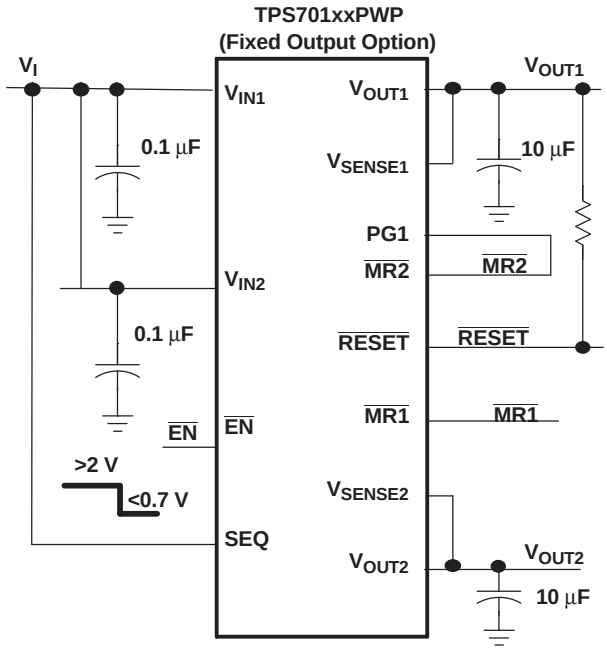
NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

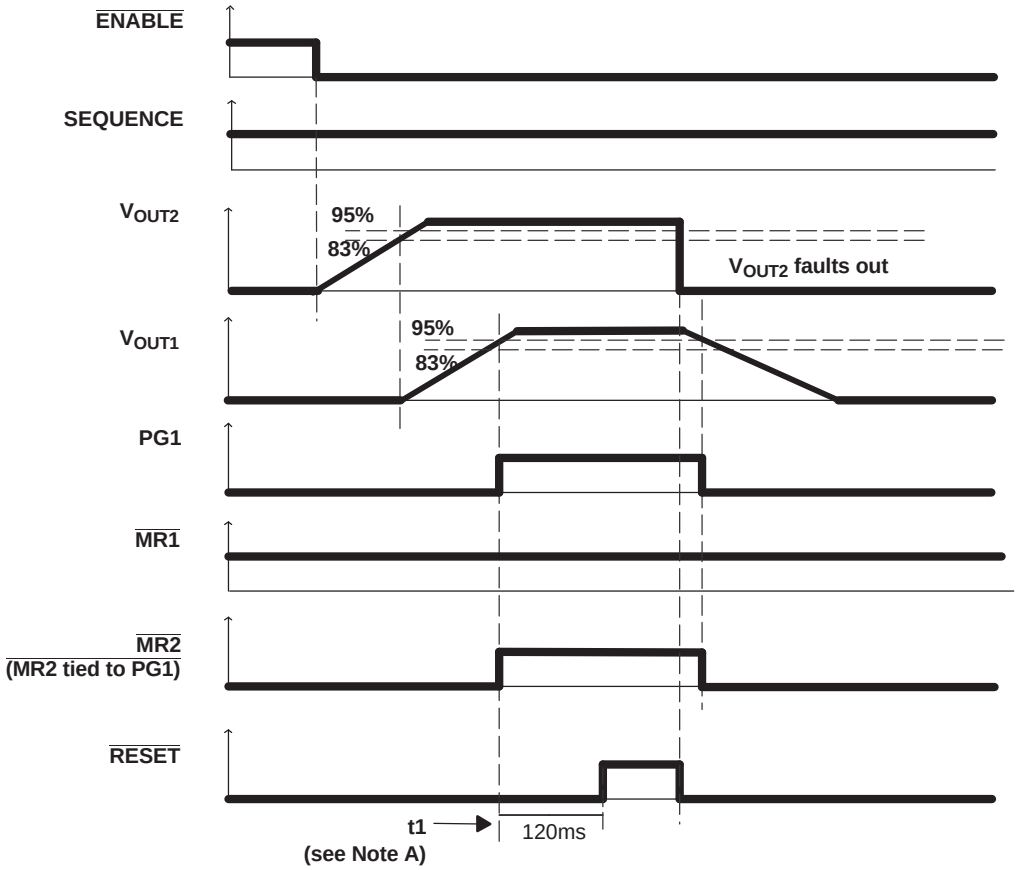
Figure 43. Timing when V_{OUT1} Faults Out

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Application condition: $\overline{MR2}$ is tied to PG1, V_{IN1} and V_{IN2} are tied to same input voltage, the SEQ is tied to logic high, the device is enabled, and V_{OUT2} faults out.

V_{OUT2} begins to power up when the device is enabled ($\overline{EN}$ is pulled low). When V_{OUT2} reaches 83% of its regulated voltage, V_{OUT1} begins to power up. When V_{OUT1} reaches 95% of its regulated voltage, PG1 turns on and $\overline{RESET}$ switches to high voltage level after a 120ms delay. When V_{OUT2} faults out, V_{OUT1} is powered down because SEQ is high. PG1 is tied to MR2 and both change state to logic low. $\overline{RESET}$ goes low when V_{OUT2} faults out (see Figure 44).



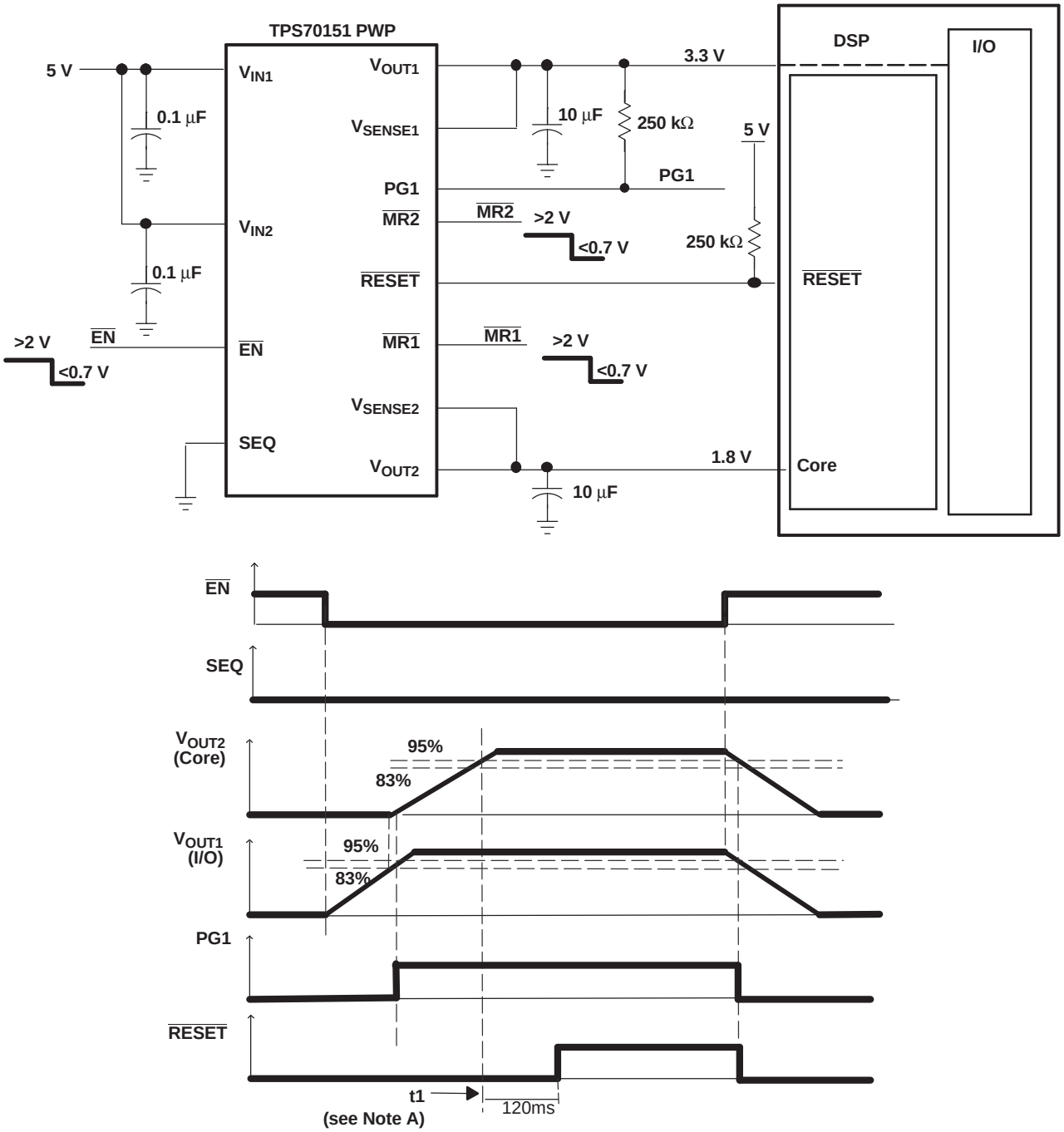


NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

Figure 44. Timing when V_{OUT2} Faults Out

Split Voltage DSP Application

Figure 45 shows a typical application where the TPS70151 is powering up a DSP. In this application, by grounding the SEQ pin, V_{OUT1} (I/O) is powered up first, and then V_{OUT2} (core).

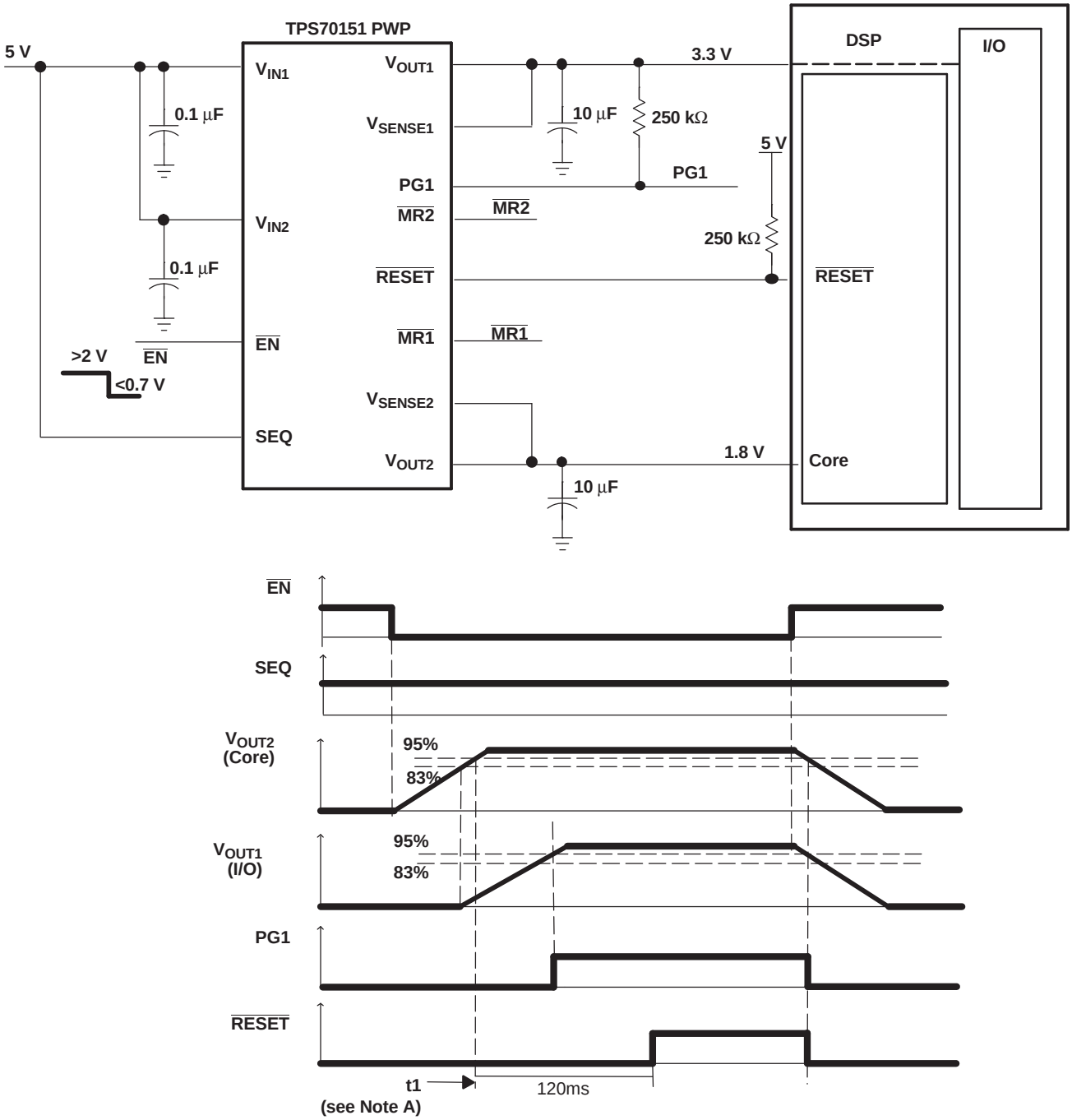


NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

Figure 45. Application Timing Diagram (SEQ = Low)

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Figure 46 shows a typical application where the TPS70151 is powering up a DSP. In this application, by pulling up the SEQ pin, V_{OUT2} (core) is powered up first, and then V_{OUT1} (I/O).



NOTE A: t1 − Time at which both V_{OUT1} and V_{OUT2} are greater than the PG1 thresholds and $\overline{MR1}$ is logic high.

Figure 46. Application Timing Diagram (SEQ = High)

Input Capacitor

For a typical application, an input bypass capacitor (0.1µF to 1µF) is recommended. This capacitor filters any high-frequency noise generated in the line. For fast transient conditions where droop at the input of the LDO may occur because of high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor depends on the output current and response time of the main power supply, as well as the distance to the V_I pins of the LDO.

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Output Capacitor

As with most LDO regulators, the TPS701xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10μF and the ESR (equivalent series resistance) must be between 50mΩ and 2.5Ω. Capacitor values 10μF or larger are acceptable, provided the ESR is less than 2.5Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Table 3 provides a partial listing of surface-mount capacitors suitable for use with the TPS701xx for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

Table 3. Partial Listing of TPS701xx-Compatible Surface-Mount Capacitors

VALUE	MANUFACTURER	MAXIMUM ESR	MFR PART NO.
22μF	Kemet	345mΩ	7495C226K0010AS
33μF	Sanyo	100mΩ	10TPA33M
47μF	Sanyo	100mΩ	6TPA47M
68μF	Sanyo	45mΩ	10TPC68M

ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called *equivalent series resistance* (ESR), and the inductive impedance is called *equivalent series inductance* (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 47.



Figure 47. ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

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Figure 48 shows the output capacitor and its parasitic resistances in a typical LDO output stage.

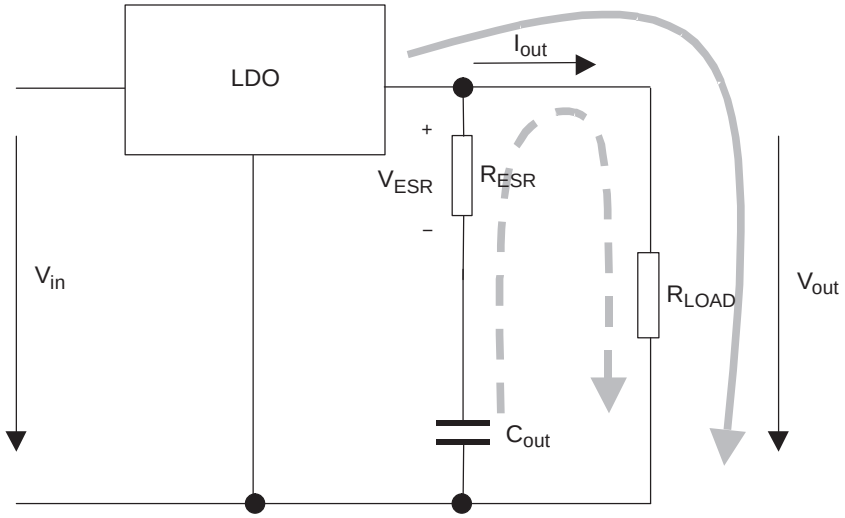


Figure 48. LDO Output Stage with Parasitic Resistances ESR

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V_{(CO)} = V_{OUT}$). This condition means no current is flowing into the C_O branch. If I_{OUT} suddenly increases (a transient condition), the following results occur:

- The LDO is not able to supply the sudden current need because of its response time (t_1 in Split Voltage DSP Application). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at R_{ESR}. This voltage is shown as V_{ESR} in Figure 44.
- When C_O is conducting current to the load, initial voltage at the load will be $V_O = V_{(CO)} – V_{ESR}$. As a result of the discharge of C_O, the output voltage V_O drops continuously until the response time t_1 of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 49.

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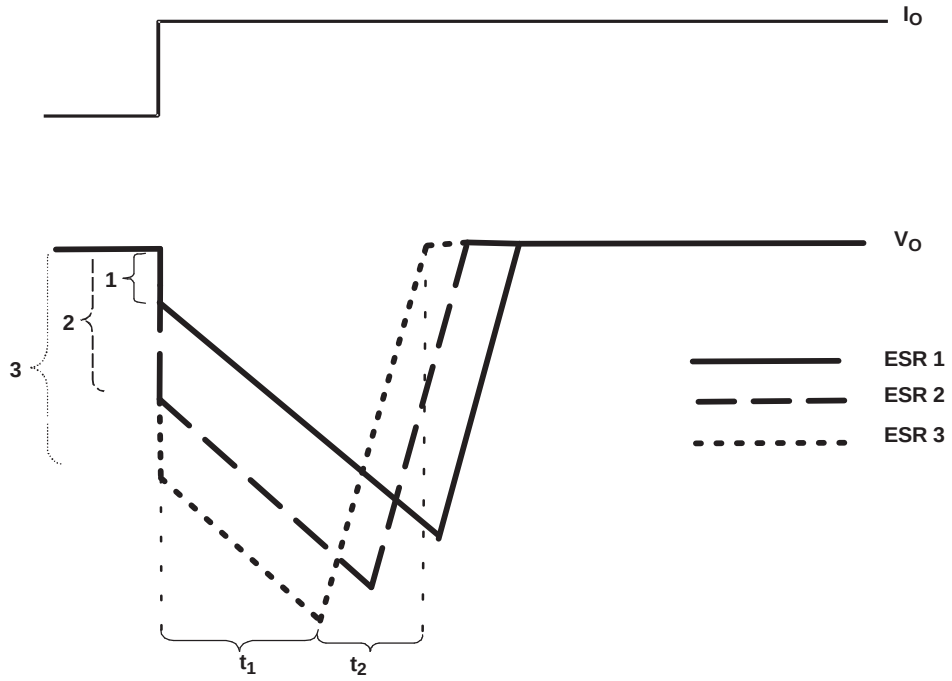


Figure 49. Correlation of Different ESRs and Their Influence on the Regulation of V_O at a Load Step from Low-to-High Output Current

Figure 49 also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the greater the voltage droop during the LDO response period.

Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

Programming the TPS70102 Adjustable LDO Converter

The output voltage of the TPS70102 adjustable regulators are programmed using external resistor dividers as shown in Figure 50.

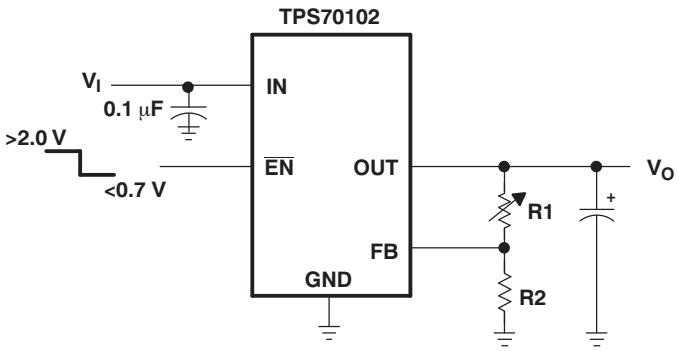
Resistors R1 and R2 should be chosen for approximately 50μA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 30.1kΩ to set the divider current at approximately 50μA, and then calculate R1 using Equation 1:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (1)$$

where:

- V_{REF} = 1.224V typ (the internal reference voltage)

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OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	31.6	30.1	kΩ
3.3 V	51.1	30.1	kΩ
3.6 V	59.0	30.1	kΩ

Figure 50. TPS70102 Adjustable LDO Regulator Programming

Regulator Protection

Both TPS701xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS701xx also features internal current limiting and thermal protection. During normal operation, the TPS701xx regulator 1 limits output current to approximately 1.6A (typ) and regulator 2 limits output current to approximately 750mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 2:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (2)$$

where:

- T_{Jmax} is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package; that is, 32.6°C/W for the 20-terminal PWP with no airflow
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 3:

$$P_D = (V_I - V_O) \times I_O \quad (3)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (December, 2009) to Revision I **Page**

- Replaced the *Dissipation Ratings* table with the *Thermal Information* table 4

Changes from Revision G (August, 2009) to Revision H **Page**

- Corrected typo in *output current limit* specification units 5
- Corrected typo in V_{OUT2} *UV comparator*, falling edge deglitch specification units 5

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS70102PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWP.B	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWPR.B	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70102PWPRG4	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70102
TPS70145PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70145
TPS70145PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70145
TPS70145PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70145
TPS70145PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70145
TPS70145PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70145
TPS70148PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70148
TPS70148PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70148
TPS70148PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70148
TPS70148PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70148
TPS70151PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70151
TPS70151PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70151
TPS70151PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70151
TPS70151PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70151
TPS70151PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70151
TPS70151PWPRG4	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70151
TPS70158PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70158
TPS70158PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70158
TPS70158PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70158
TPS70158PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70158
TPS70158PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT70158

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

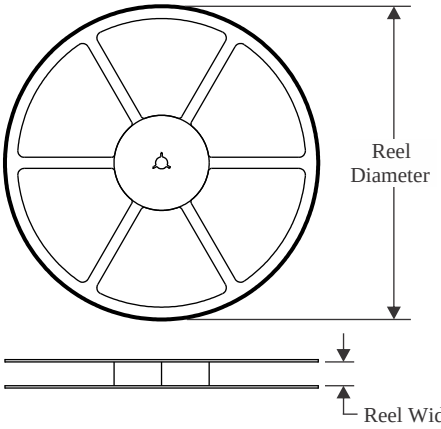
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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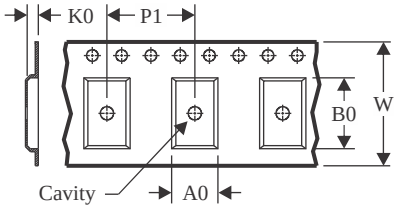
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

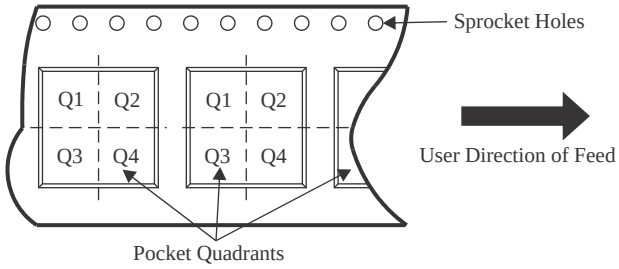


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

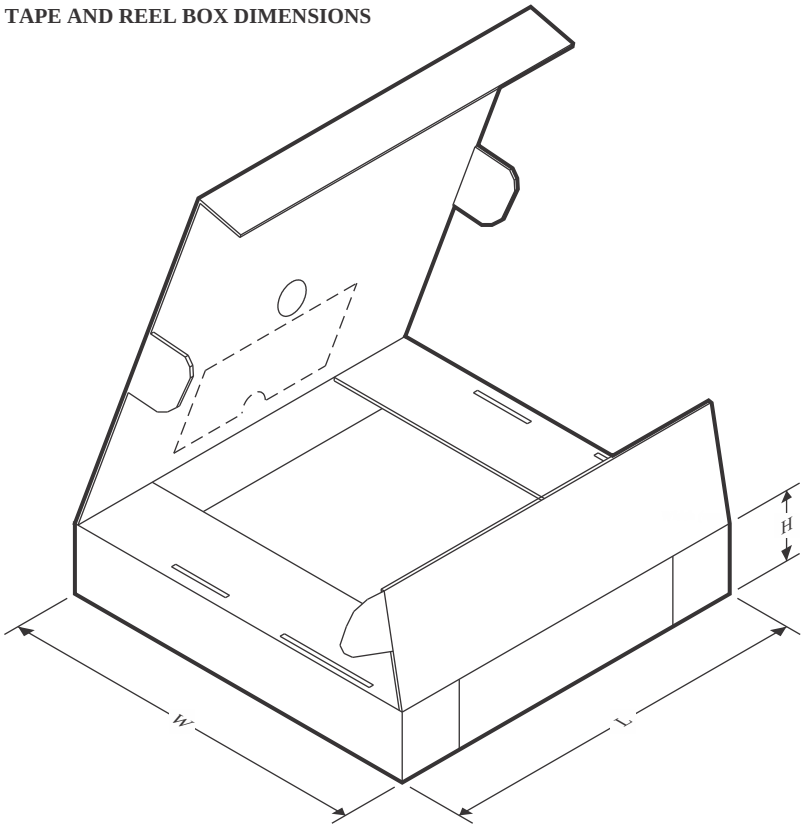
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70102PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS70145PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS70148PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS70151PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS70158PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

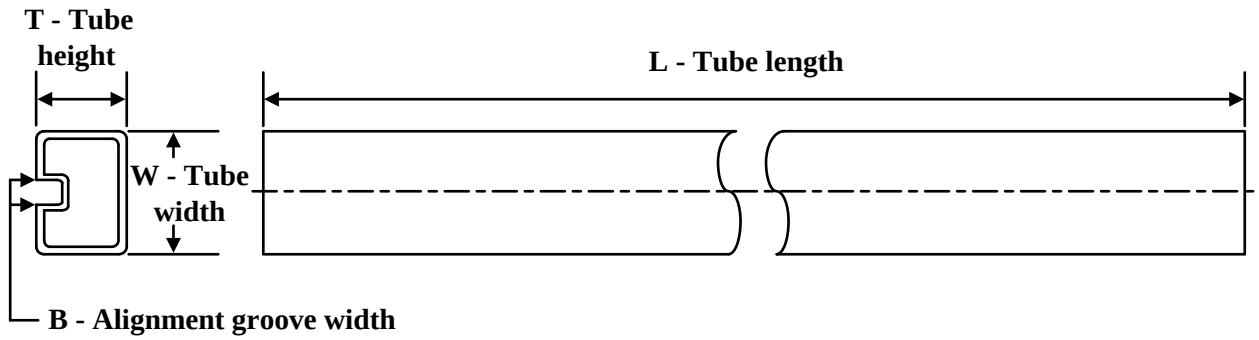
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70102PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS70145PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS70148PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS70151PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS70158PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS70102PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70102PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70102PWP.B	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70102PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70145PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70145PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70145PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70148PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70148PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70151PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70151PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70151PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70158PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70158PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS70158PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

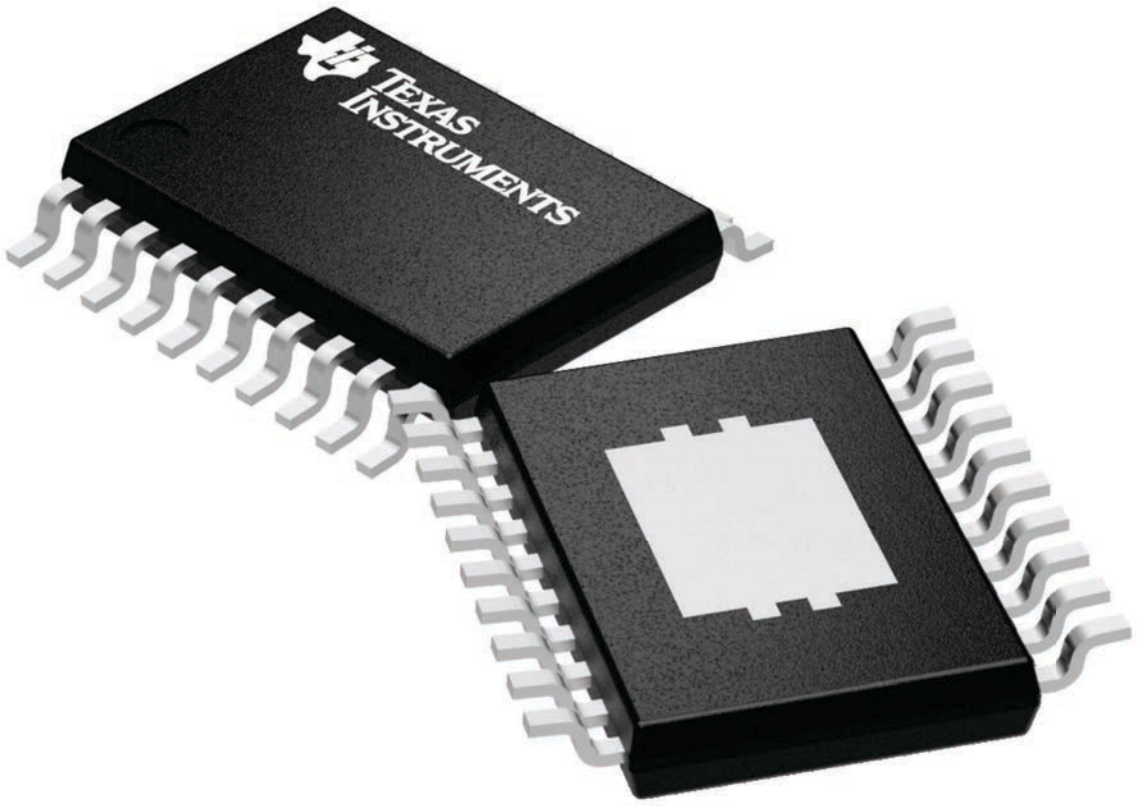
PWP 20

HTSSOP - 1.2 mm max height

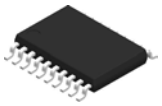
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

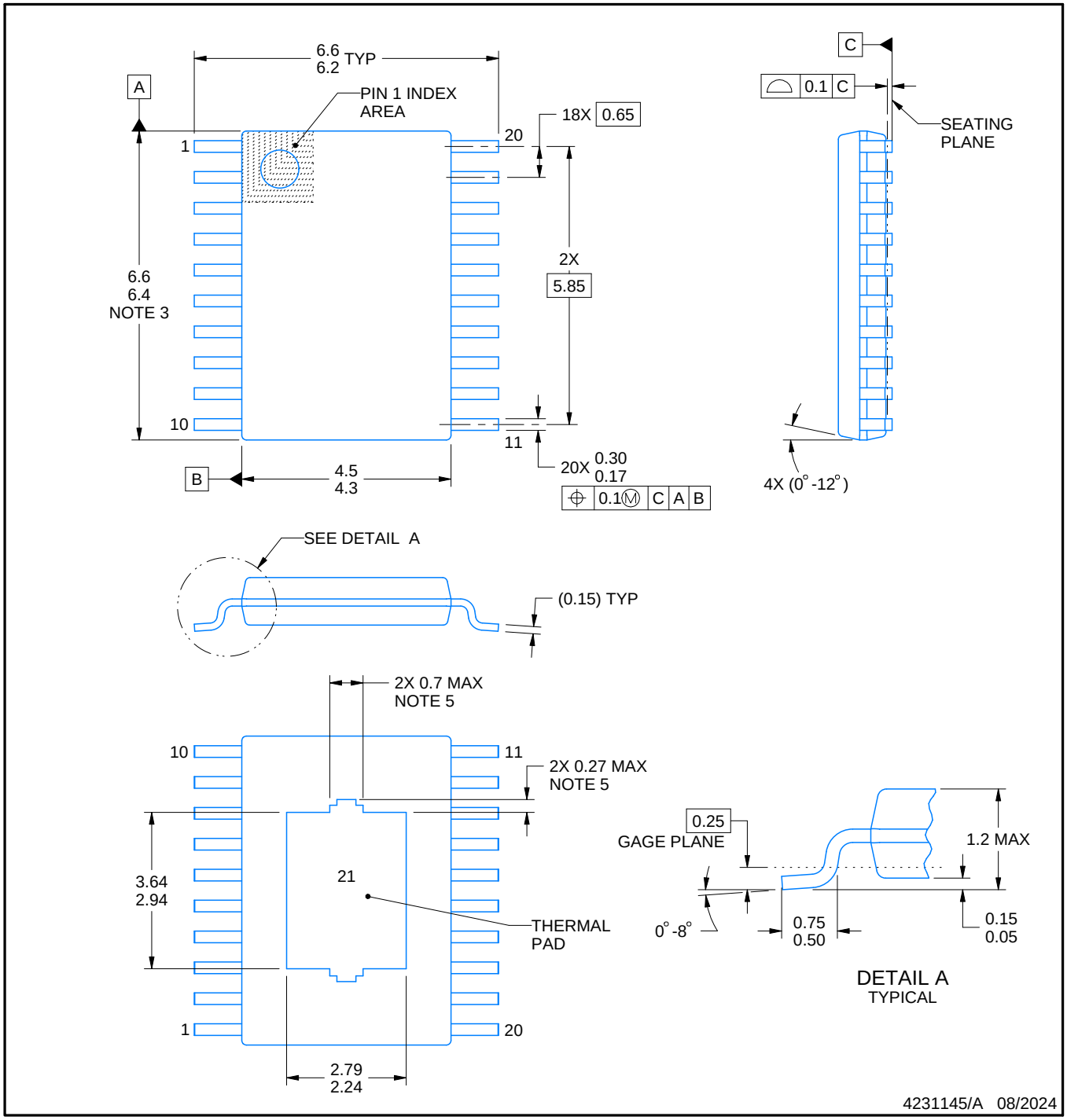


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

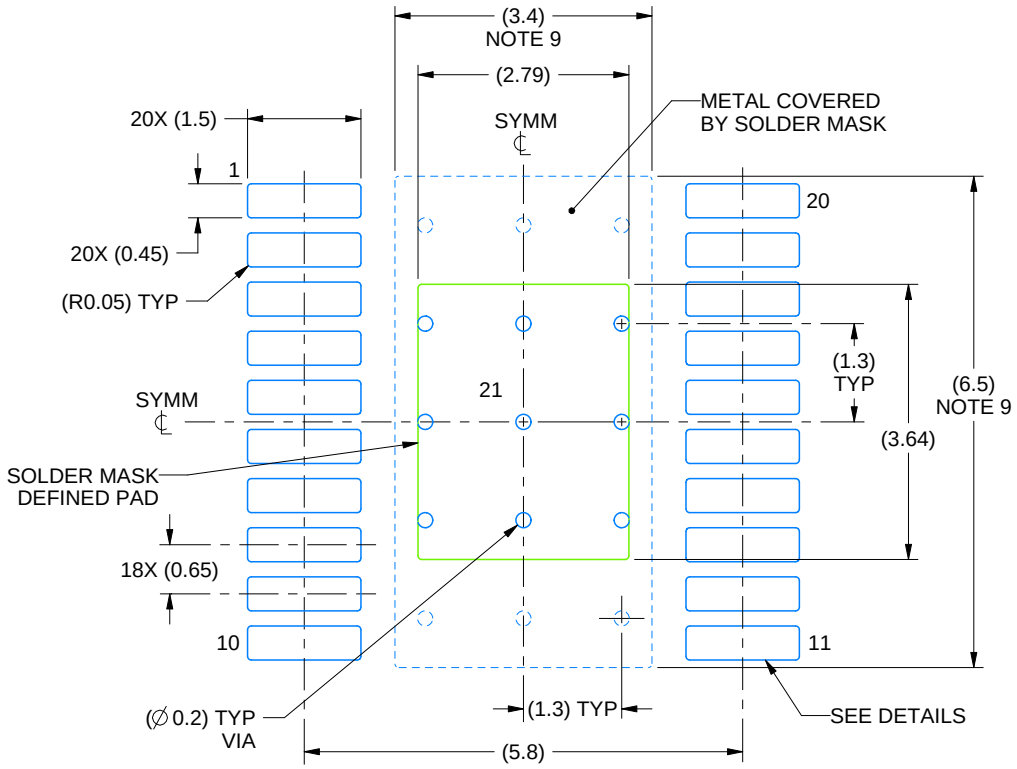
SMALL OUTLINE PACKAGE



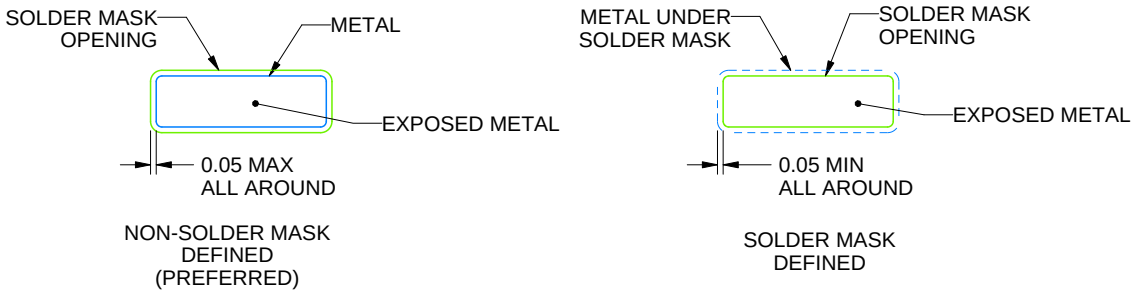
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

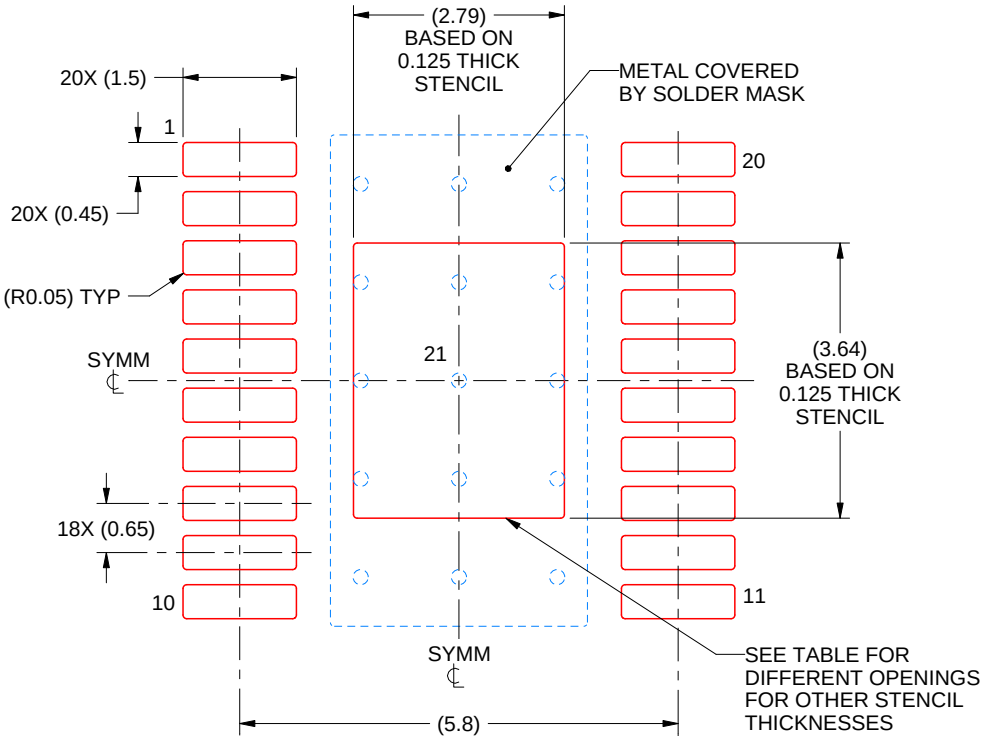


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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