TPS715 50-mA, 24-V, 3.2-µA Quiescent Current, Low-Dropout Linear Regulator

1 Features

- Input voltage range:
  - 2.5 V to 24 V (30 V max for new chip only)
- Available output voltage options:
  - Fixed: 1.8 V to 5 V
  - Adjustable: 1.205 V to 15 V
- Output current: Up to 50 mA
- Very low I_Q: 3.2 µA at 50-mA load current
- Stable with output capacitor ≥ 0.47 µF
- Overcurrent protection
- Package: 5-pin SC70 (DCK)
- Operating junction temperature: –40°C to +125°C
- For an 80-mA rated current and higher power package, see the TPS715A

2 Applications

- Home and building automation
- Retail automation and payment
- Grid infrastructure
- Medical applications
- Lighting applications

3 Description

The TPS715 low-dropout (LDO) linear voltage regulator is low quiescent current device that offers the benefits of a wide input voltage range and low-power operation in miniaturized packaging. Thus, the TPS715 is designed for battery-powered applications and as a power-management attachment to low-power microcontrollers.

The TPS715 is available in both fixed and adjustable versions. For more flexibility or higher output voltages, the adjustable version uses feedback resistors to set the output voltage from 1.205 V to 15 V. The TPS715 LDOs support a low dropout of typically 415 mV at 50 mA of load current. The low quiescent current (3.2 µA typically) is stable over the entire range of output load current (0 mA to 50 mA). The TPS715 also features an internal soft-start to lower the inrush current. The built-in overcurrent limit helps protect the regulator in the event of a load short or fault.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS715	DCK (SC70, 5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

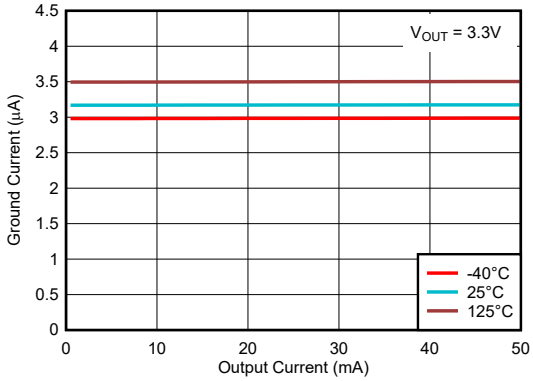
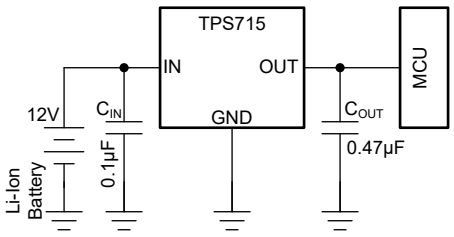


Figure 3-1. Quiescent Current vs Load Current for TPS715xx (New Chip Only)



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (August 2022) to Revision T (December 2022)	Page
• Added information for M3 devices (new chip information) to document	1
• Changed *Features* section: changed adjustable output voltage options, changed *Specified junction temperature* to *Operating junction temperature*, and reordered *Features* bullets	1
• Added *Quiescent Current vs Load Current* curve to front page	1
• Deleted low power level discussion from *Description* section	1
• Changed *Typical Application Schematic* figure	1
• Changed *Pin Functions* table: changed *Description* column and added footnote	4
• Added condition statement and characterization conditions plots to *Typical Characteristics* section	8
• Changed curve titles in *Typical Characteristics* section to distinguish between new and legacy chips	8
• Changed block diagrams in *Functional Block Diagrams* section	11
• Changed *Low Quiescent Current* section and title	12
• Deleted thermal shutdown discussion from *Current Limit* section	12
• Changed third bullet in *Normal Operation* section	13
• Changed *Application Information* section	14
• Changed *Typical Application* section	14
• Changed output operating voltage range from *1.2 V to 15 V* to *1.205 V to 15 V* in *Setting VOUT for the TPS71501 Adjustable LDO*	14
• Added reverse current limit discussion to *Reverse Current* section	15
• Changed *Application Curves* section	18
• Deleted sentence stating *This input supply must be well regulated* from *Power Supply Recommendations* section	19
• Changed *Example Layout for the TPS71501DCK* figure	20
• Changed *Device Nomenclature* table	21

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Changes from Revision R (February 2015) to Revision S (August 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Changed document title....1
- Changed *Features* section....1
- Changed *Applications* section....1
- Changed *Description* section....1
- Changed descriptions of FB and NC pins in *Pin Functions* table, split fixed and adjustable pin outs apart....4
- Added new chip specific plots to *Typical Characteristics* section....8
- Changed *Overview* section....11
- Changed block diagrams in *Functional Block Diagrams* section....11
- Changed *Low Quiescent Current* section and title....12
- Changed *Dropout Voltage (V_{DO})* section....12
- Deleted *Disabled* row from *Device Functional Mode Comparison* table....13
- Changed *Dropout Operation* section....13
- Changed *External Capacitor Requirements* section....15
- Added *Input and Output Capacitor Requirements* section....15
- Changed *Reverse Current* section....15
- Changed output voltage value when no C_{FF} is used from *0.8 V* to *1.205 V*....16
- Added *Power Dissipation (P_D)* section....16
- Added new chip specific plots to *Application Curves* section....18
- Added second row and deleted second footnote from *Device Nomenclature* table....21

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5 Pin Configuration and Functions

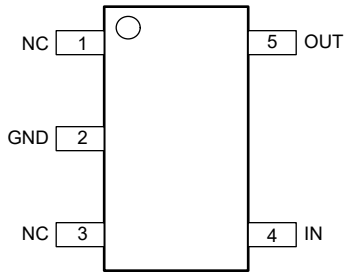


Figure 5-1. DCK Package (Fixed), 5-Pin SC70 (Top View)

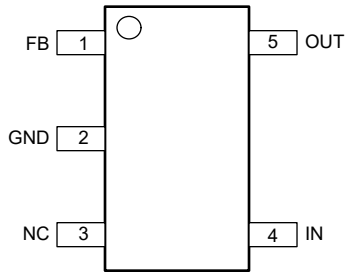


Figure 5-2. DCK Package (Adjustable), 5-Pin SC70 (Top View)

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	FIXED	ADJUSTABLE		
FB	—	1	I	In the adjustable configuration, this pin sets the output voltage with the help of the feedback divider.
GND	2	2	—	Ground pin.
IN	4	4	I	Input supply pin. A capacitor with a value of 0.1 µF or larger is recommended from this pin to ground. See the *Input and Output Capacitor Requirements* section for more information.
NC	1, 3	3	—	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.
OUT	5	5	O	Output of the regulator. A capacitor with a value of 1 µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Requirements* section for more information.

(1) The nominal output capacitance must be greater than 0.47 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47 µF.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Voltage	V_{IN} (for legacy chip only)	–0.3	24	V
	V_{IN} (for new chip only)	–0.3	30	
	V_{OUT} (for legacy chip only)	–0.3	16.5	
	V_{OUT} (for fixed output new chip only)	–0.3	2 X $V_{OUT(typ)}$ or V_{IN} + 0.3V or 5.5V (whichever is lower)	
Voltage	V_{OUT} (for adjustable output new chip only)	–0.3	V_{IN} + 0.3	V
	V_{FB} (for adjustable output new chip only)		2.4	
	V_{FB} (for adjustable output legacy chip only)	–0.3	4.5	
Current	Peak output current	Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
V_{OUT}	Output voltage	1.205		15	
I_{OUT}	Output current	0		50	mA
C_{IN}	Input capacitor(2)	0	0.047		μF
C_{OUT}	Output capacitor (for legacy chip only)	0.47	1		
	Output capacitor (for new chip only) (3)	1			
T_J	Operating junction temperature	-40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.047 μF is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 0.47 μF minimum for the stability.

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Thermal Information

THERMAL METRIC (1)		Legacy Chip DCK (SC-70) 5 PINS	New Chip DCK (SC-70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.8	195.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	88.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.6	40.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	11.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.9	40.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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6.4 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage (1)	I_O = 10 mA	2.5		24	V
		I_O = 50 mA	3		24	
V_{OUT}	Output voltage range (TPS71501)		1.205		15	V
	Output voltage accuracy (1) (2)	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, 100 µA ≤ I_{OUT} ≤ 50 mA	–4		4	%
I_{GND}	Ground pin current (legacy chip)(3)	0 ≤ I_{OUT} ≤ 50 mA , T_J = –40°C to 85°C		3.2	4.2	µA
		0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.8	
		0 mA ≤ I_{OUT} ≤ 50 mA , V_{IN} = 24 V			5.8	
	Ground pin current (new chip) (3)	0 ≤ I_{OUT} ≤ 50 mA , T_J = –40°C to 85°C		3.2	4.1	
		0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.3	
		0 mA ≤ I_{OUT} ≤ 50 mA , V_{IN} = 24 V			4.5	
$\Delta V_{OUT\ (\Delta IOUT)}$	Load regulation	I_{OUT} = 100 µA to 50 mA		22		mV
$\Delta V_{OUT\ (\Delta VIN)}$	Output voltage line regulation (legacy chip) (1)	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V		20	60	mV
	Output voltage line regulation (new chip) (1)	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V		20	22	
V_n	Output noise voltage (legacy chip) (4)	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
	Output noise voltage (new chip)(4)	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		425		
I_{CL}	Output current limit (legacy chip)	V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		750	mA
		V_{OUT} = 0 V, V_{IN} < 3.5 V	90		750	
	Output current limit (new chip)	V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		350	
		V_{OUT} = 0 V, V_{IN} < 3.5 V	90		350	
PSRR	Power-supply ripple rejection	f = 100 kHz, C_{OUT} = 10 µF		60		dB
V_{DO}	Dropout voltage (legacy chip)	I_{OUT} = 50 mA, V_{IN} = $V_{OUT(nom)}$ – 0.1 V		415	750	mV
	Dropout voltage (new chip)			415	525	

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) For adjustable device, output accuracy excludes the tolerance and mismatch associated with external resistors used for setting up the output voltage level.
(3) This device employs a leakage null control circuit. This circuit is active only if output current is less than pass FET leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.
(4) See Device Nomenclature for details about new and legacy chip descriptions

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6.5 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

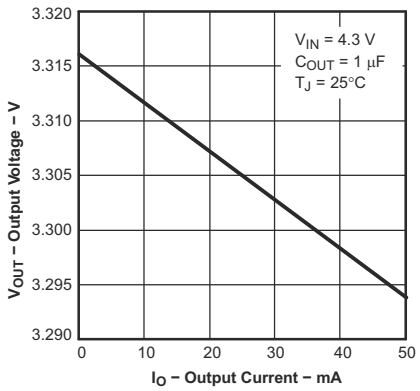


Figure 6-1. Output Voltage vs Output Current for Legacy Chip

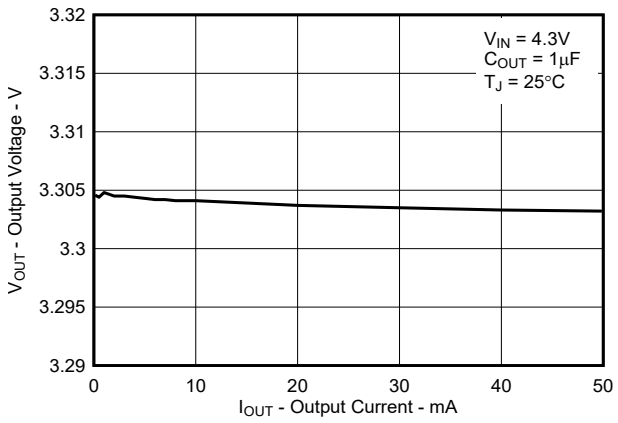


Figure 6-2. Output Voltage vs Output Current for New Chip

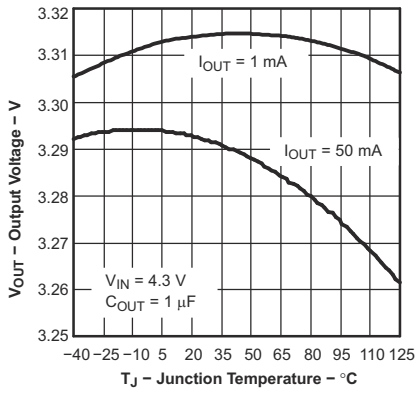


Figure 6-3. Output Voltage vs Junction Temperature for Legacy Chip

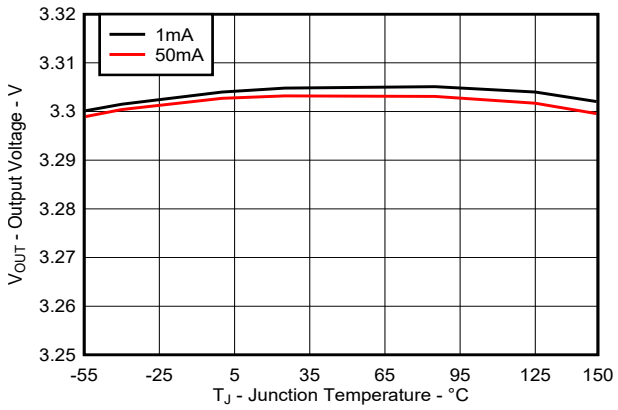


Figure 6-4. Output Voltage vs Junction Temperature for New Chip

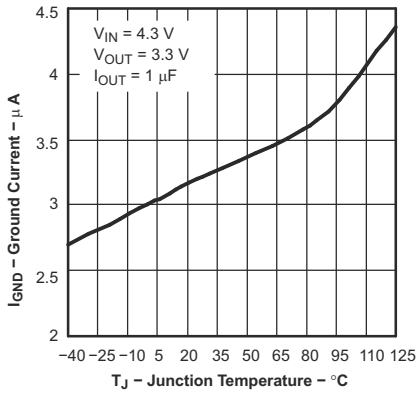


Figure 6-5. Quiescent Current vs Junction Temperature for Legacy Chip

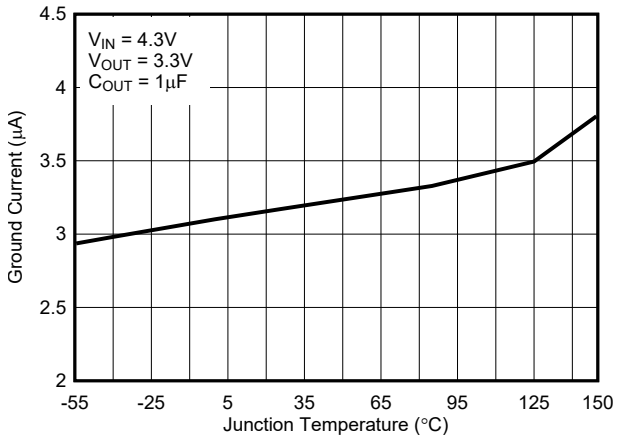


Figure 6-6. Quiescent Current vs Junction Temperature for New Chip

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6.5 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

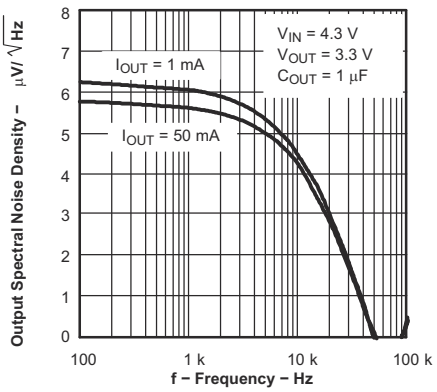
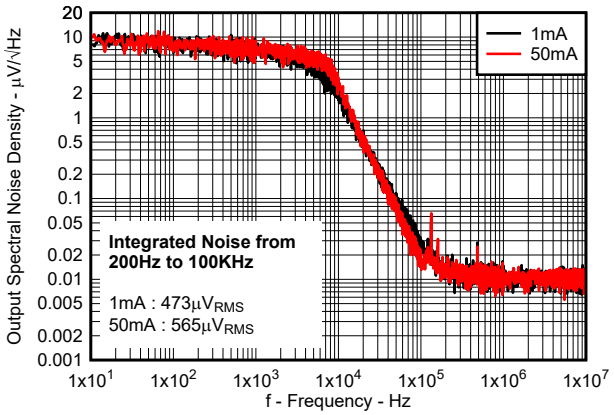


Figure 6-7. Output Voltage Spectral Noise Density vs Frequency for Legacy Chip



Integrated noise vs I_{LOAD}, V_{IN} = 4.3V, V_{OUT} = 3.3V ,

Figure 6-8. Output Voltage Spectral Noise Density vs Frequency for New Chip

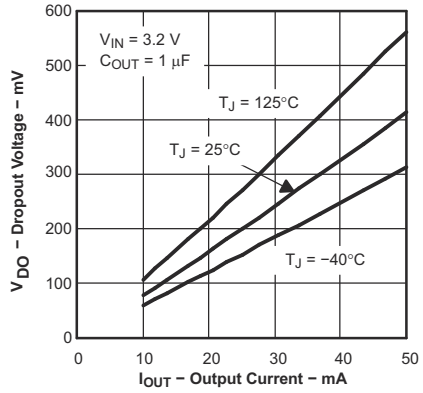


Figure 6-9. Dropout Voltage vs Output Current for Legacy Chip

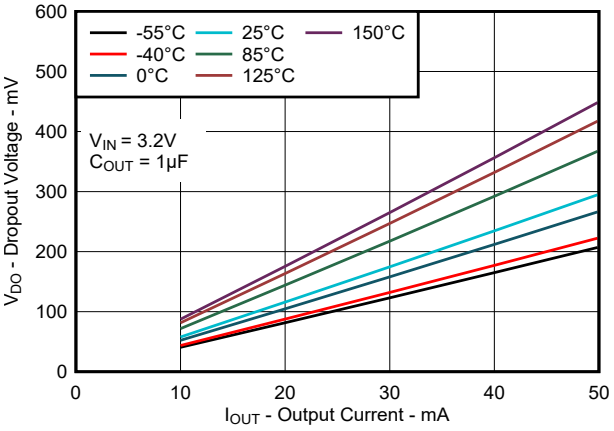


Figure 6-10. Dropout Voltage vs Output Current for New Chip

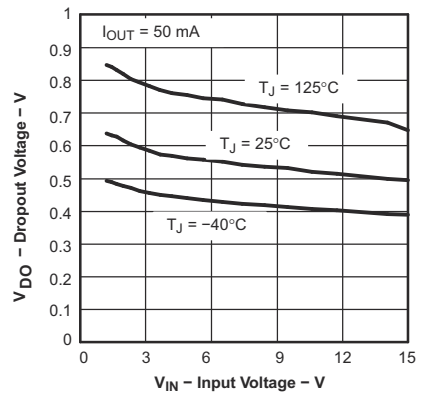


Figure 6-11. TPS71501 Dropout Voltage vs Input Voltage for Legacy Chip

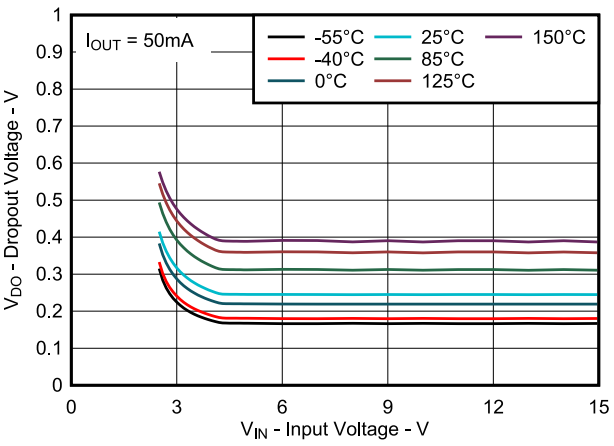


Figure 6-12. TPS71501 Dropout Voltage vs Input Voltage for New Chip

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6.5 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

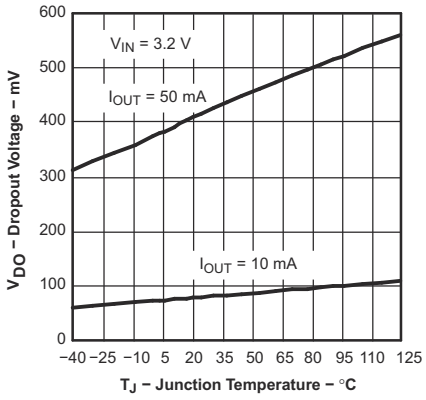


Figure 6-13. Dropout Voltage vs Junction Temperature for Legacy Chip

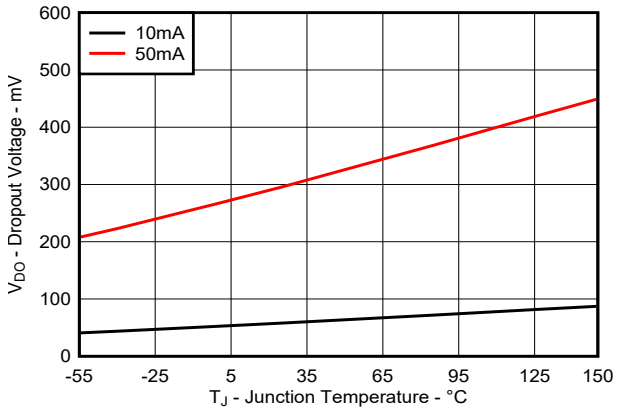


Figure 6-14. Dropout Voltage vs Junction Temperature for New Chip

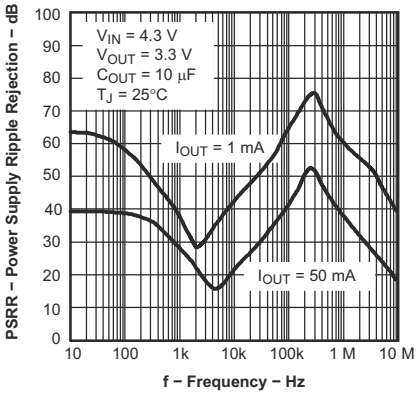


Figure 6-15. Power-Supply Ripple Rejection vs Frequency for Legacy Chip

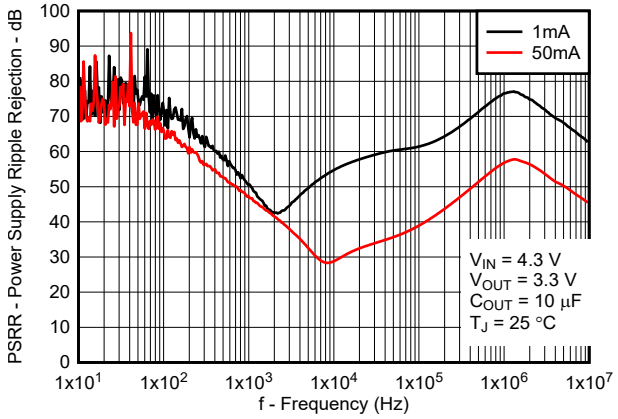


Figure 6-16. Power-Supply Ripple Rejection vs Frequency for New Chip

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7 Detailed Description

7.1 Overview

The TPS715 low-dropout regulator (LDO) consumes only 3.2 µA (typ) of quiescent current across the entire output current range, while offering a wide input voltage range and low-dropout voltage in small packaging. The device, which operates over an input range of 2.5 V to 24 V, is stable with any output capacitor greater than or equal to 0.47 µF. The low quiescent current across the complete load current range makes the TPS715 optimal for powering battery-operated applications. The TPS715 has internal soft-start to control inrush current into the output capacitor. This LDO also has overcurrent protection during a load-short or fault condition on the output.

7.2 Functional Block Diagrams

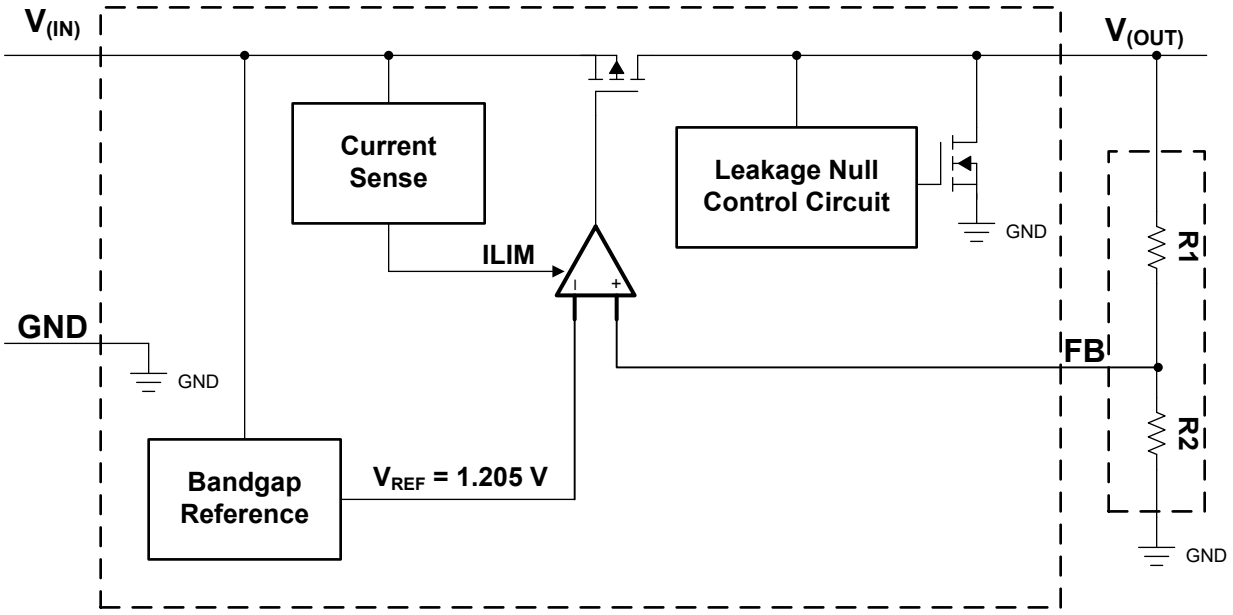


Figure 7-1. Functional Block Diagram—Adjustable Version

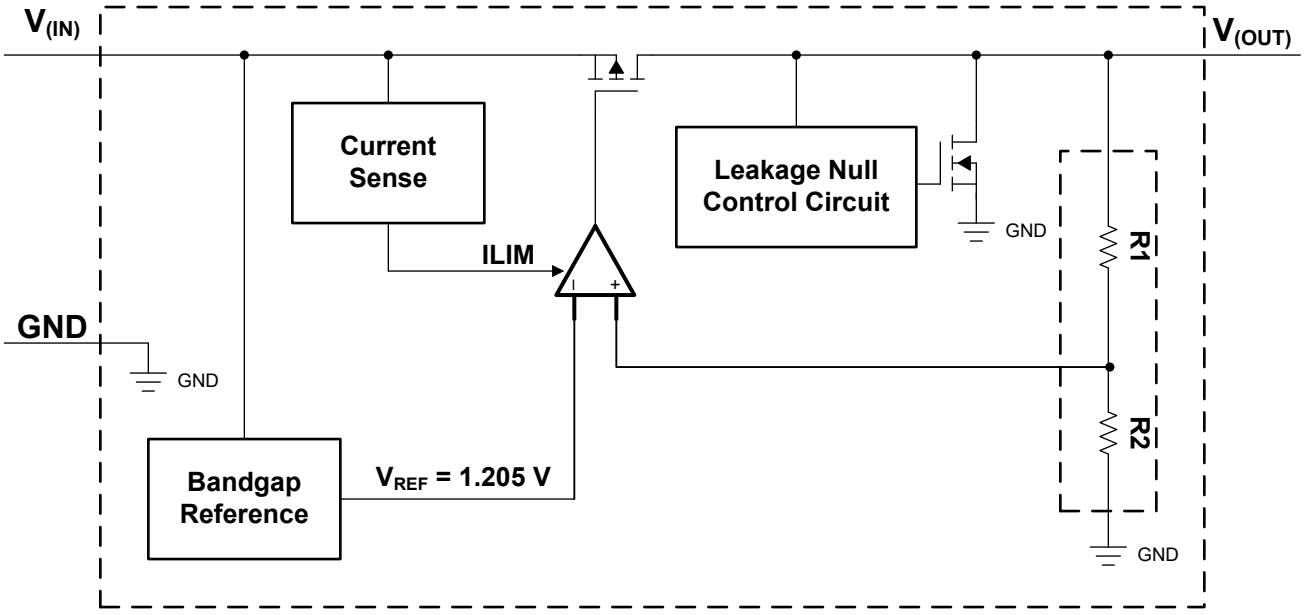


Figure 7-2. Functional Block Diagram—Fixed Version

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7.3 Feature Description

7.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is designed for applications that have either large transients or high DC voltage supplies.

7.3.2 Low Quiescent Current

This device only requires 3.2 µA (typical) of quiescent current across the complete load current range (0 mA to 50 mA) from –40°C to +125°C.

7.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN} – V_{OUT}$) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note.

Figure 7-3 shows a diagram of the current limit.

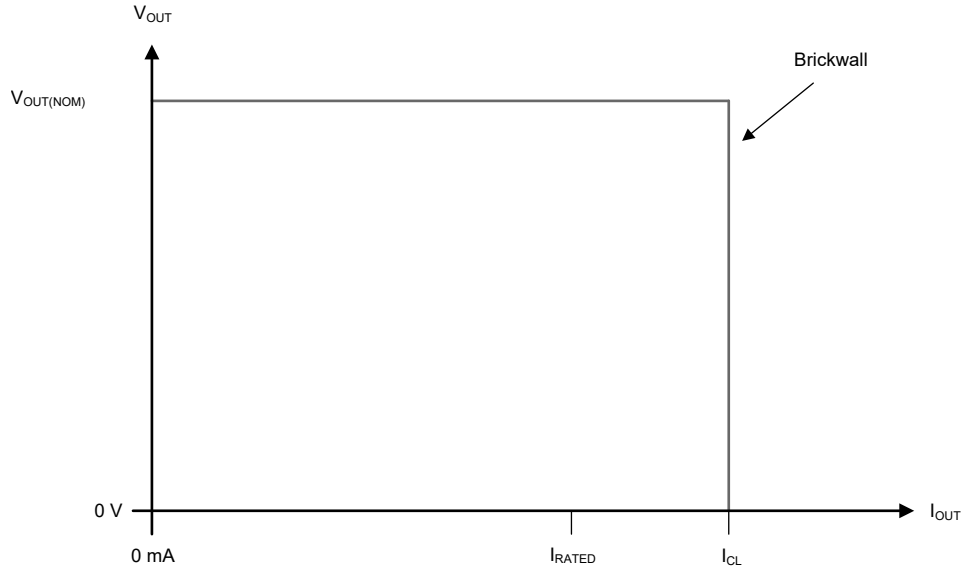


Figure 7-3. Current Limit

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7.4 Device Functional Modes

Table 7-1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS715 family of LDO regulators is designed for battery-powered applications and is a good supply for low-power microcontrollers (such as the MSP430) because of the device family low I_Q performance across load current range. The ultra-low-supply current of the TPS715 device maximizes efficiency at light loads, and the high input voltage range and flexibility of output voltage selection in the adjustable configuration and fixed output levels makes the device an optimal supply for building automation and power tools.

8.2 Typical Application

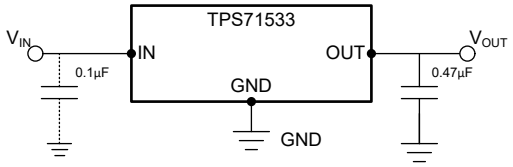
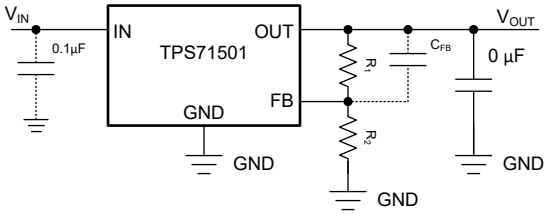


Figure 8-1. Typical Application Circuit (Fixed-Voltage Version)



Output Voltage	R1	R2
1.8V	0.499 MΩ	1MΩ
2.8V	1.33 MΩ	1MΩ
5.0V	3.16 MΩ	1MΩ

Figure 8-2. TPS71501 Adjustable LDO Regulator Programming

8.2.1 Detailed Design Procedure

8.2.1.1 Setting V_{OUT} for the TPS71501 Adjustable LDO

The TPS715 family contains an adjustable version, the TPS71501, which sets the output voltage using an external resistor divider as shown in Figure 8-2. The output voltage operating range is 1.205 V to 15 V, and is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where:

- V_{REF} = 1.205 V (typical)

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Choose resistors R1 and R2 allows approximately 1.5 µA of current through the resistor divider. Lower value resistors can be used for improved noise performance, but consume more power. Avoid higher resistor values because leakage current into or out of FB across R1 / R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 3:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (3)$$

Figure 8-2 depicts this configuration.

8.2.1.2 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.2.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.2.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN}$ + 0.3 V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

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Figure 8-3 shows one approach for protecting the device.

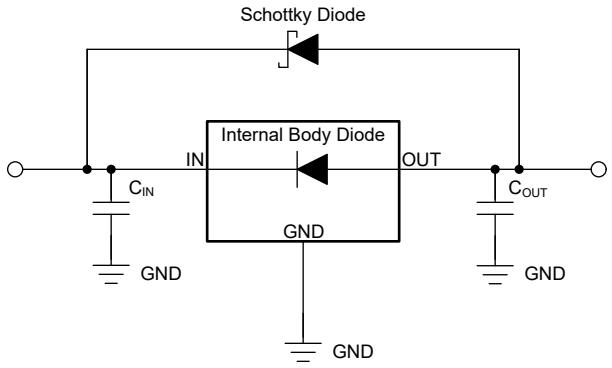


Figure 8-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.2.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 µA. Equation 6 calculates the feedback divider current.

$$I_{FB_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 1.205 V with the FB pin tied to the OUT pin, no C_{FF} is used.

8.2.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

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The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.2.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2.2 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

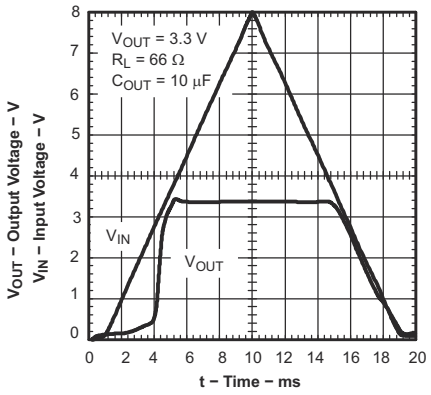


Figure 8-4. Power-Up and Power-Down for Legacy Chip

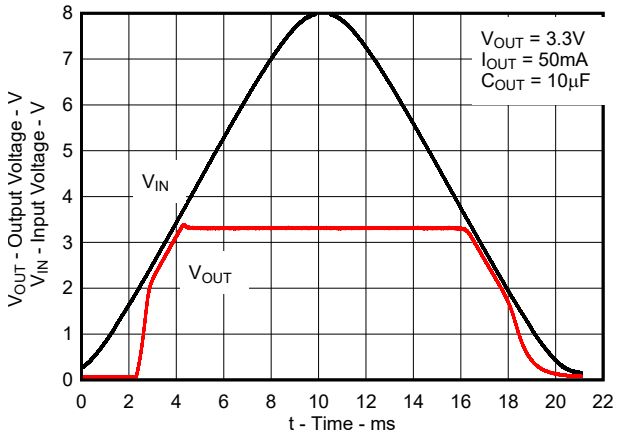


Figure 8-5. Power-Up and Power-Down for New Chip

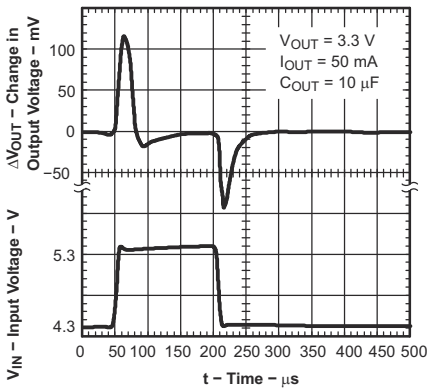


Figure 8-6. Line Transient Response for Legacy Chip

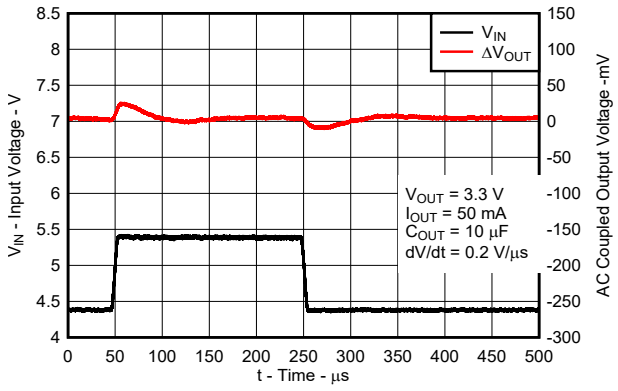


Figure 8-7. Line Transient Response for New Chip

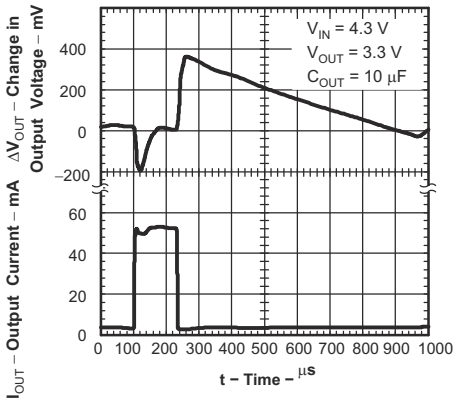


Figure 8-8. Load Transient Response for Legacy Chip

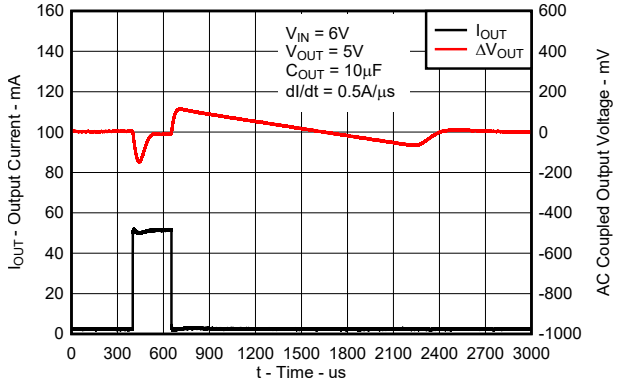


Figure 8-9. Load Transient Response for New Chip

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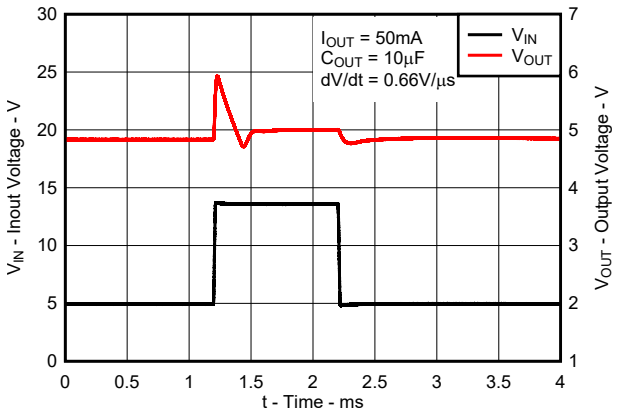


Figure 8-10. Dropout Exit Transient Response for New Chip

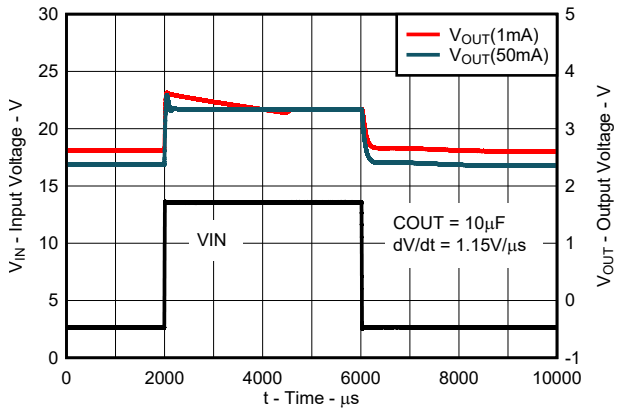


Figure 8-11. Fast Line Transient Response for New Chip

8.3 Best Design Practices

Place at least one 0.47-µF capacitor as close as possible to the OUT and GND terminals of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor as close as possible to the IN and GND terminals of the regulator for best performance.

Do not exceed the absolute maximum ratings.

8.4 Power Supply Recommendations

The TPS715 is designed to operate from an input voltage supply range between 2.5 V and 24 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

8.5 Layout

8.5.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because this practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage and shield the LDO from noise.

8.5.1.1 Power Dissipation

To ensure reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

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The maximum-power-dissipation limit is determined using Equation 11:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \tag{11}$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 12:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{12}$$

For a higher power package version of the TPS715, see the TPS715A.

8.5.2 Layout Example

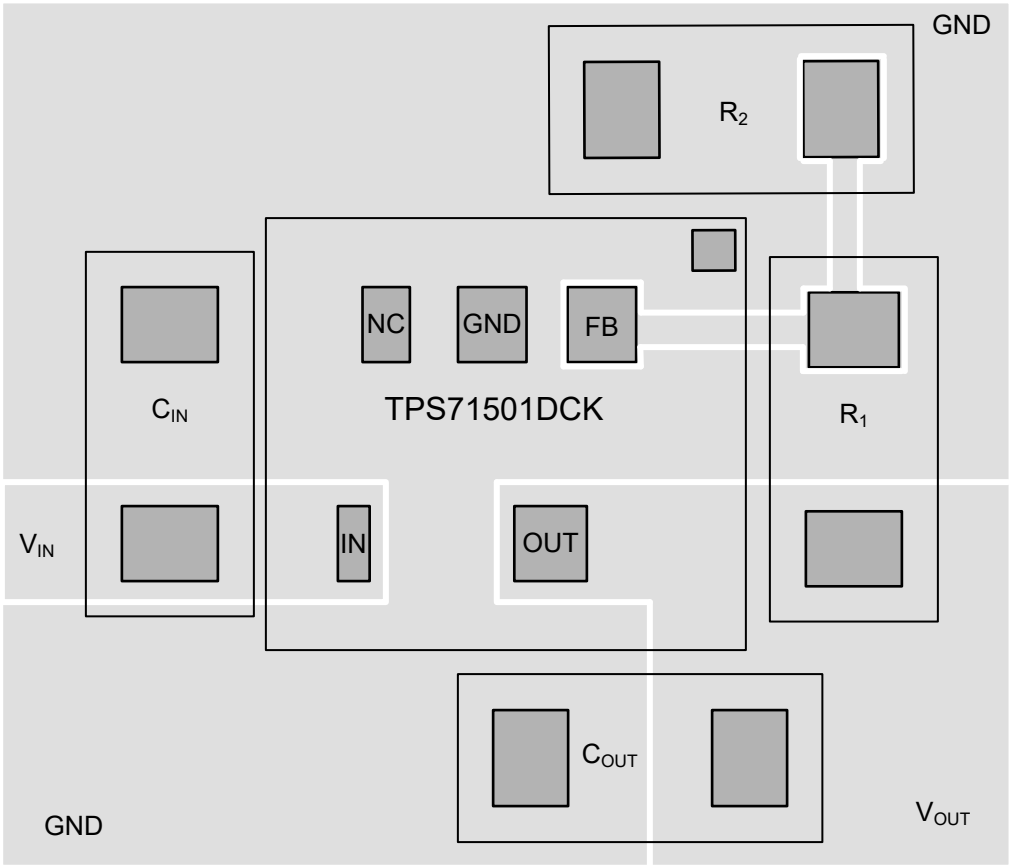


Figure 8-12. Example Layout for the TPS71501DCK

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715. The TPS71533EVM evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715 is available through the product folders under *Tools & Software*.

9.1.2 Device Nomenclature

Table 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS715**xxyyyz** Legacy chip	**xx** is the nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **yyy** is the package designator. **z** is the package quantity.
TPS715**xxyyyz M3** New chip	**xx** is the nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS715A 24-V High Input Voltage, Micropower, 80-mA LDO Voltage Regulator* data sheet
- Texas Instruments, *TPS71533EVM LDO Evaluation Module* user guide
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *Know Your Limits* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71501DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARB
TPS71501DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARB
TPS71501DCKR1G4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	ARB
TPS71501DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	ARB
TPS71501DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARB
TPS71501DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARB
TPS71518DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ARD
TPS71518DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARD
TPS71518DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARD
TPS71518DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARD
TPS71518DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ARD
TPS71519DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BOX
TPS71519DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BOX
TPS71523DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BNX
TPS71523DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNX
TPS71523DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNX
TPS71523DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNX
TPS71523DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNX
TPS71523DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNX
TPS71525DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQL
TPS71525DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQL
TPS71525DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQL
TPS71525DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQL
TPS71525DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQL
TPS71530DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQM
TPS71530DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQM
TPS71530DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQM
TPS71530DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQM
TPS71530DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71533DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQI
TPS71533DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQI
TPS71533DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQI
TPS71533DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQI
TPS71533DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AQI
TPS715345DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BNY
TPS715345DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNY
TPS715345DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNY
TPS715345DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNY
TPS715345DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNY
TPS715345DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BNY
TPS71550DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T48
TPS71550DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T48
TPS71550DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T48
TPS71550DCKRM3	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T48
TPS71550DCKRM3.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T48

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS715 :

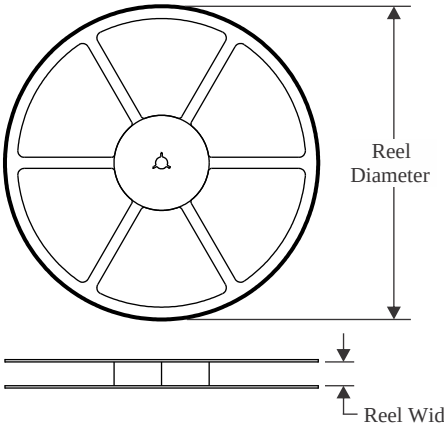
- Automotive : TPS715-Q1

NOTE: Qualified Version Definitions:

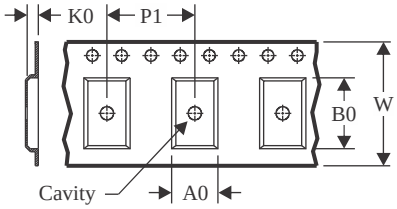
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

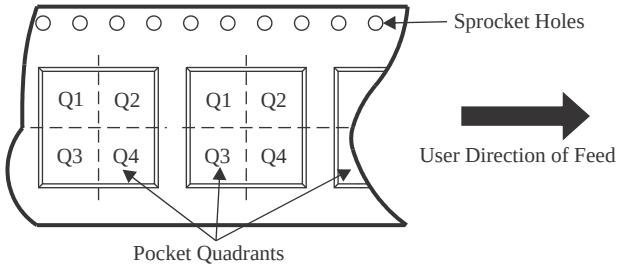


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

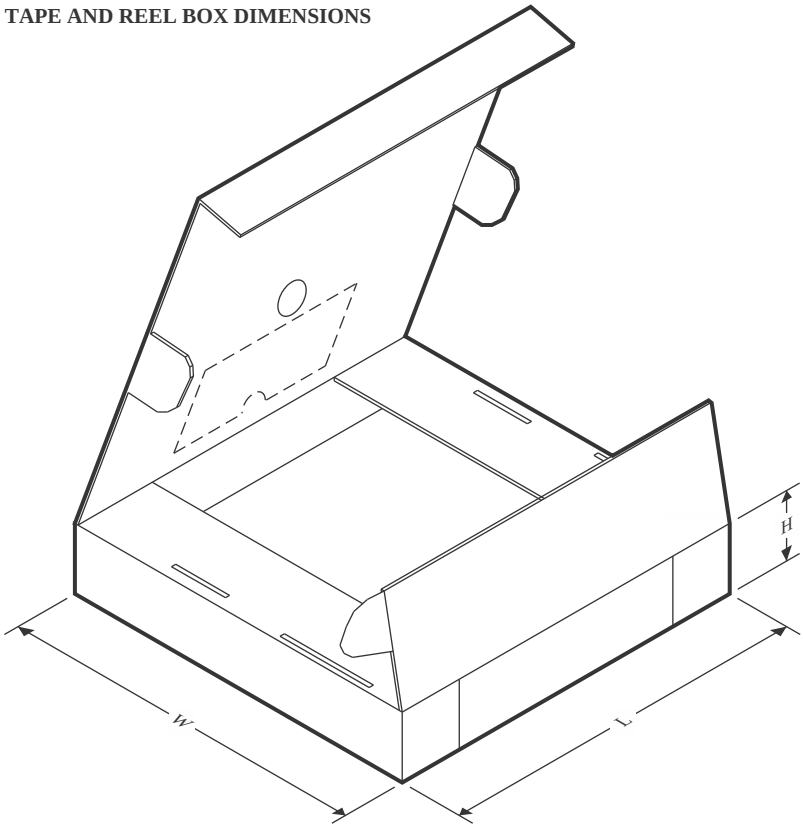


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71501DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71501DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71518DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71518DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71518DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71519DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS71523DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71523DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71523DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71525DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71525DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71530DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71530DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71533DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71533DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS715345DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS715345DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS715345DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS715345DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71550DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71550DCKRM3	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71501DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71501DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71518DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71518DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71518DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71519DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS71523DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71523DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71523DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71525DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71525DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71530DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71530DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71533DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71533DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS715345DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS715345DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS715345DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0

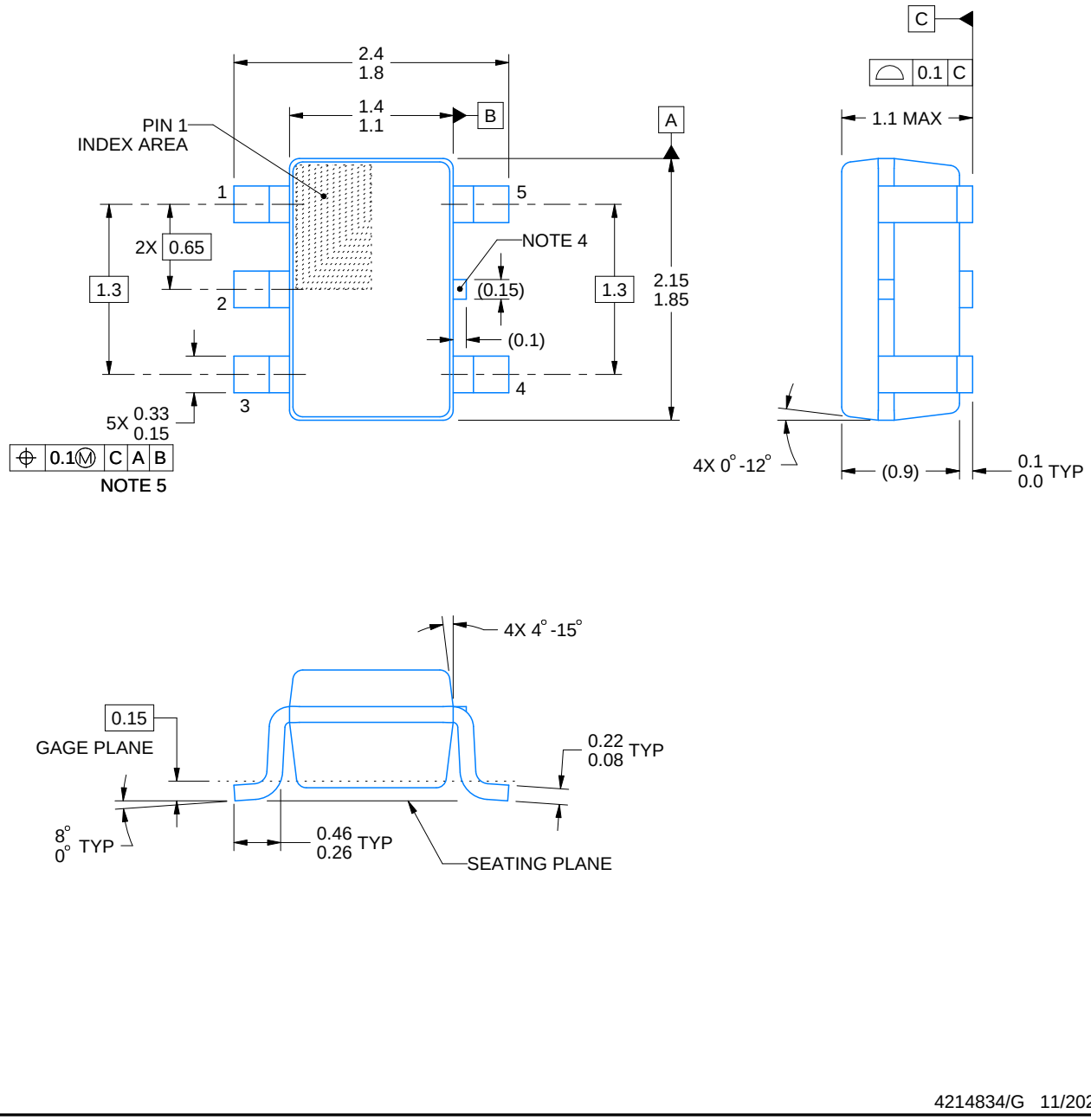
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS715345DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71550DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71550DCKRM3	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

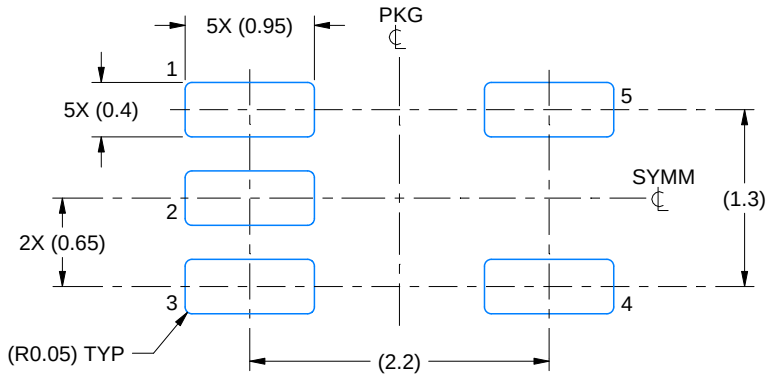
SMALL OUTLINE TRANSISTOR



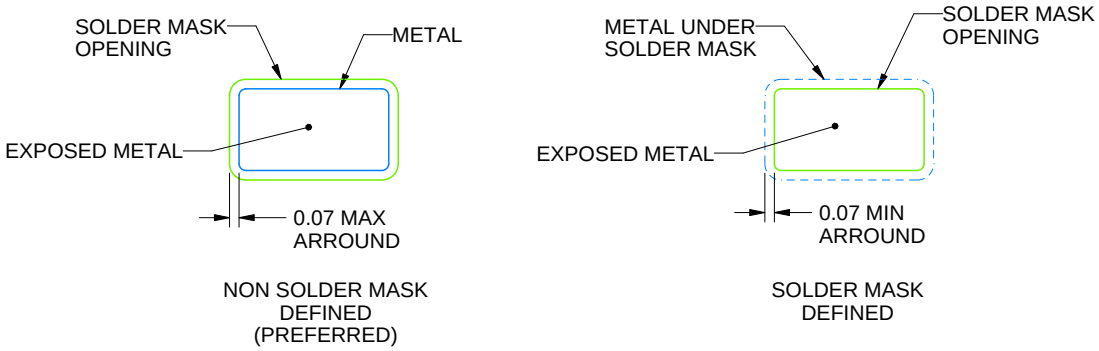
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

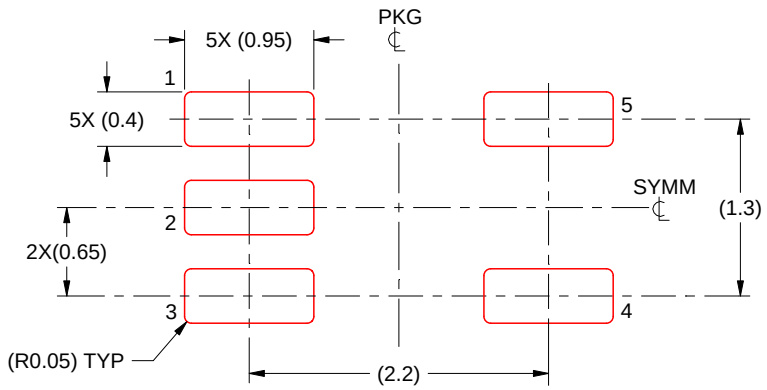


SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025

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