TPS717-Q1
Low-Noise, High-Bandwidth PSRR, Low-Dropout, 150-mA Linear Regulator

1 Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device HBM ESD Classification Level C4B
- Input Voltage: 2.5 V to 6.5 V
- Available in Multiple Output Versions:
  - Fixed Output with Voltages from 0.9 V to 5 V
  - Adjustable Output Voltage from 0.9 V to 6.2 V
- Ultra-High PSRR:
  - 70 dB at 1 kHz, 67 dB at 100 kHz, and 45 dB at 1 MHz
- Excellent Load and Line Transient Response
- Very Low Dropout: 170 mV typical at 150 mA
- Low Noise: 30 μV_{RMS} typical (100 Hz to 100 kHz)
- Small 5-pin SOT, 2-mm × 2-mm WSON-6, and 1.5-mm × 1.5-mm WSON-6 Packages

2 Applications

- PLLs
- VCOs
- Camera Sensor Power
- Microcontroller Power
- Wireless LAN, Bluetooth®
- ADAS and Infotainment Systems

3 Description

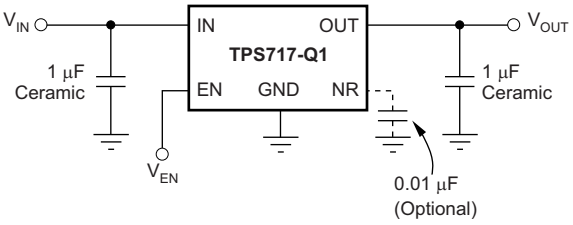
The TPS717-Q1 family of low-dropout (LDO), low-power linear regulators offers very high power-supply rejection (PSRR) and maintains very low 45-µA ground current in an ultra-small, five-pin SOT package. The family uses an advanced BiCMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717-Q1 is stable with a 1-µF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. The device family is fully specified from T_J, T_A = –40°C to 125°C and is offered in a small SOT (SC70-5) package, a 2-mm × 2-mm WSON-6 package with a thermal pad, and a 1.5-mm × 1.5-mm WSON-6 package, which are ideal for small form-factor portable equipment (such as wireless handsets and PDAs). The TPS717-Q1 family of LDOs is qualified for AEC-Q100 grade 1.

Device Information(1)

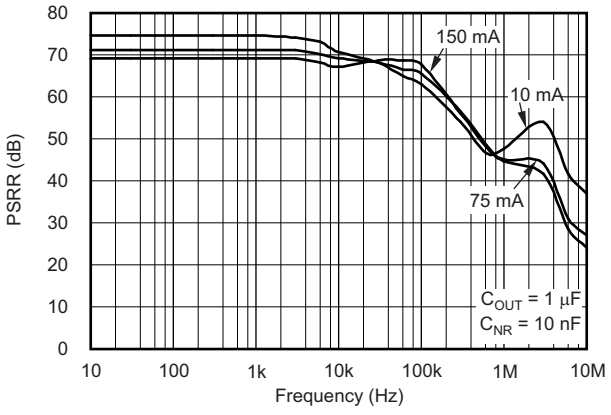
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS717-Q1	SOT (5)	2.00 mm × 1.25 mm
	WSON (6)	2.00 mm × 2.00 mm
	WSON (6)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit for Fixed-Voltage Versions



PSRR vs Frequency



Power-Supply Rejection Ratio (V_{IN} – V_{OUT} = 1 V)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Revision History 2
5 Pin Configuration and Functions 4
6 Specifications 5
6.1 Absolute Maximum Ratings 5
6.2 ESD Ratings 5
6.3 Recommended Operating Conditions 6
6.4 Thermal Information 6
6.5 Electrical Characteristics 7
6.6 Typical Characteristics 8
7 Detailed Description 13
7.1 Overview 13
7.2 Functional Block Diagrams 13
7.3 Feature Description 14
7.4 Device Functional Modes 15
8 Application and Implementation 17
8.1 Application Information 17
8.2 Typical Application 18
8.3 Do's and Don'ts 20
9 Power Supply Recommendations 20
10 Layout 21
10.1 Layout Guidelines 21
10.2 Layout Examples 21
11 Device and Documentation Support 23
11.1 Device Support 23
11.2 Documentation Support 23
11.3 Community Resources 23
11.4 Trademarks 24
11.5 Electrostatic Discharge Caution 24
11.6 Glossary 24
12 Mechanical, Packaging, and Orderable Information 24

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2014) to Revision C **Page**

- Moved AEC-Q100 qualification bullet to first in Features list 1
- Added TI Design 1
- Changed TPS717xx-Q1 to TPS717-Q1 throughout document 1
- Added footnote and C_{IN}, R_2, and C_{NR} parameters to *Recommended Operating Conditions* table 6
- Changed V_{FB} parameter in *Electrical Characteristics* table 7
- Changed $\Delta V_{OUT(\Delta IOUT)}$ parameter typical specification in *Electrical Characteristics* table 7
- Changed units of V_n parameter in *Electrical Characteristics* table 7
- Deleted UVLO parameter minimum specification from *Electrical Characteristics* table 7
- Changed T_A to T_J in x-axis of Figure 7, Figure 10, and Figure 11 9
- Changed 40 mV/div to 40 mA/div in y-axis of Figure 28 12
- Added last two sentences to *Undervoltage Lockout (UVLO)* section 15
- Changed last bulleted condition in *Normal Operation* section 15
- Changed T_J specification in *Normal mode* row of Table 1 16
- Added last sentence to *Input and Output Capacitor Requirements* section 17
- Clarified discussion of R_2 in second paragraph of *Design Considerations* section 19
- Changed first and third paragraphs of *Do's and Don'ts* section 20

Copyright © 2012–2016, Texas Instruments Incorporated

Changes from Revision A (August 2013) to Revision B **Page**

- Changed format to meet latest data sheet standards 1
- Changed Features list on front page: added, deleted, and reordered several bullets 1
- Added *ESD Ratings* table and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections..... 1
- Added several Applications list bullets on front page 1
- Deleted pinout drawings from front page 1
- Changed pin descriptions throughout *Pin Functions* table 4
- Added parametric measurement for I_{SHDN} for DRV package 7
- Changed Figure 1, Figure 2, Figure 3, and Figure 4: removed legend, added call-outs for clarity 8
- Changed title of Figure 15 and Figure 17..... 9
- Changed *Overview* section 13
- Corrected input and output symbols in operational amplifiers in Functional Block Diagrams 13
- Changed *Undervoltage Lockout (UVLO)* section text: reworded for clarity..... 15
- Deleted *Reverse Current Protection* section 17
- Changed Equation 4 19

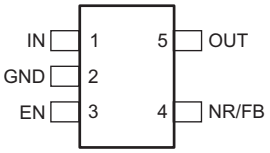
Changes from Original (September 2012) to Revision A **Page**

- Changed front page to two-column format. 1
- Added part number TPS71745-Q1. 1
- Changed C3B to C4B in Features list 1
- Removed Ordering Information table 4
- Added Junction Temperature to *Absolute Maximum Ratings* table 5
- Changed C3B to C4B in Absolute Maximum Ratings table. 5
- Changed Application Information section to one-column format. 18

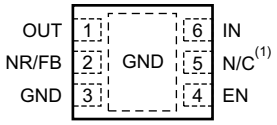
Copyright © 2012–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

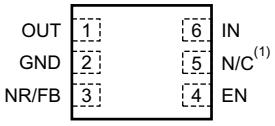
DCK Package
5-Pin SOT
Top View



DRV Package
2-mm × 2-mm, 6-Pin WSON
Top View



DSE Package
1.5-mm × 1.5-mm, 6-Pin WSON
Top View



(1) N/C = No connection

Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	DCK (SOT)	DRV (WSON)	DSE (WSON)		
EN	3	4	4	I	Driving the enable pin (EN) above $V_{EN(high)}$ turns on the regulator. Driving this pin below $V_{EN(low)}$ puts the regulator into standby mode, thereby disabling the output and reducing operating current.
FB	4	2	3	I	Adjustable voltage version only. The voltage at this pin is fed to the error amplifier. A resistor divider from OUT to FB sets the output voltage when in regulation.
GND	2	3	2	—	Ground
IN	1	6	6	I	Input to the device. A 0.1-µF to 1-µF capacitor is recommended for better performance.
N/C	—	5	5	—	Not connected. This pin can be tied to ground to improve thermal dissipation.
NR	4	2	3	—	Fixed voltage versions only. An external capacitor connected to this pin bypasses noise generated by the internal band gap, thus lowering output noise.
OUT	5	1	1	O	This pin is the regulated output voltage. A minimum capacitance of 1 µF is required for stability from this pin to ground.

Copyright © 2012–2016, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted), all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	7	V
	V_{FB}	–0.3	3.6	
	V_{NR}	–0.3	3.6	
	V_{EN}	–0.3	V_{IN} + 0.3 V(2)	
	V_{OUT}	–0.3	7	
Current	I_{OUT}	Internally limited		A
Continuous total power dissipation	P_{DISS}	See *Thermal Information* table		
Ambient temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{EN} absolute maximum rating is V_{IN} + 0.3 V or 7 V, whichever is greater.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
TPS717-Q1 in DCK and DSE packages				
$V_{(ESD)}$ Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±750	V
		Corner pins, DCK (1, 3, 4, and 5)	±750	
		Corner pins, DSE (1, 3, 4, and 6)	±750	
TPS717-Q1 in DRV package				
$V_{(ESD)}$ Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±500	V
		Corner pins (1, 3, 4, and 6)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Copyright © 2012–2016, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		6.5	V
V_{OUT}	Output voltage	0.9		5	V
I_{OUT}	Output current	0		150	mA
V_{EN}	Enable voltage	0		V_{IN}	V
C_{IN}	Input capacitor		1		µF
R_2	Lower feedback resistor	160	320	332	kΩ
C_{NR}	Noise reduction capacitor		10		nF
C_{OUT}	Output capacitor	1 (1)		100	µF
T_J	Junction temperature	–40		125	°C

(1) Adjustable voltage version only. When using feedback resistors that are smaller than recommended, the minimum output capacitance must be greater than 5 µF.

6.4 Thermal Information

THERMAL METRIC (1)		TPS717-Q1			UNIT
		DCK (SOT)	DRV (WSON)	DSE (WSON)	
		5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	279.2	71.1	190.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.5	96.5	94.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.1	40.5	149.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	2.7	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.1	40.9	152.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	10.7	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2012–2016, Texas Instruments Incorporated

6.5 Electrical Characteristics

Over operating temperature range (T_J, T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)				2.5		6.5	V
V_{FB}	Feedback pin voltage (TPS71701)		I_{OUT} = 5 mA		–2%	0.793	2%	V
V_{OUT}	Output voltage range	TPS717-Q1			0.9		5	V
		TPS71701-Q1			0.9		6.5 – V_{DO}	
V_{OUT}	Output accuracy (nominal)		T_A = 25°C			±2.5		mV
	Output accuracy (V_{OUT} < 1 V)	Over V_{IN}, I_{OUT}, temperature(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.5 V, 0 mA ≤ I_{OUT} ≤ 150 mA		–30		30	
	Output accuracy (V_{OUT} ≥ 1 V)	Over V_{IN}, I_{OUT}, temperature(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.5 V, 0 mA ≤ I_{OUT} ≤ 150 mA		–3%		3%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 5 mA			125		µV/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		0 mA ≤ I_{OUT} ≤ 150 mA			70		µV/mA
V_{DO}	Dropout voltage(3) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 150 mA			170	300	mV
I_{LIM} (fixed)	Output current limit (fixed output)		V_{OUT} = 0.9 × $V_{OUT(nom)}$		200	325	575	mA
I_{LIM} (adjustable)	Output current limit (TPS71701-Q1)		V_{OUT} = 0.9 × $V_{OUT(nom)}$		200	325	575	mA
I_{GND}	Ground pin current		I_{OUT} = 0.1 mA			45	80	µA
			I_{OUT} = 150 mA			100		
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, 2.5 V ≤ V_{IN} < 4.5 V, T_A = –40°C to 125°C			0.20	1.5	µA
			V_{EN} ≤ 0.4 V, 4.5 V ≤ V_{IN} ≤ 6.5 V, T_A = –40°C to 125°C			0.90		
			V_{EN} ≤ 0.4 V, 2.5 V ≤ V_{IN} < 4.5 V, T_A = –40°C to 125°C, DRV package				2	
I_{FB}	Feedback pin current (TPS71701-Q1)					0.02	1	µA
PSRR	Power-supply rejection ratio		V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 150 mA	f = 100 Hz		70		dB
				f = 1 kHz		70		
				f = 10 kHz		67		
				f = 100 kHz		67		
				f = 1 MHz		45		
V_n	Output noise voltage		BW = 100 Hz to 100 kHz, V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 10 mA	C_{NR} = none		95 × V_{OUT}		$\mu V_{RMS}/V$
				C_{NR} = 0.001 µF		25 × V_{OUT}		
				C_{NR} = 0.01 µF		12.5 × V_{OUT}		
				C_{NR} = 0.1 µF		11.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 90% $V_{OUT(nom)}$, R_L = 19 Ω, C_{OUT} = 1 µF	0.9 V ≤ V_{OUT} ≤ 1.6 V, C_{NR} = 0.001 µF		0.700		ms
				1.6 V < V_{OUT} < $V_{OUT(max)}$, C_{NR} = 0.01 µF		0.160		
$V_{EN(high)}$	Enable high (enabled)		V_{IN} ≤ 5.5 V		1.2		6.5(4)	V
			5.5 V < V_{IN} ≤ 6.5 V		1.25		6.5	
$V_{EN(low)}$	Enable low (shutdown)				0		0.4	V
$I_{EN(high)}$	Enable pin current, enabled		EN = 6.5 V			0.02	1	µA
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		
UVLO	Undervoltage lockout		V_{IN} rising			2.45	2.49	V
	Hysteresis		V_{IN} falling			150		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.5 V, whichever is greater.
(2) Does not include external resistor tolerances.
(3) V_{DO} is not measured for devices with $V_{OUT(nom)}$ < 2.6 V because minimum V_{IN} = 2.5 V.
(4) Maximum $V_{EN(high)}$ = V_{IN} + 0.3 or 6.5 V, whichever is smaller.

Copyright © 2012–2016, Texas Instruments Incorporated

6.6 Typical Characteristics

Over operating temperature range (T_J, T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

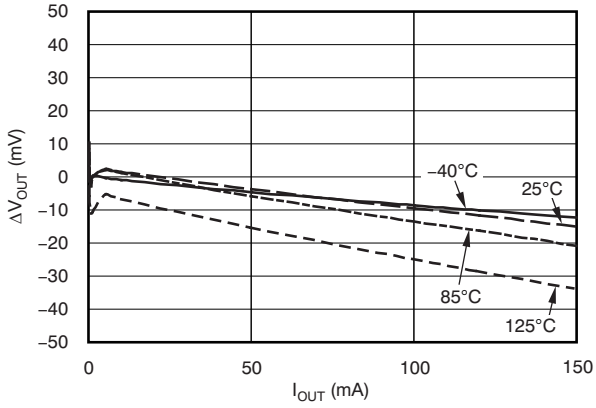


Figure 1. Load Regulation

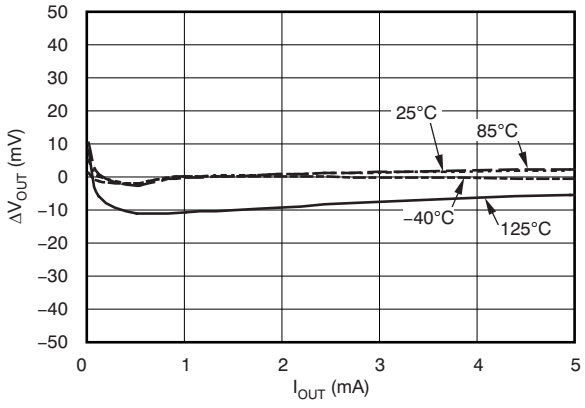


Figure 2. Load Regulation Under Light Loads

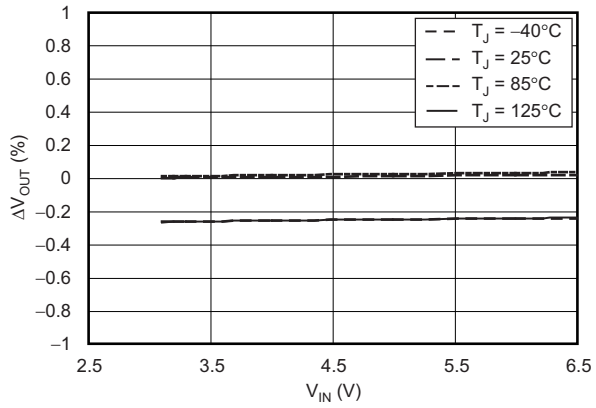


Figure 3. Line Regulation (I_{OUT} = 5 mA)

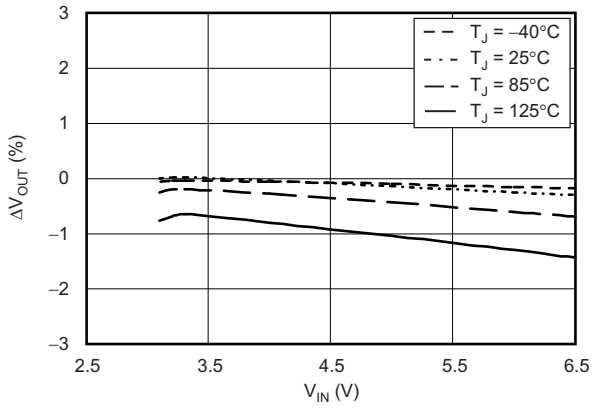


Figure 4. Line Regulation (I_{OUT} = 150 mA)

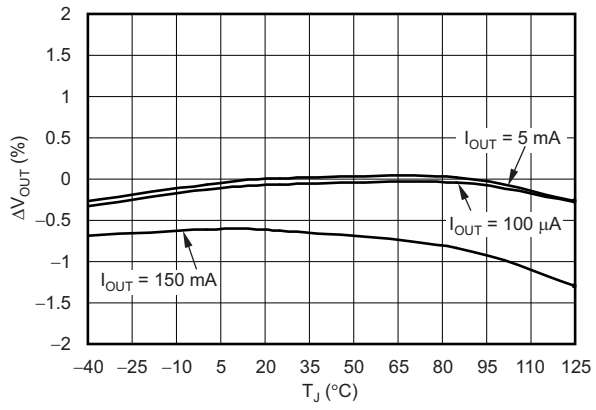


Figure 5. Output Voltage vs Temperature

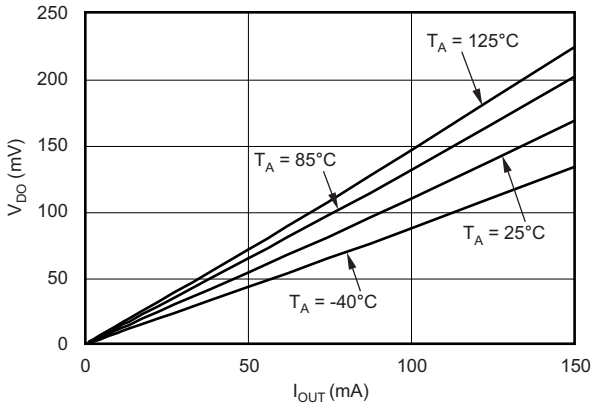


Figure 6. Dropout Voltage vs Output Current

Copyright © 2012–2016, Texas Instruments Incorporated

Typical Characteristics (continued)

Over operating temperature range (T_J, T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

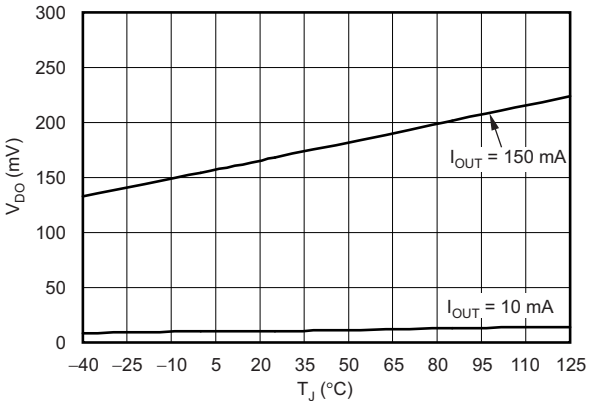


Figure 7. Dropout Voltage vs Temperature

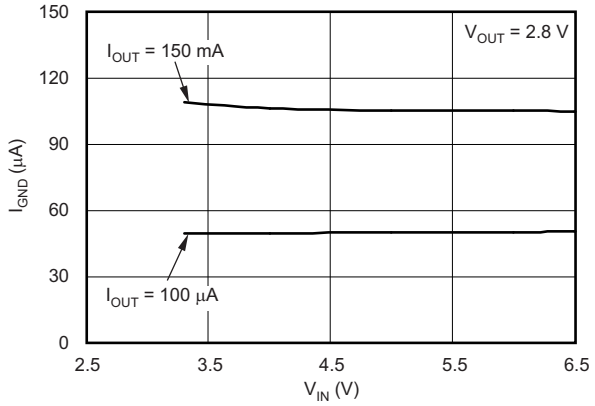


Figure 8. Ground Pin Current vs Input Voltage

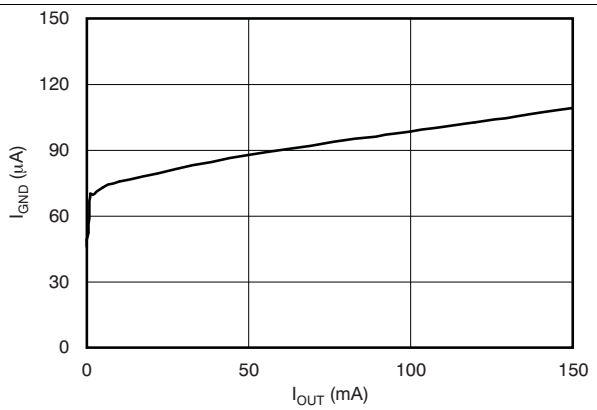


Figure 9. Ground Pin Current vs Output Current

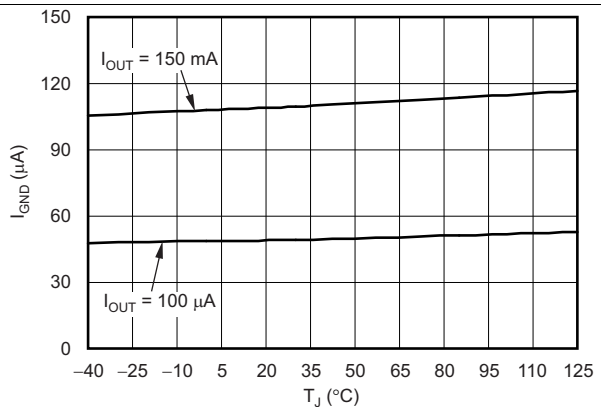


Figure 10. Ground Pin Current vs Temperature (Enabled)

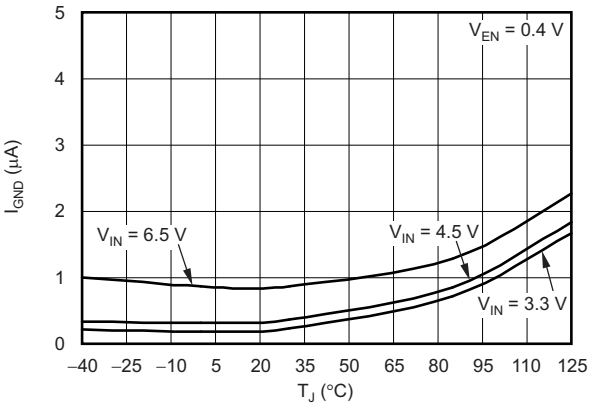


Figure 11. Ground Pin Current vs Temperature (Disabled)

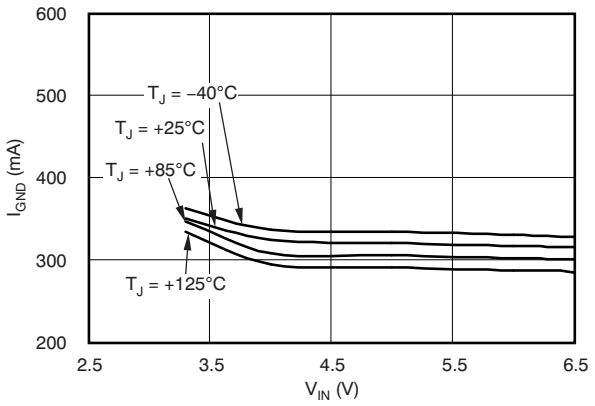


Figure 12. Current Limit vs Input Voltage

Typical Characteristics (continued)

Over operating temperature range (T_J, T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

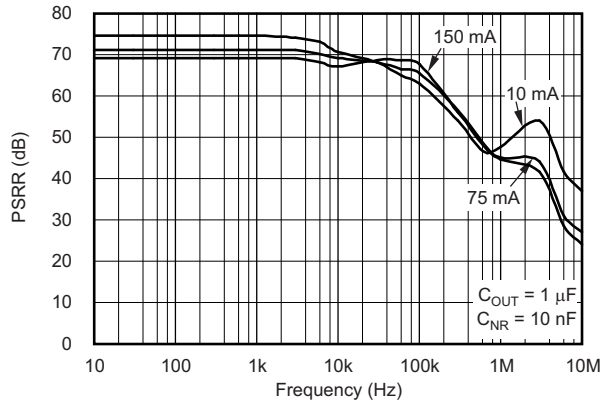


Figure 13. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 1 V)

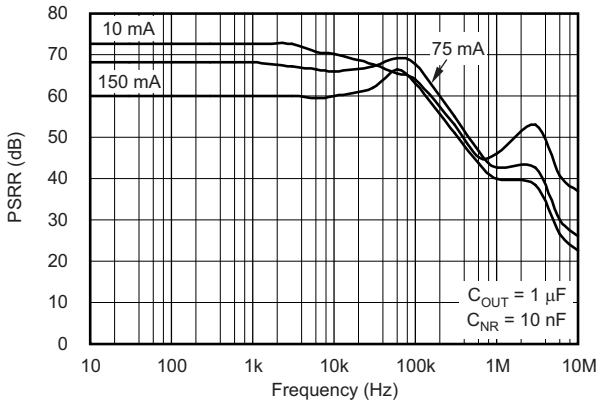


Figure 14. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 0.5 V)

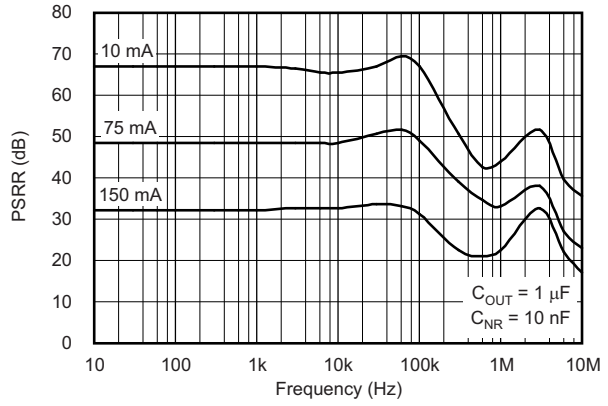


Figure 15. Power-Supply Ripple Rejection vs Frequency in Dropout Conditions (V_{IN} – V_{OUT} = 0.25 V)

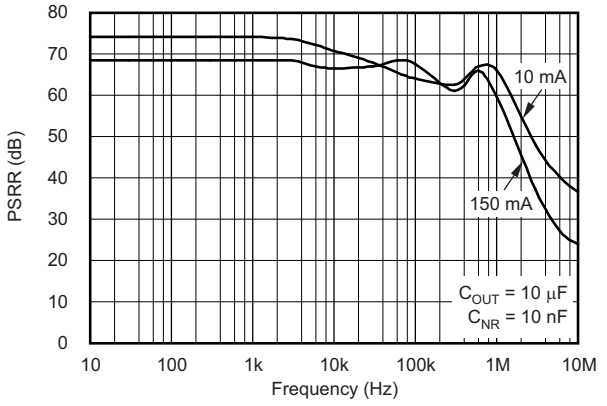


Figure 16. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 1 V)

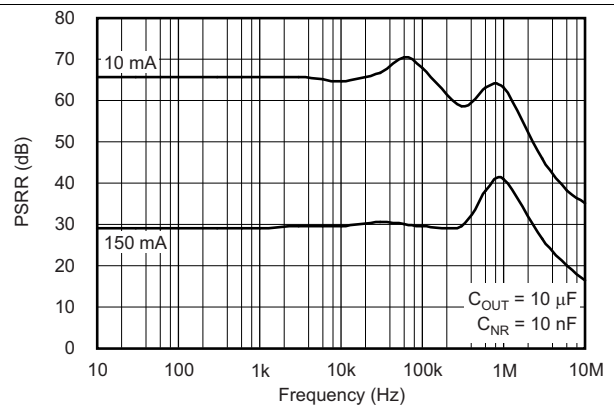


Figure 17. Power-Supply Ripple Rejection vs Frequency in Dropout Conditions (V_{IN} – V_{OUT} = 0.25 V)

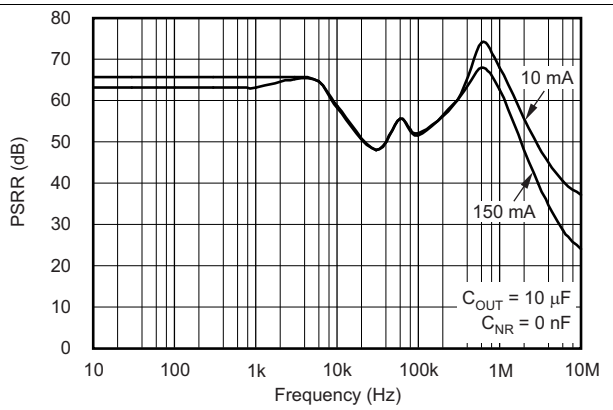


Figure 18. Power-Supply Ripple Rejection vs Frequency (V_{IN} – V_{OUT} = 1 V)

Copyright © 2012–2016, Texas Instruments Incorporated

Typical Characteristics (continued)

Over operating temperature range (T_J, T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

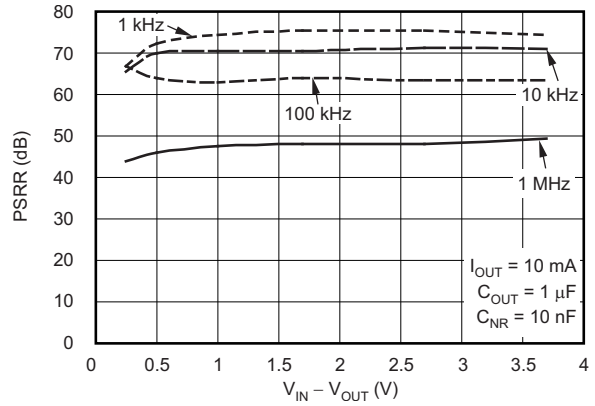


Figure 19. Power-Supply Ripple Rejection vs (V_{IN} – V_{OUT})

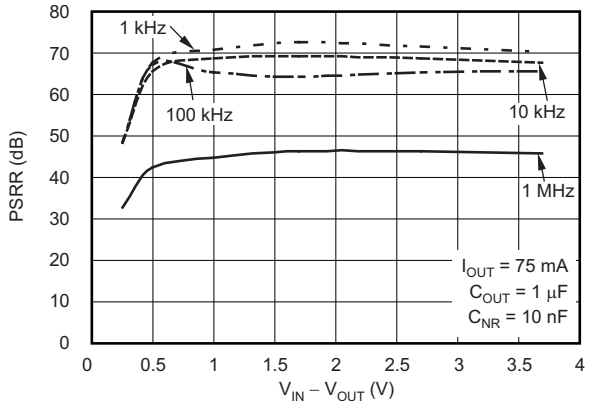


Figure 20. Power-Supply Ripple Rejection vs (V_{IN} – V_{OUT})

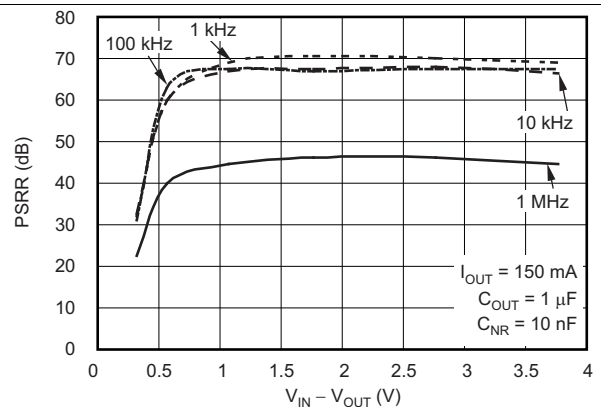


Figure 21. Power-Supply Ripple Rejection vs (V_{IN} – V_{OUT})

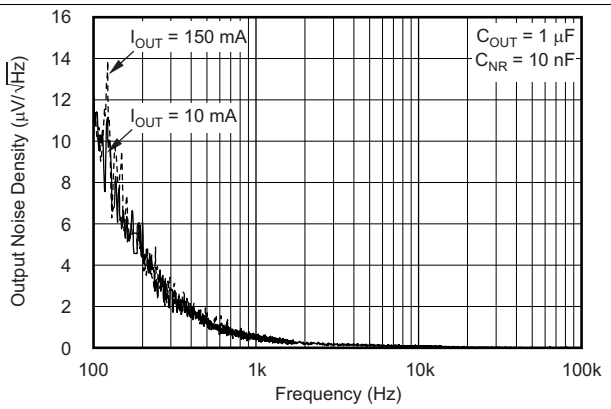


Figure 22. Output Spectral Noise Density vs Output Current

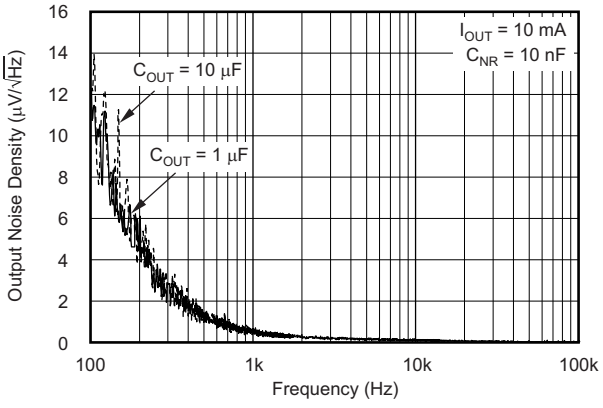


Figure 23. Output Spectral Noise Density vs Output Capacitance

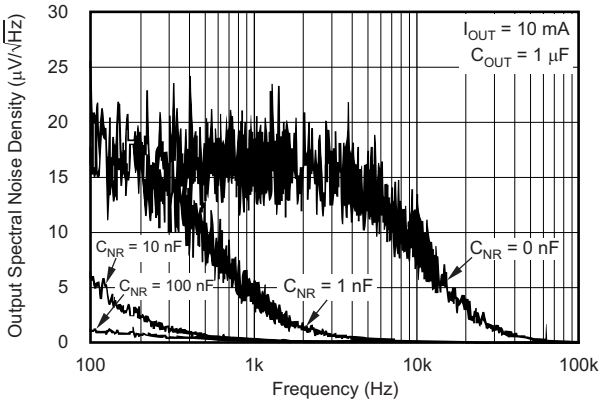


Figure 24. Output Spectral Noise Density vs Noise Reduction

Copyright © 2012–2016, Texas Instruments Incorporated

Typical Characteristics (continued)

Over operating temperature range (T_J, T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{NR} = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701-Q1), V_{OUT} = 2.8 V. Typical values are at T_A = 25°C.

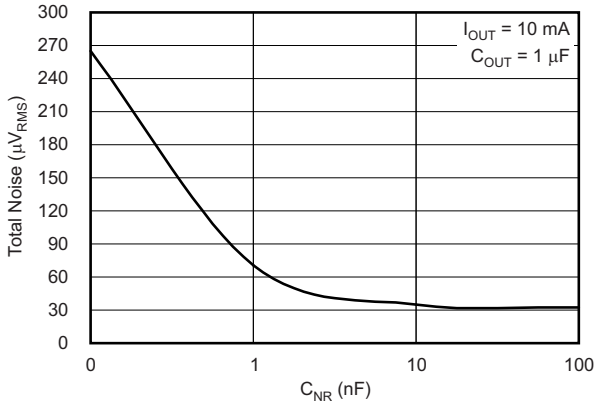


Figure 25. Total Output Noise vs Noise Reduction

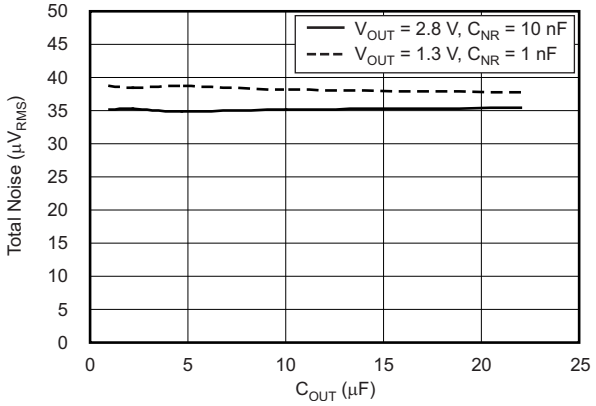


Figure 26. Total Output Noise vs Output Capacitance

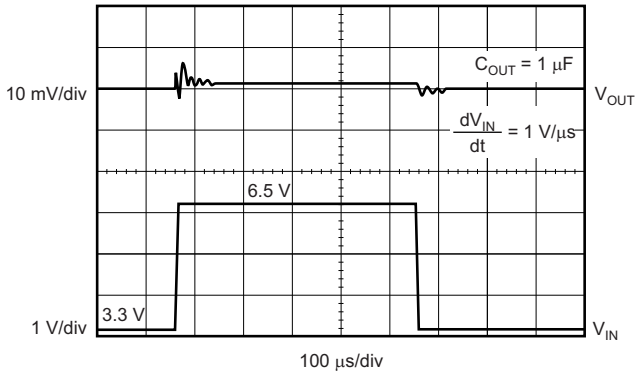


Figure 27. Line Transient Response

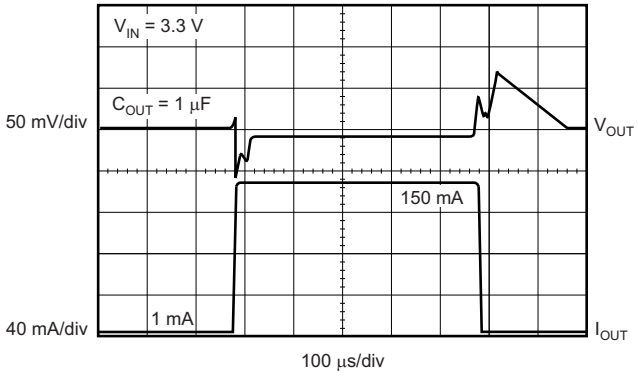


Figure 28. Load Transient Response

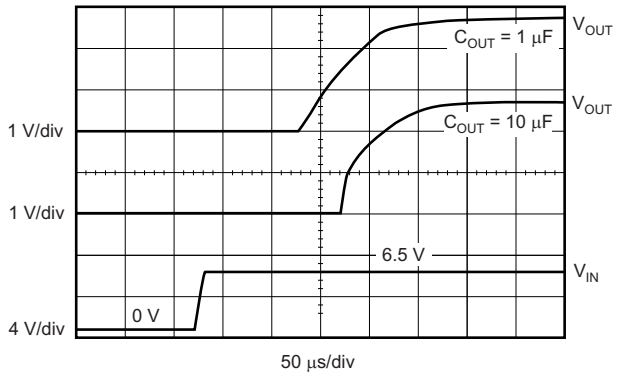


Figure 29. Turn-On Response

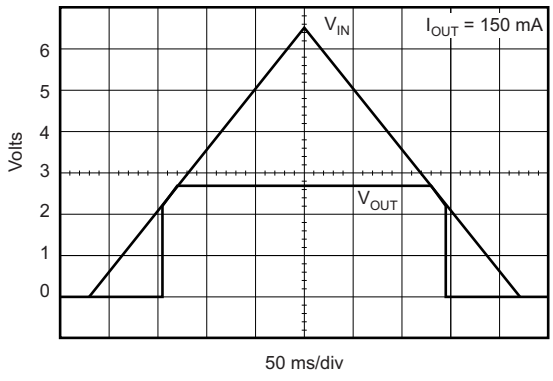


Figure 30. Power-Up and Power-Down

Copyright © 2012–2016, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The TPS717-Q1 family of low-dropout (LDO) regulators combines the high performance required by many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection with very low headroom ($V_{IN} – V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS717-Q1 family of devices an excellent choice for battery-powered applications. All versions have thermal and overcurrent protection. These devices are all also AEC-100 qualified for the grade 1 temperature range.

7.2 Functional Block Diagrams

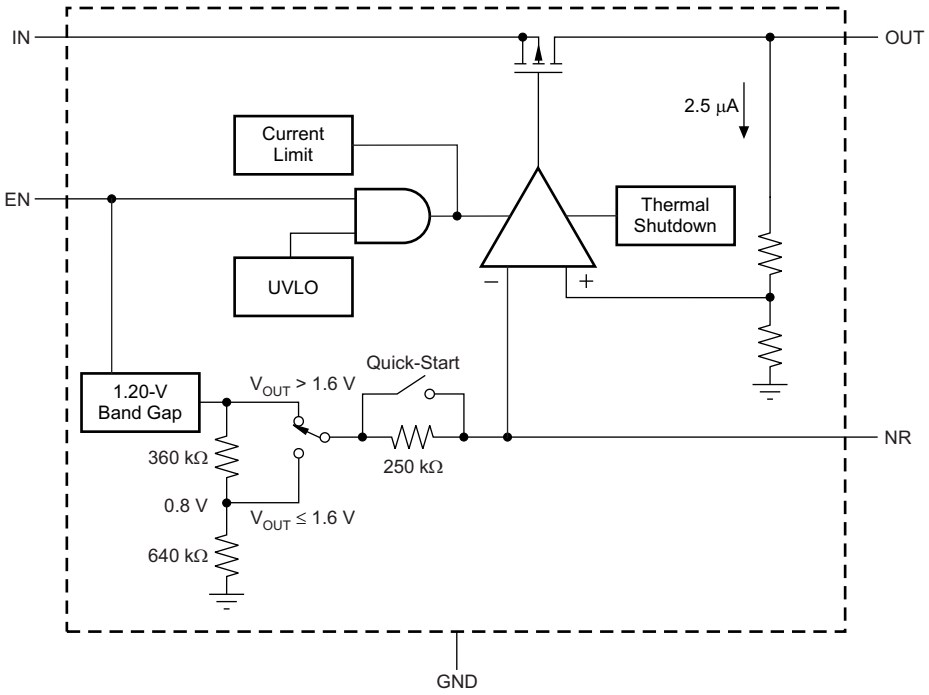


Figure 31. Fixed Voltage Versions

Functional Block Diagrams (continued)

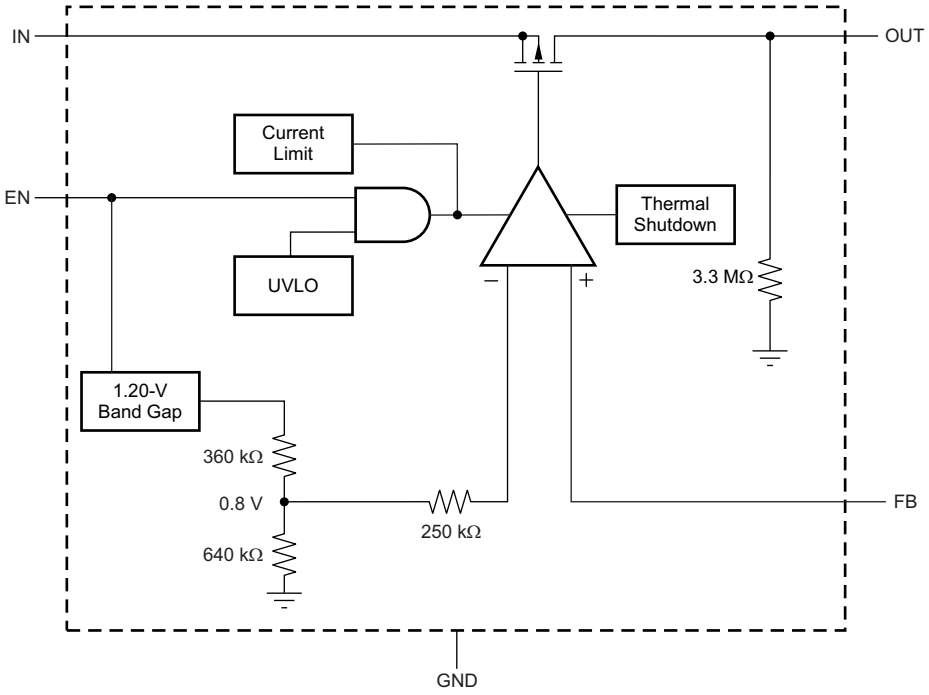


Figure 32. Adjustable Voltage Version

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS717-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS717-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS717-Q1 use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see Figure 31). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance, so a low-leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, apply V_{IN} first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower; see Figure 29 in the *Typical Characteristics* section. The quick-start switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during the quick-start time, use a 0.01-µF or smaller capacitor.

Copyright © 2012–2016, Texas Instruments Incorporated

Feature Description (continued)

For output voltages below 1.6 V, a voltage divider on the band-gap reference voltage is employed to optimize output regulation performance for lower output voltages. This configuration results in an additional resistor in the quick-start path and combined with the noise reduction capacitor (C_{NR}) results in slower start-up times for output voltages below 1.6 V.

Equation 1 approximates the start-up time as a function of C_{NR} for output voltages below 1.6 V:

$$t_{START} = 160\mu s + \left(540 \frac{\mu s}{nF} \times C_{NR} nF\right)\mu s \quad (1)$$

7.3.4 Undervoltage Lockout (UVLO)

The TPS717-Q1 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a limited glitch immunity so undershoot transients are typically ignored on the input if these transients are less than 5 µs in duration. Note that a slow V_{IN} ramp can cause the output voltage to rise when V_{IN} is between 1.1 V to 1.4 V when at hot temperatures. When the input is lower than 1.4 V, the UVLO circuit may not have enough headroom to keep the output fully off.

7.3.5 Minimum Load

The TPS717-Q1 is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS717-Q1 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS717-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS717-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is within the specified junction temperature range.

Copyright © 2012–2016, Texas Instruments Incorporated

Device Functional Modes (continued)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} >$ UVLO	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	UVLO $< V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 165°C$
Disabled mode (any true condition disables the device)	$V_{IN} <$ UVLO $- V_{hys}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$

Copyright © 2012–2016, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS717-Q1 belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR when a quick-start circuit fast-charges this capacitor. These features, combined with low noise, enable, low ground pin current, and ultra-small packaging, make this part ideal for automotive applications. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to 125°C.

8.1.1 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases duration of the transient. The TPS717-Q1 has an ultra-wide loop bandwidth that allows it to respond quickly to load transient events. As with any regulator, the loop bandwidth is finite and the initial transient voltage peak is controlled by the sizing of the output capacitor. Typically, larger output capacitors reduce the peak and also reduce the bandwidth of the LDO, thus slowing the response time.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF or larger low equivalent series resistance (ESR) capacitor from IN to GND near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS717-Q1 is designed to be stable with ceramic output capacitors of values 1 µF or larger. The X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. The maximum ESR of the output capacitor must be less than 1 Ω. The minimum output capacitance is increased to 5 µF or larger if using an R_2 value outside of the range of 160 kΩ to 320 kΩ.

8.1.3 Dropout Voltage

The TPS717-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DSon} of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 15 through Figure 17 in the *Typical Characteristics* section.

Copyright © 2012–2016, Texas Instruments Incorporated

Application Information (continued)

8.1.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

8.1.5 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS717-Q1, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF (minimum) noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2.5 µA of divider current has the same noise performance as a fixed voltage version.

Equation 3 approximates the total noise referred to the feedback point (FB pin) when C_{NR} = 0.01 µF:

$$V_N = 11.5 \frac{\mu V_{RMS}}{V} \times V_{OUT} \quad (3)$$

8.2 Typical Application

Figure 33 shows the basic circuit connections for the fixed voltage options. Figure 34 gives the connections for the adjustable output version (TPS71701-Q1). **Note that the NR pin is not available on the adjustable version**.

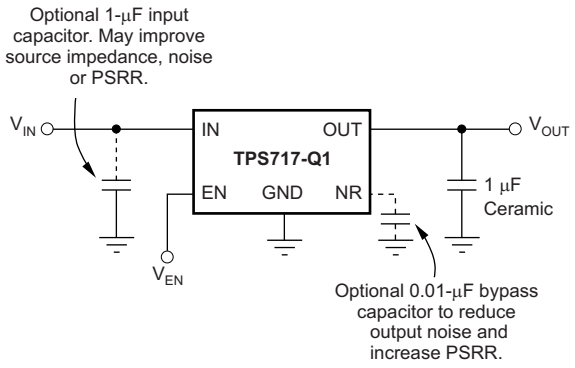


Figure 33. Typical Application Circuit (Fixed Voltage Versions)

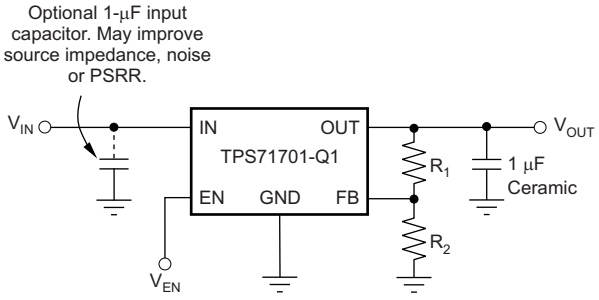


Figure 34. Typical Application Circuit (Adjustable Voltage Version)

Copyright © 2012–2016, Texas Instruments Incorporated

8.2.1 Design Requirements

Table 2 summarizes the design requirements for Figure 35.

Table 2. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V, ±10%
Output voltage	2.8 V, ±5%
Output current	100 mA typical, 150 mA peak
Output voltage transient deviation	5%
Maximum ambient temperature	85°C

8.2.2 Detailed Design Procedure

8.2.2.1 Design Considerations

For the adjustable version (TPS71701-Q1), the NR pin is replaced with a feedback (FB) pin. The voltage on this pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 4:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (4)$$

The value of R_2 directly affects the operation of the device and must be chosen in the range of approximately 160 kΩ to 332 kΩ. Sample resistor values for common output voltages are shown in Table 3.

Table 3. Sample 1% Resistor Values For Common Output Voltages

V_{OUT}	R_1	R_2
1	80.6 kΩ	324 kΩ
1.2	162 kΩ	324 kΩ
1.5	294 kΩ	332 kΩ
1.8	402 kΩ	324 kΩ
2.5	665 kΩ	316 kΩ
3.3	1.02 MΩ	324 kΩ
5	1.74 MΩ	332 kΩ

8.2.2.2 Powering a PLL Integrated on an SOC

Figure 35 shows the TPS71701-Q1 powering a phase-locked loop (PLL) that is integrated into a system-on-a-chip (SOC).

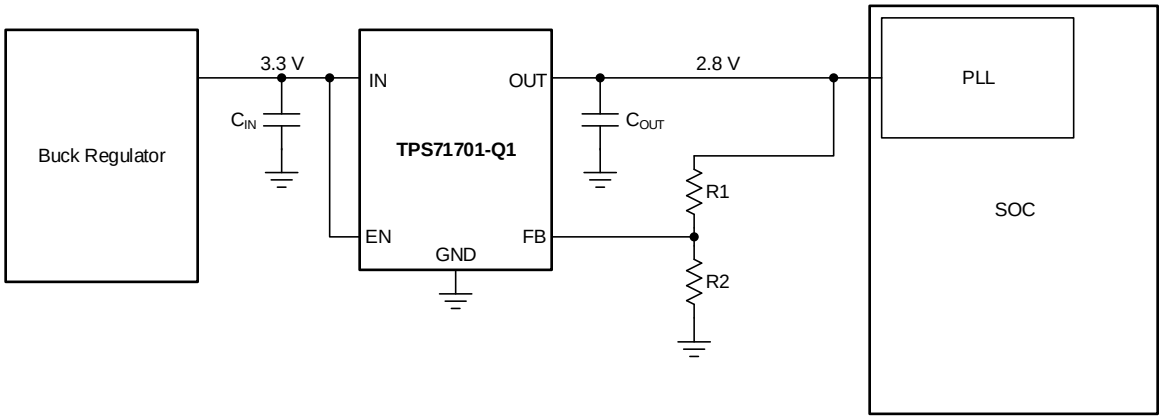


Figure 35. Typical Application Circuit: PLL on an SOC

8.2.2.3 Design Considerations

Use the input and output capacitors to ensure the voltage transient requirements. A 1-µF input and 1-µF output capacitor are selected to maximize the capacitance and minimize capacitor size.

R2 is chosen to be 158 kΩ for optimal noise and PSRR, and by Equation 2, R1 is selected to be 402 kΩ. Both R1 and R2 must be 1% tolerance resistors to meet the dc accuracy specification over line, load, and temperature.

8.2.3 Application Curve

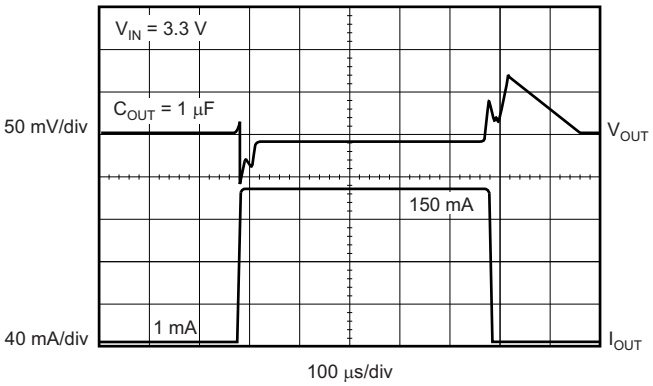


Figure 36. Load Transient Response

8.3 Do's and Don'ts

Do place at least one 1-µF ceramic capacitor as close as possible to both the input and output pins of the LDO.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not place any components in the feedback loop except for the input, output, and feed-forward capacitor and the feedback resistors.

Do not exceed the device absolute maximum ratings.

Do not float the enable (EN) pin.

9 Power Supply Recommendations

The TPS717-Q1 is designed to operate from an input voltage between 2.5 V and 6.5 V. The input supply must provide adequate headroom for the device to operate in a normal mode of operation.

Connect a low output impedance power supply directly to the IN pin of the TPS717-Q1. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor. To increase the overall PSRR of the power solution, use a pi-filter before the input of the LDO or after the FB network of the LDO.

Copyright © 2012–2016, Texas Instruments Incorporated

10 Layout

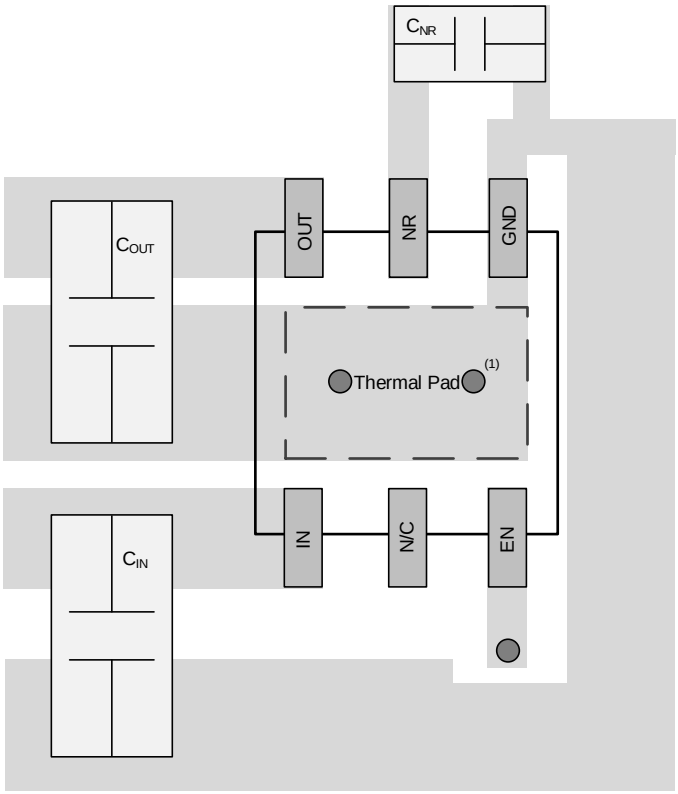
10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to the GND pin as possible, connected by wide, component-side, copper surface area. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and functions similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

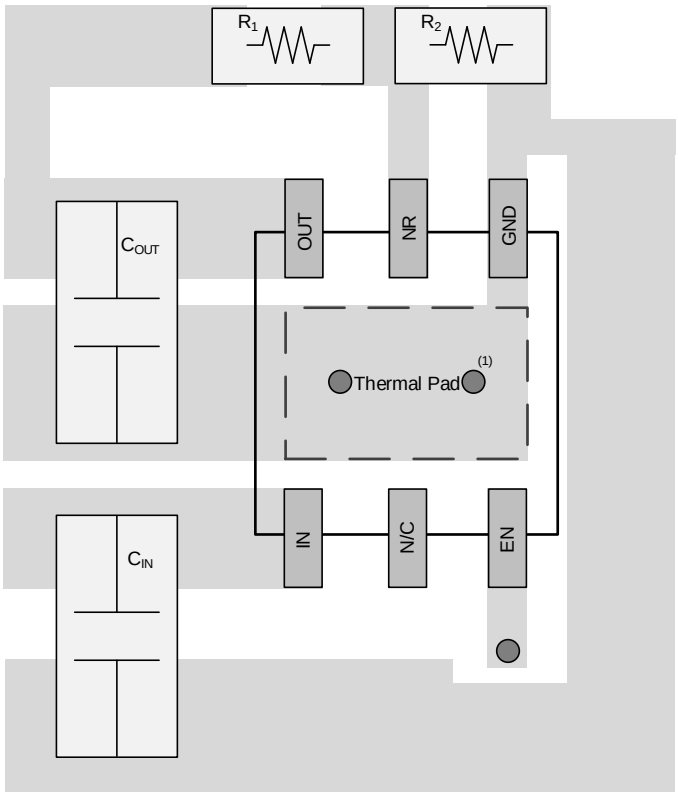
10.2 Layout Examples



(1) Circles within thermal pad area indicate vias to other layers on the board.

Figure 37. Fixed Voltage Layout

Layout Examples (continued)



(1) Circles within thermal pad area indicate vias to other layers on the board.

Figure 38. Adjustable Voltage Layout

Copyright © 2012–2016, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS717. The TPS717xxEVM-134 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 4. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS717**xx(x)QYYYz-Q1**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). An **01** denotes an adjustable voltage version. **YYY** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). **Q** and **-Q1** denote an automotive device that is qualified at grade 1.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

PMP10651 Test Results, TIDUAE4

TPS717xxEVM-134 Evaluation Module User Guide, SLVU148

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

Copyright © 2012–2016, Texas Instruments Incorporated

11.4 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2012–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71701QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13B
TPS71701QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13B
TPS71709QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHW
TPS71709QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHW
TPS71709QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD
TPS71709QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD
TPS71712QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHX
TPS71712QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHX
TPS71715QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHY
TPS71715QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHY
TPS71718QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHZ
TPS71718QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHZ
TPS71725QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIA
TPS71725QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIA
TPS71728QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIB
TPS71728QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIB
TPS71730QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIC
TPS71730QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIC
TPS71733QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SID
TPS71733QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SID
TPS71745QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHF
TPS71745QDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHF
TPS71745QDCKRQ1G4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHF
TPS71745QDCKRQ1G4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHF
TPS71745QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIE
TPS71745QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIE
TPS71750QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIF
TPS71750QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIF
TPS71750QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AV

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71750QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS717-Q1 :

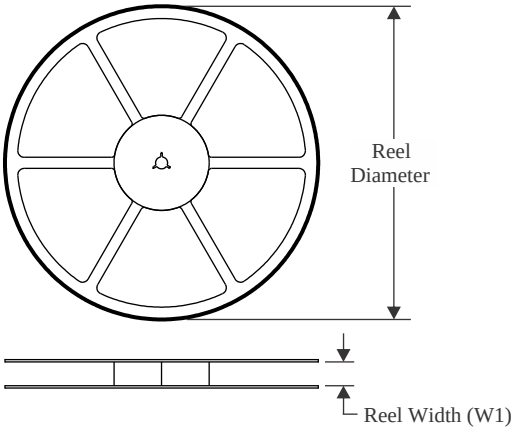
- Catalog : TPS717

NOTE: Qualified Version Definitions:

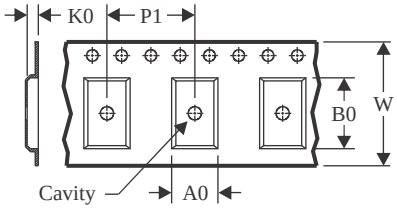
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

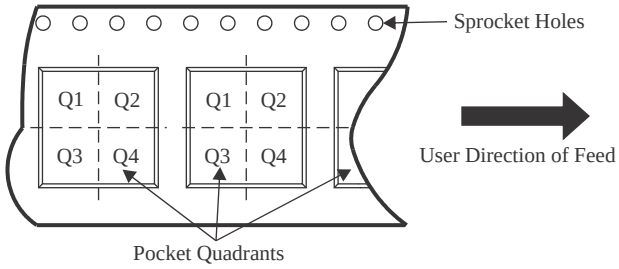


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

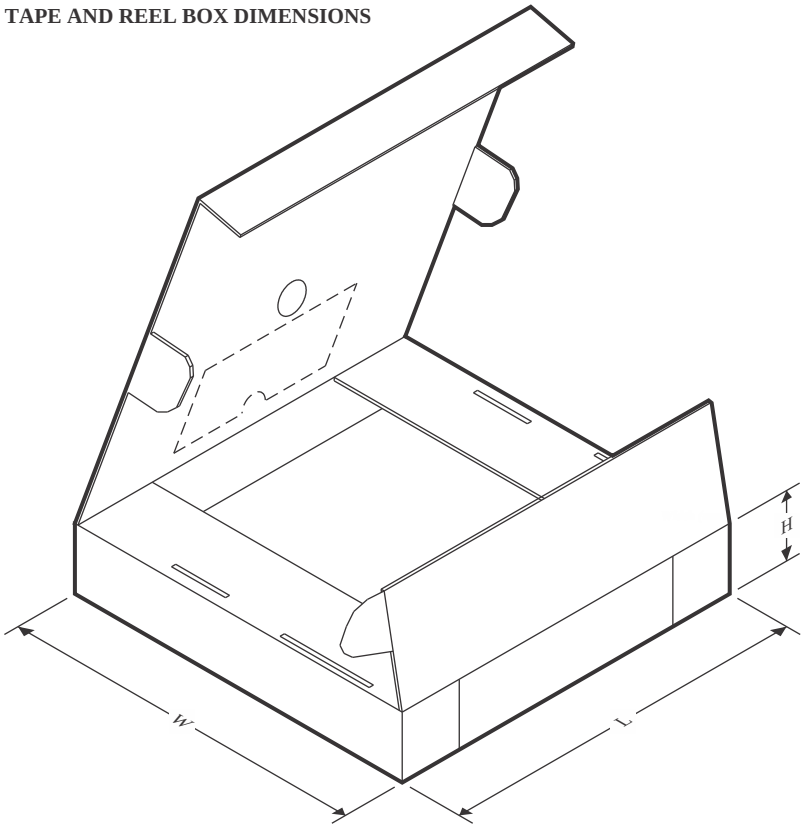
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71701QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71709QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71709QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS71712QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71715QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71718QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71725QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71728QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71730QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71733QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71745QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71745QDCKRQ1G4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71745QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71750QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS71750QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

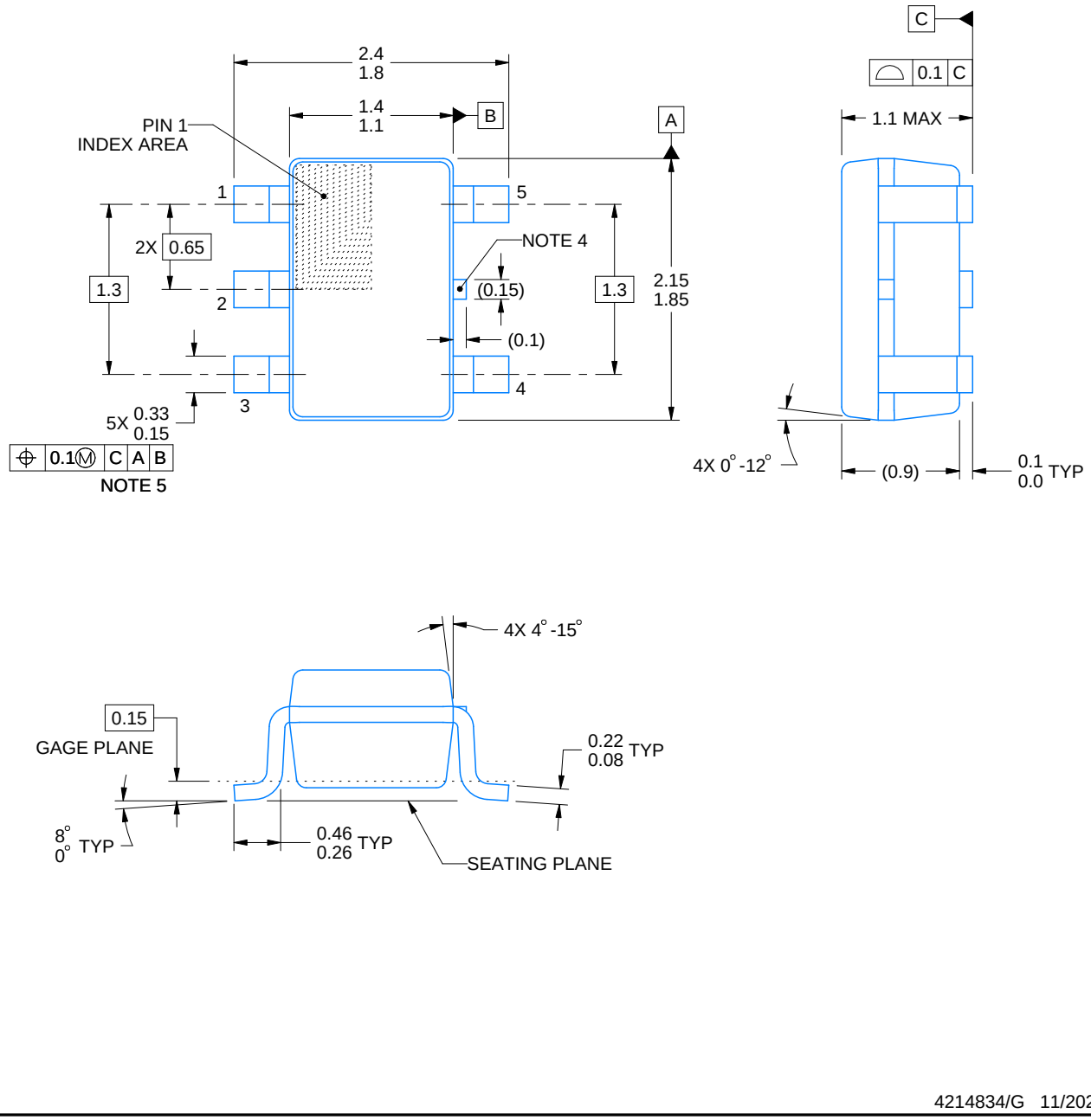
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71701QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71709QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71709QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TPS71712QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71715QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71718QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71725QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71728QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71730QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71733QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71745QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71745QDCKRQ1G4	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71745QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71750QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS71750QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

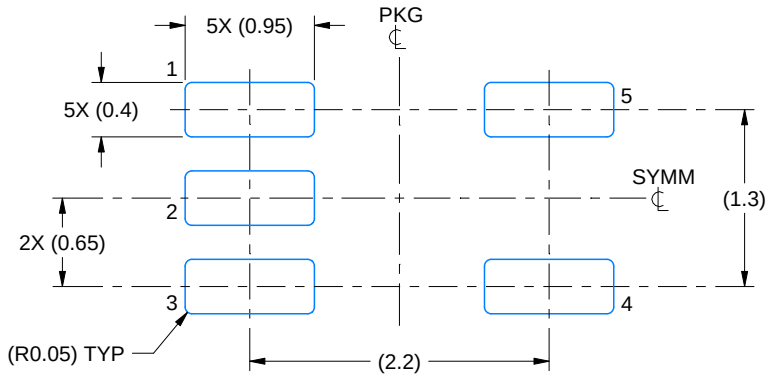
SMALL OUTLINE TRANSISTOR



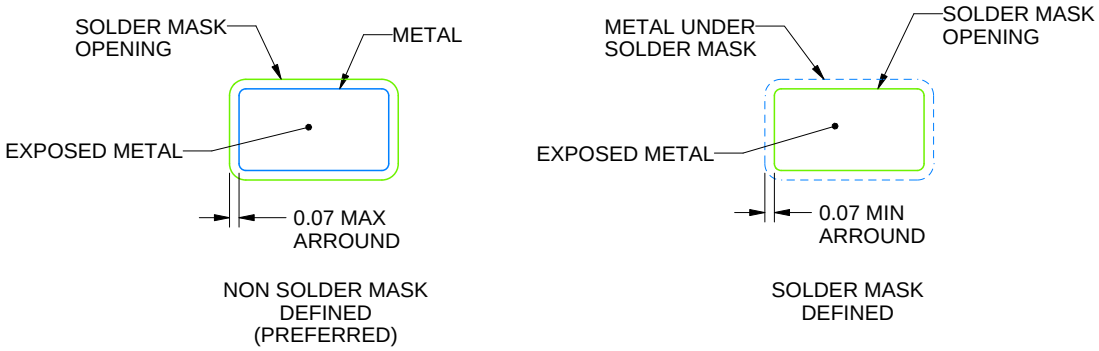
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

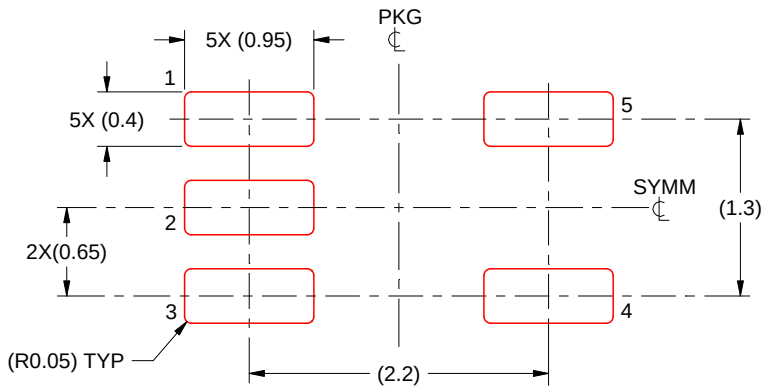


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

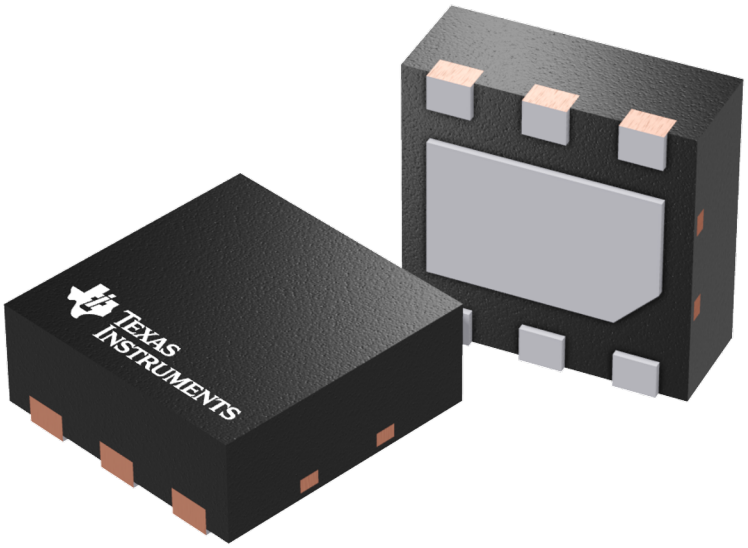
4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



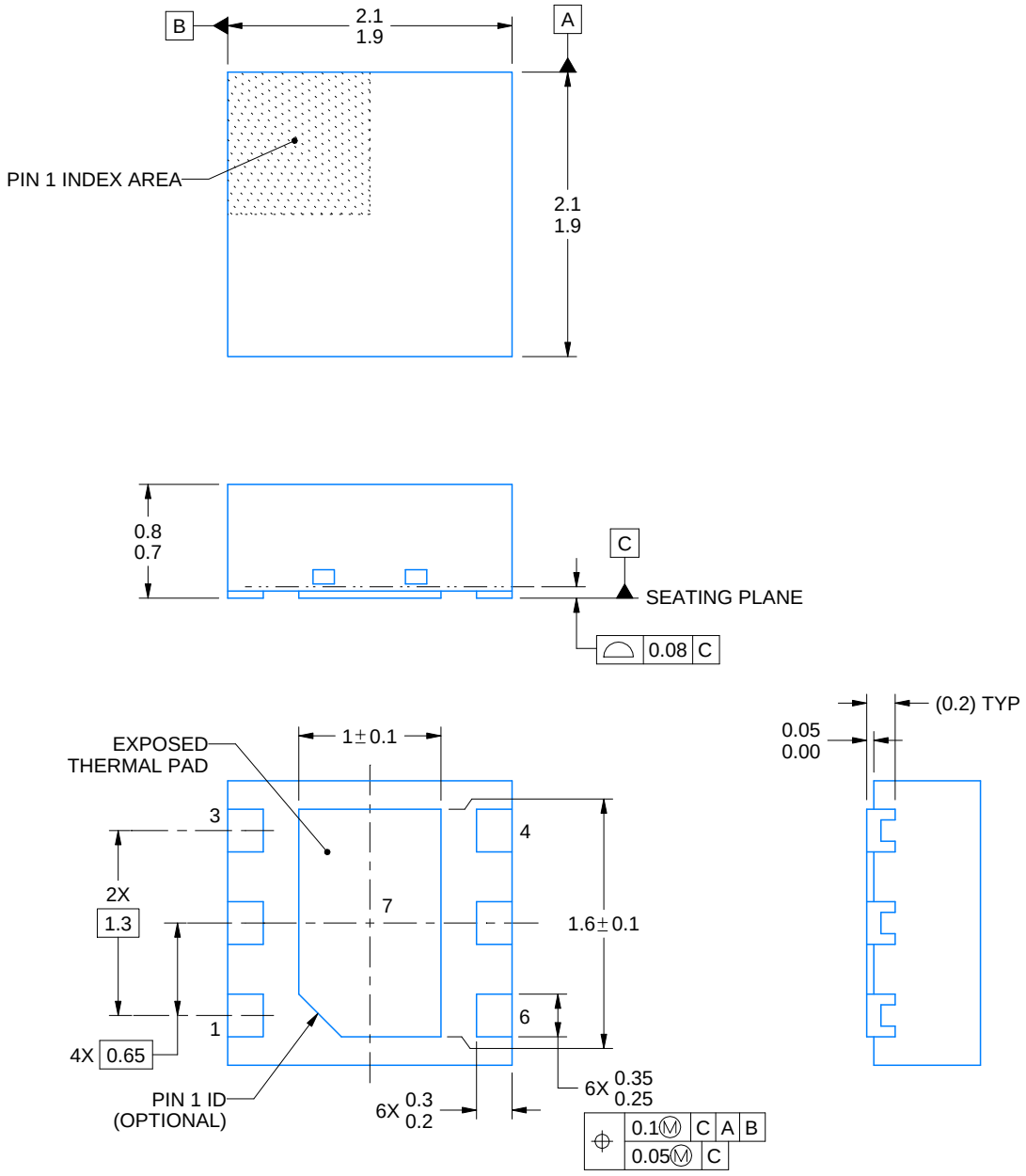
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

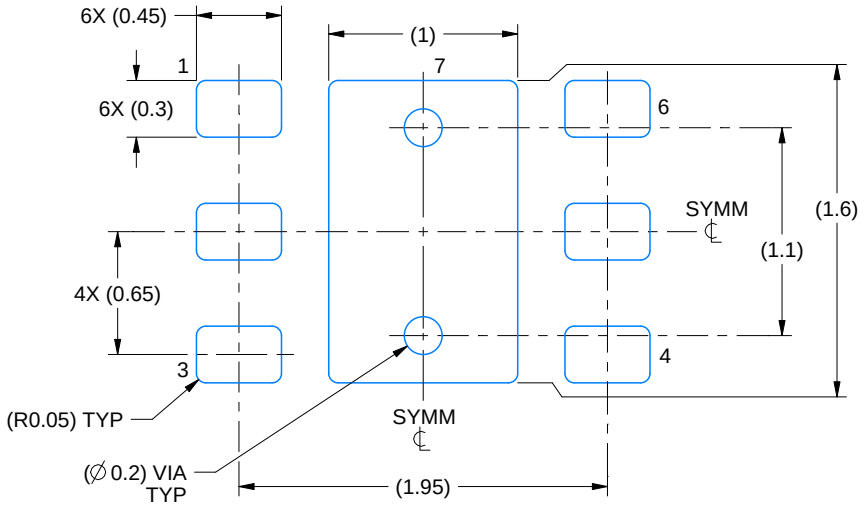
PLASTIC SMALL OUTLINE - NO LEAD



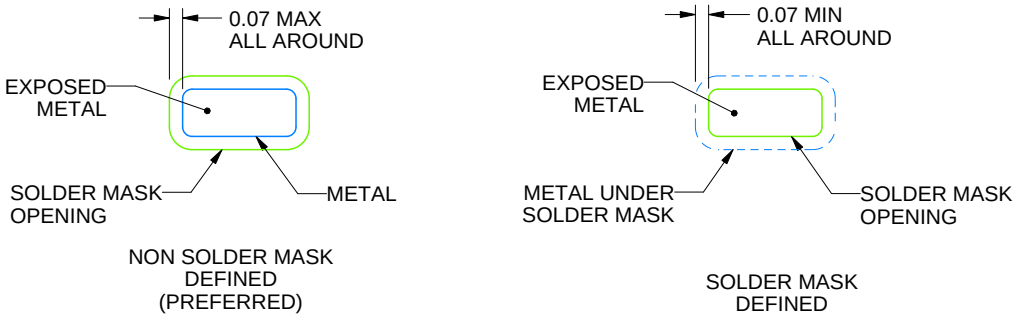
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

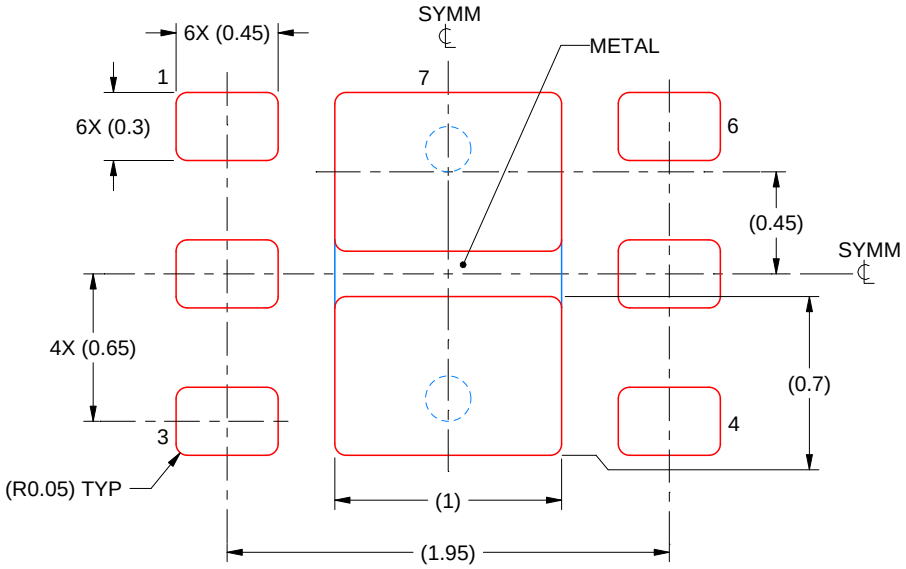


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

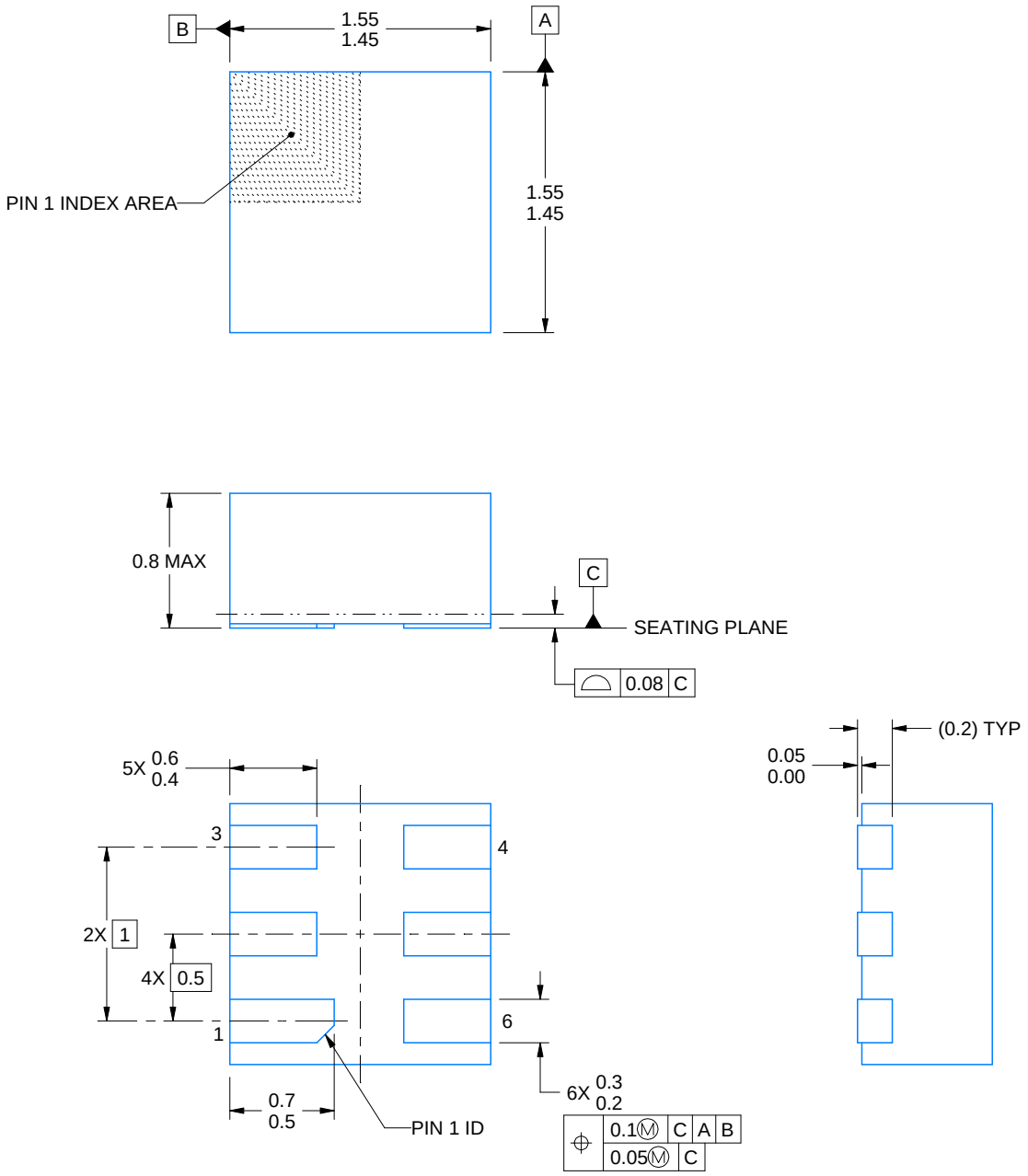
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

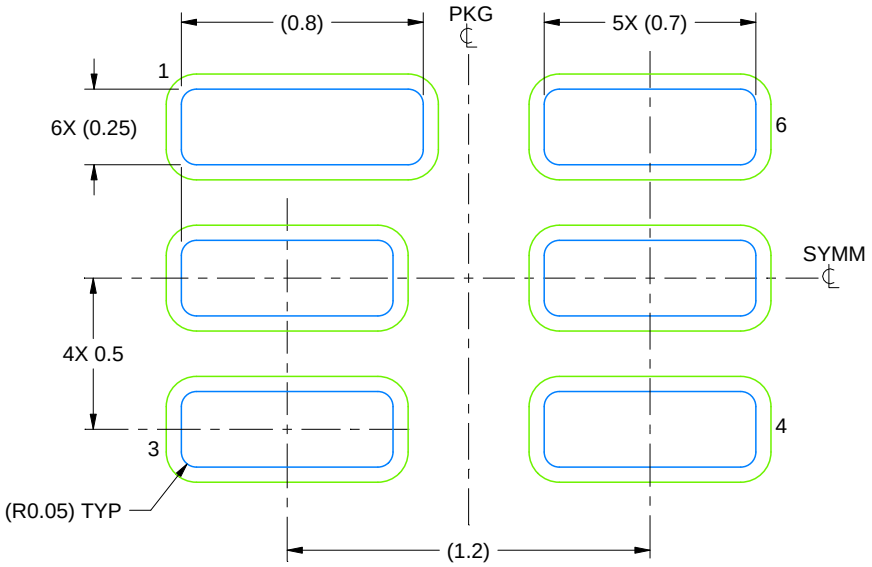
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

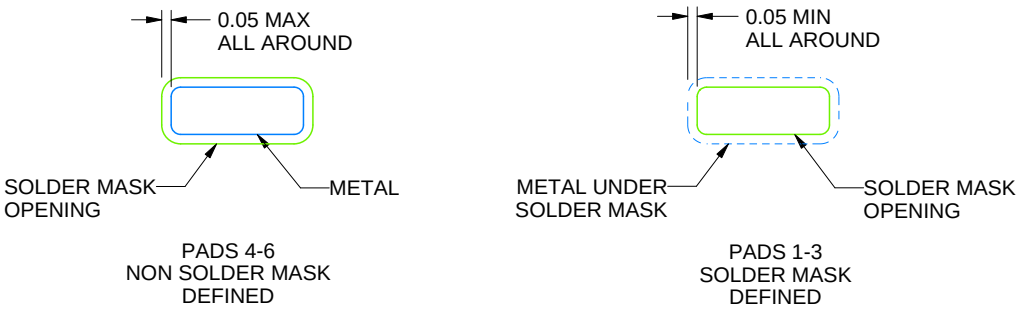
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

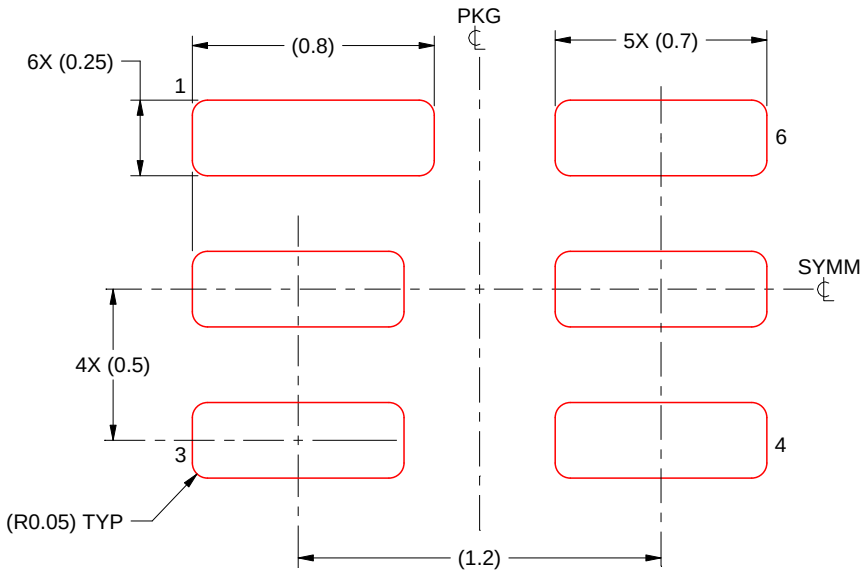
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025

ENTEGRECİ

Bu belge www.entegreci.com üzerinden sunulmaktadır.

Elektronik komponent tedarikinde Entegreci

Entegreci, Eskişehir merkezli, Türkiye geneline satış yapan bir elektronik komponent mağazasıdır. Entegreler (IC), mikrodenetleyiciler, transistörler, diyotlar, pasif elemanlar, konnektörler, modüller ve geliştirme kartları tek adetten seri üretim adetlerine kadar satılır. Ürün sayfalarında güncel stok durumunu, fiyatı ve datasheet bağlantısını bulabilirsiniz.

Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

www.entegreci.com

Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

Üreticileri görün

Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

Entegreci is an online electronic components store based in Türkiye. Search by manufacturer part number to see stock, prices and datasheets for integrated circuits, microcontrollers, transistors, passive components and connectors, or request a quote for parts that are not listed.

Bu sayfa Entegreci tarafından eklenmiştir. Belgenin önceki sayfaları asıl yayıncısına aittir ve içeriği değiştirilmemiştir; en güncel sürüm için belgenin yayıncısına başvurun.