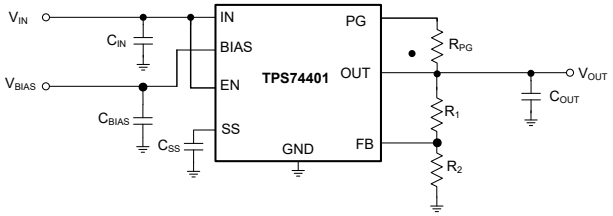
TPS74401 3.0A, Ultra-LDO With Programmable Soft-Start

1 Features

- Input voltage range: 1.1V to 5.5V
- Adjustable start-up in-rush control
- 1% accuracy over line, load, and temperature
- V_{BIAS} permits low V_{IN} operation with good transient response
- Adjustable output: 0.8V to 3.6V
- Ultra-low dropout:
  - 115mV (typical, legacy chip) at 3.0A
  - 120mV (typical, new chip) at 3.0A
- Stable with any or no output capacitor (legacy chip)
- Stable with any output capacitor ≥2.2µF (new chip)
- Power-good (PG) output allows supply monitoring or provides a sequencing signal for other supplies
- Packages:
  - 5mm × 5mm × 1mm VQFN (RGW)
  - 3.5mm × 3.5mm VQFN (RGR), and DDPAK-7 (legacy chip)

2 Applications

- Network attached storage - enterprise
- Rack servers
- Network interface cards (NIC)
- Merchant network and server PSU



Typical Application Circuit

3 Description

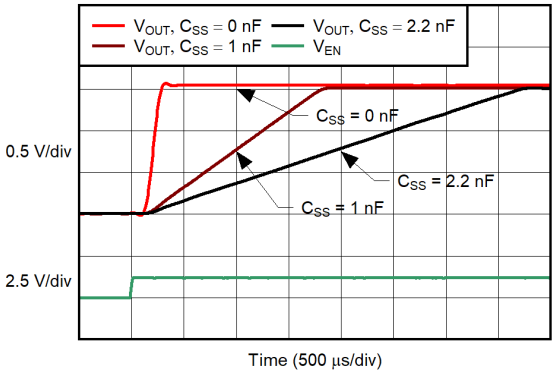
The TPS74401 low-dropout (LDO) linear regulators provide an easy-to-use robust power-management option for a wide variety of applications. The user-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and designed for powering many different types of processors and application-specific integrated circuits (ASICs). The enable input and power-good output allow easy sequencing with external regulators. Complete flexibility lets the user configure a plan that meets the sequencing requirements of field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and other applications with specific start-up requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. The device is stable without an output capacitor (legacy chip) or with any type of capacitor ≥ 2.2µF (new chip). The device is fully specified from T_J = –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS74401	KTW (TO-263, 7)	10.1mm × 15.24mm
	RGR (VQFN, 20)	3.5mm × 3.5mm
	RGW (VQFN, 20)	5mm × 5mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Turn-On Response

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4 Pin Configuration and Functions

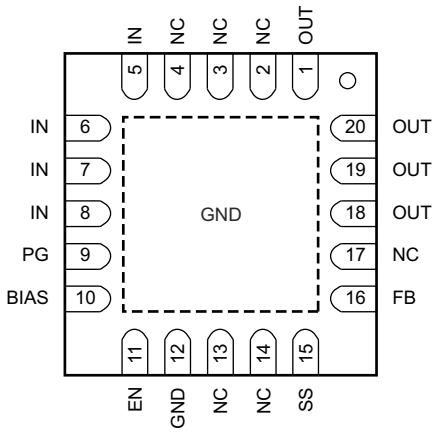

Figure 4-1. RGW and RGR Package, 5mm × 5mm and 3.5mm × 3.5mm, 20-Pin VQFN (Top View)

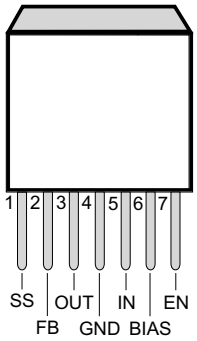

Figure 4-2. KTW Package, 7-Pin DDPAK (Top View)

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	KTW	RGW, RGR		
BIAS	6	10	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1µF or larger bias capacitor is recommended for best performance. If IN is connected to BIAS, use a 4.7µF or larger capacitor.
EN	7	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	4	12	—	Ground
IN	5	5–8	I	Unregulated input to the device. An input capacitor of 1µF or greater is recommended for best performance.
NC	N/A	2–4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18–20	O	Regulated output voltage. No capacitor is required on this pin for stability, but is recommended for excellent performance.
PAD/TAB	—	—	—	Must be soldered to the ground plane for increased thermal performance. Internally connected to ground.
PG	N/A	9	O	Power-good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold, the pin is driven to a low-impedance state. Connect a pullup resistor from 10kΩ to 1MΩ from this pin to a supply up to 5.5V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SS	1	15	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100µs.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	Soft-start voltage	–0.3	6	V
V_{FB}	Feedback voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
T_J	Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})		5.5	V
V_{EN}	Enable supply voltage			5.5	V
V_{BIAS} (1)	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})(2)		5.5	V
V_{OUT}	Output voltage	0.8		3.6	V
I_{OUT}	Output current	0		3	A
C_{OUT}	Output capacitor (legacy chip)	0			µF
	Output capacitor (new chip)	2.2			µF
C_{IN}	Input capacitor(3)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

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5.4 Thermal Information

THERMAL METRIC[1]		TPS744[2]				UNIT
		RGW (VQFN)	RGW (VQFN)[3]	RGR (VQFN)	KTW (TO-263)	
		20 PINS	20 PINS	20 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	34.7	39.1	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	31	29.3	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	13.5	10.2	12.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.4	0.4	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.8	13.5	10.1	7.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	3.6	2.0	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* the application note.
(2) Thermal data for the RGW, RGR, and KTW packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations: (a) i. RGW and RGR: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array. - ii. KTW: The exposed pad is connected to the PCB ground layer through a 6x6 thermal via array. (b) Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage. (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, refer to the Thermal Considerations section.
(3) New Chip.

5.5 Electrical Characteristics

at V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, I_{OUT} = 50mA, V_{BIAS} = 5.0V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	BIAS pin voltage range		2.375		5.25	V
V_{REF}	Internal reference (Adjustable)	T_A = +25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5V, I_{OUT} = 1.5A, V_{BIAS} = 5V	V_{REF}		3.6	V
V_{OUT}	Accuracy	2.97V ≤ V_{BIAS} ≤ 5.25V, V_{OUT} + 1.62V ≤ V_{BIAS}, 50mA ≤ I_{OUT} ≤ 3.0A[1] (legacy chip)	–1	±0.2	1	%
		V_{OUT} + V_{DO} BIAS ≤ V_{BIAS} ≤ 5.25 V, 100 mA ≤ I_{OUT} ≤ I $_{VDO\ BIAS}$, VQFN[2]	–1	±0.2	1	
		2.97V ≤ V_{BIAS} ≤ 5.25V, V_{OUT} + 1.62V ≤ V_{BIAS}, 50mA ≤ I_{OUT} ≤ 3.0A[1] (new chip)	–1	±0.3	1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5V VQFN (legacy chip)		0.0005	0.05	%/V
		$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5V DDPAK (legacy chip)		0.0005	0.06	
		$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5V (new chip)		0.001	0.05	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0mA ≤ I_{OUT} ≤ 50mA (legacy chip)		0.013		%/mA
		50mA ≤ I_{OUT} ≤ 3A (legacy chip)		0.03		%/A
		0mA ≤ I_{OUT} ≤ 50mA (new chip)		0.09		%/mA
		50mA ≤ I_{OUT} ≤ 3A (new chip)		0.09		%/A

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5.5 Electrical Characteristics (continued)

at V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, I_{OUT} = 50mA, V_{BIAS} = 5.0V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	V_{IN} dropout voltage[3]	I_{OUT} = 3A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62V, VQFN (legacy chip)		115	195	mV
		I_{OUT} = 3A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62V, DDPAK(legacy chip)		120	240	mV
		I_{OUT} = 3 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62V, VQFN (new chip)		120	200	mV
	V_{BIAS} dropout voltage[3]	I_{OUT} = 3A, V_{IN} = V_{BIAS}			1.62	V
		I_{OUT} = 1A			1.35	V
		I_{OUT} = 500mA			1.27	V
		I_{OUT} = 100mA			1.16	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT(nom)}$, VQFN (legacy chip)	3.8		6	A
		V_{OUT} = 80% × $V_{OUT(nom)}$, DDPAK (legacy chip only)	3.5		6	
		V_{OUT} = 80% × $V_{OUT(nom)}$ (new chip)	3.9		5.5	
I_{BIAS}	BIAS pin current	I_{OUT} = 0mA to 3.0 A		2	4	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4V		1	100	µA
I_{FB}	Feedback pin current[4]	I_{OUT} = 50mA to 3A	–250	95	250	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (legacy chip)		73		dB
		1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (new chip)		60		
		800kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (legacy chip)		42		
		800kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (new chip)		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (legacy chip)		62		
		1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (New Chip)		57		
		800kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (legacy chip)		50		
		800kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (new chip)		45		
V_n	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 1.5A, C_{SS} = 0.001 µF (legacy chip)		16		µVrms x Vout
		100 Hz to 100 kHz, I_{OUT} = 3A, C_{SS} = 1 nF (new chip)		20		
VTRAN	%V_{OUT} droop during load transient	I_{OUT} = 100mA to 3.0A at 1A/µs, C_{OUT} = 0µF (legacy chip)		4		%V_{OUT}
		I_{OUT} = 100mA to 3.0A at 1A/µs, C_{OUT} =2.2µF (new chip)		5		

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5.5 Electrical Characteristics (continued)

at V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, I_{OUT} = 50mA, V_{BIAS} = 5.0V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Minimum start-up time	I_{OUT} = 1.5A, C_{SS} = open (legacy chip)		100		µs
		R_{LOAD} for I_{OUT} = 1.0A, C_{SS} = open (new chip)		250		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4V, I_{OUT} = 0mA (legacy chip)	500	730	1000	nA
		V_{SS} = 0.4V, I_{OUT} = 0mA (new chip)	300	530	800	nA
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			50		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing (legacy chip)	86.5	90	93.5	$\%V_{OUT}$
		V_{OUT} decreasing (new chip)	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25V, V_{OUT} > V_{IT}		0.03	1	µA
T_J	Operating junction temperature		–40		125	℃
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing (legacy chip)		155		℃
		Shutdown, temperature increasing (new chip)		165		℃
		Reset, temperature decreasing		140		℃
$R_{PULLDOWN}$	V_{BIAS} = 5V, V_{EN} = 0V	New chip only		0.83		kΩ

(1) Devices tested at 0.8V; external resistor tolerance is not taken into account.
(2) V_{OUT} is set to 1.5V to avoid minimum V_{BIAS} restrictions.
(3) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 2% below nominal
(4) I_{FB} current flow is out of the device.

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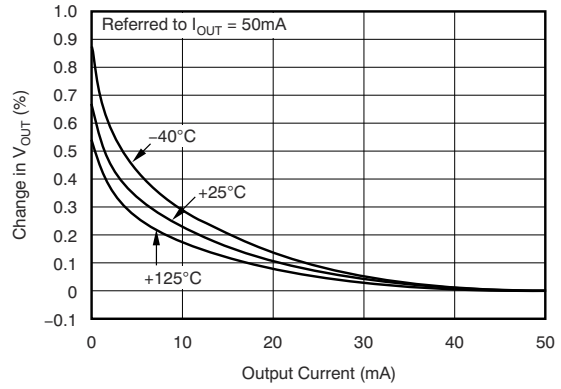
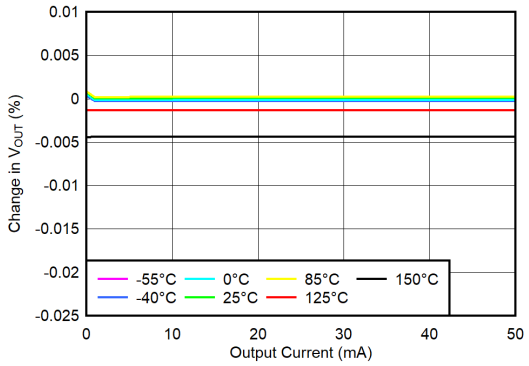
5.6 Typical Characteristics

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



Legacy chip

Figure 5-1. Load Regulation



New chip

Figure 5-2. Load Regulation at Light Load

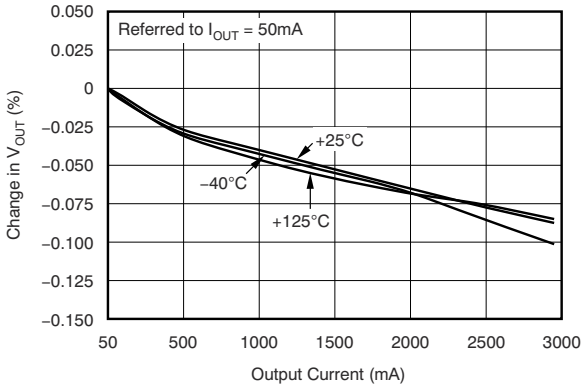
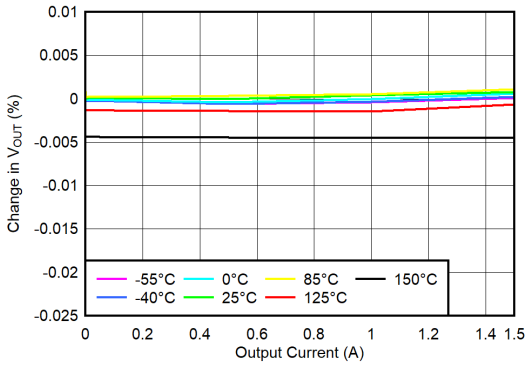
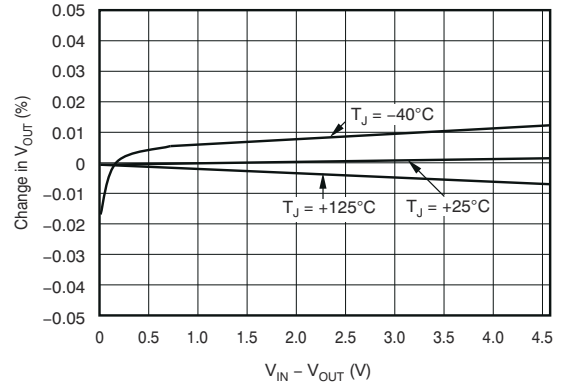


Figure 5-3. Load Regulation



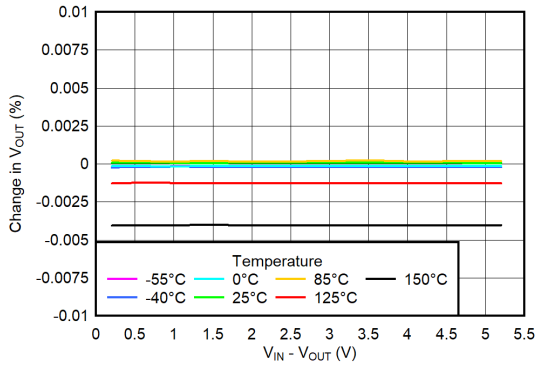
New chip

Figure 5-4. Load Regulation



Legacy chip

Figure 5-5. Line Regulation



New chip

Figure 5-6. V_{IN} Line Regulation

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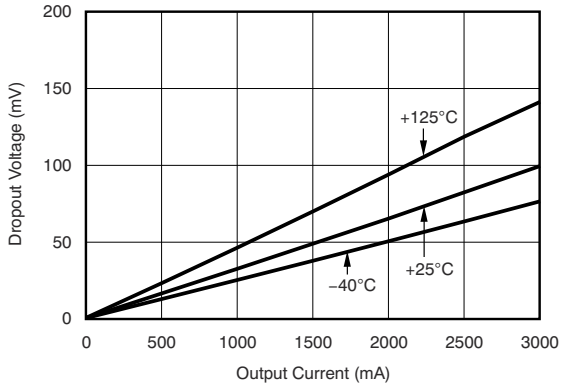
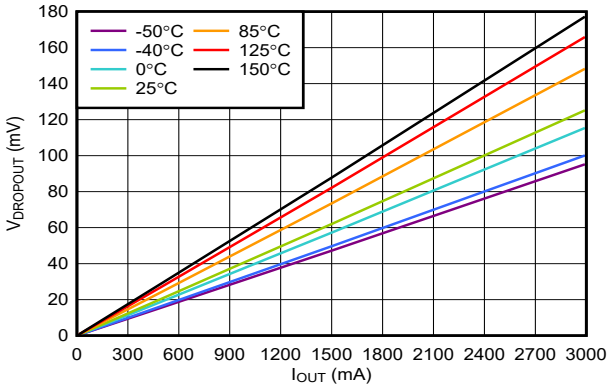
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



Legacy chip

Figure 5-7. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)



New chip

Figure 5-8. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

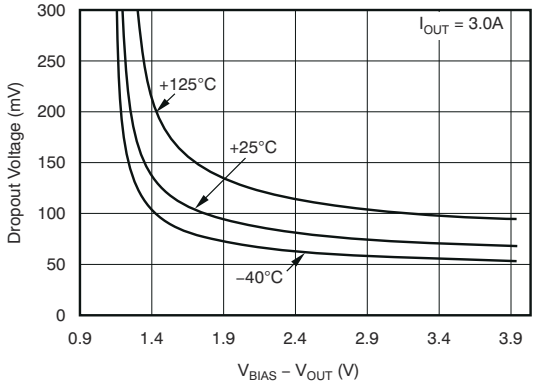


Figure 5-9. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

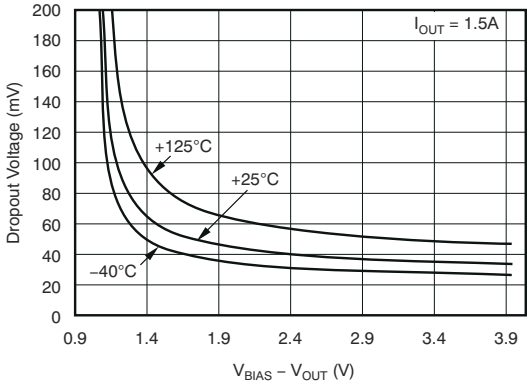
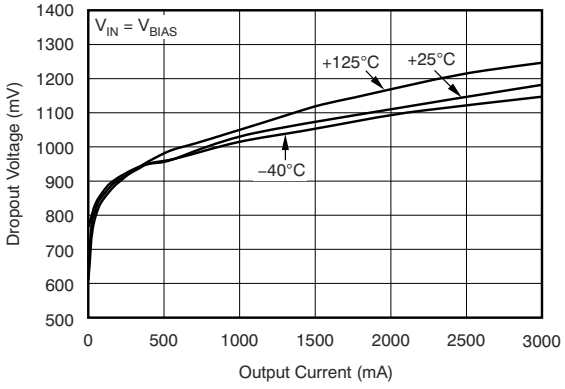
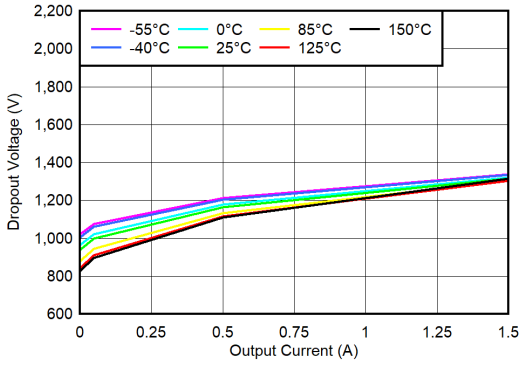


Figure 5-10. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)



Legacy chip

Figure 5-11. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)



New chip

Figure 5-12. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

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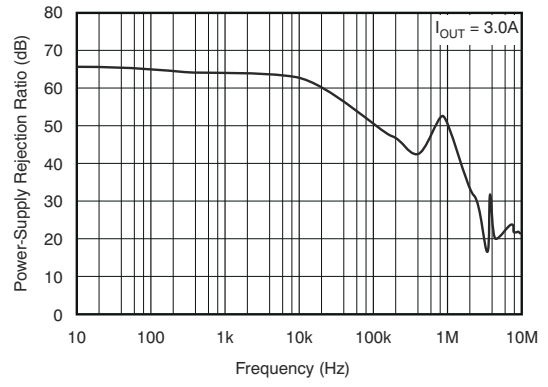
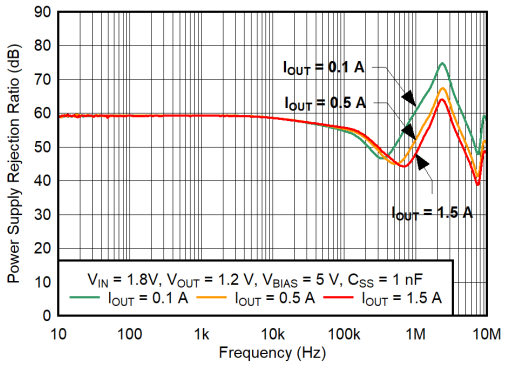
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



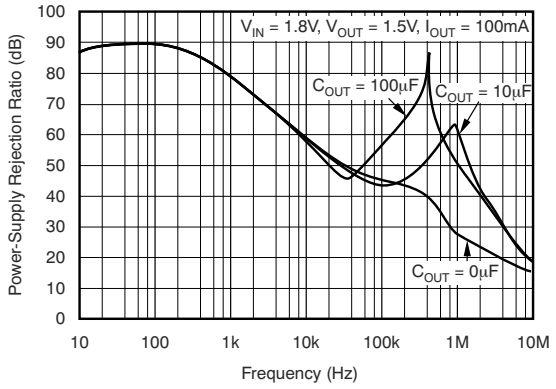
Legacy chip

Figure 5-13. V_{BIAS} PSRR vs Frequency



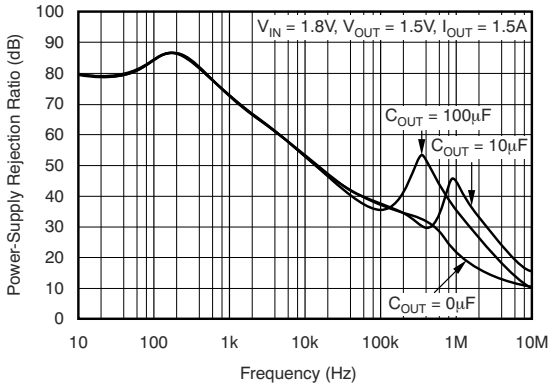
New chip

Figure 5-14. V_{BIAS} PSRR vs Frequency



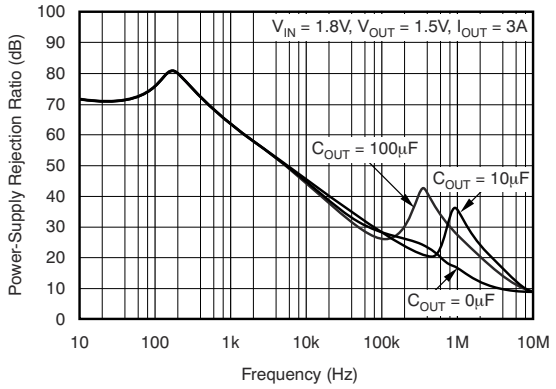
Legacy chip

Figure 5-15. V_{IN} PSRR vs Frequency



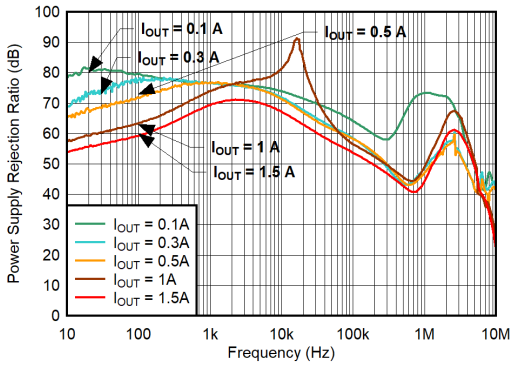
Legacy chip

Figure 5-16. V_{IN} PSRR vs Frequency



Legacy chip

Figure 5-17. V_{IN} PSRR vs Frequency



New chip

Figure 5-18. V_{IN} PSRR vs Frequency

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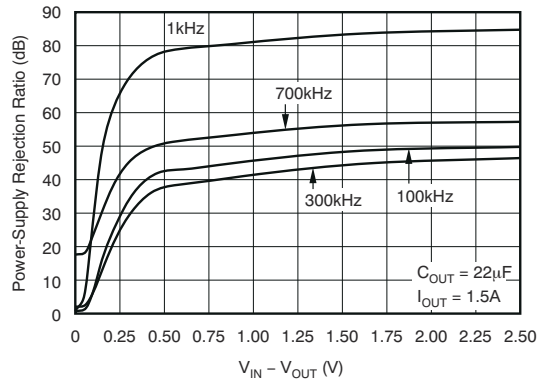
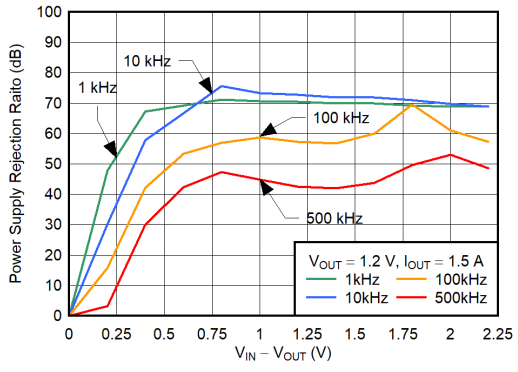
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



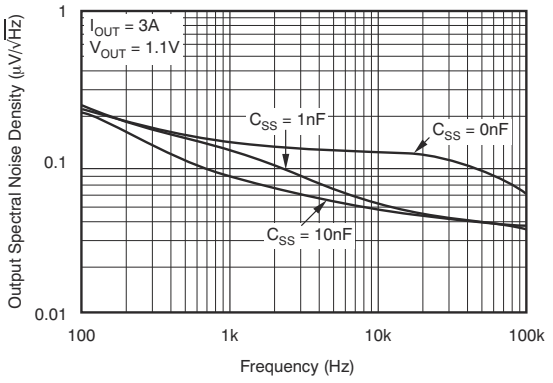
Legacy chip

Figure 5-19. V_{IN} PSRR vs V_{IN} – V_{OUT}



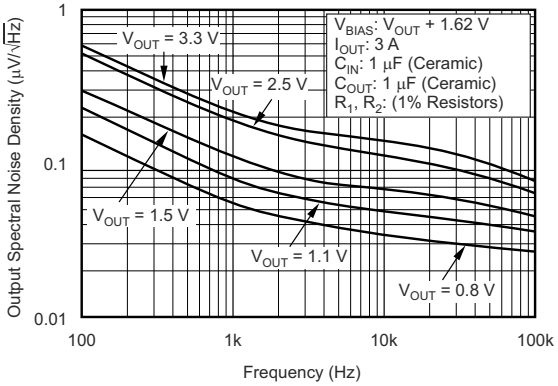
New chip

Figure 5-20. V_{IN} PSRR vs (V_{IN} – V_{OUT})



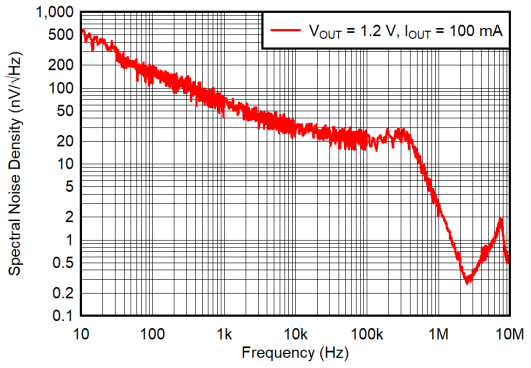
Legacy chip

Figure 5-21. Noise Spectral Density



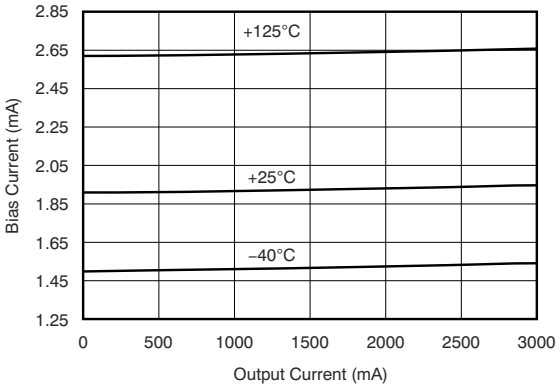
Legacy chip

Figure 5-22. Noise Spectral Density



New chip

Figure 5-23. Noise Spectral Density



Legacy chip

Figure 5-24. I_{BIAS} vs Output Current and Temperature

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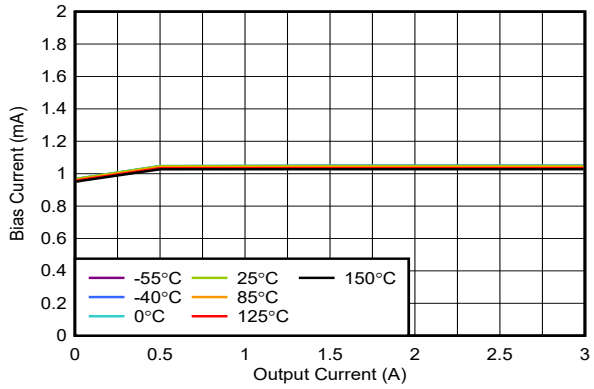
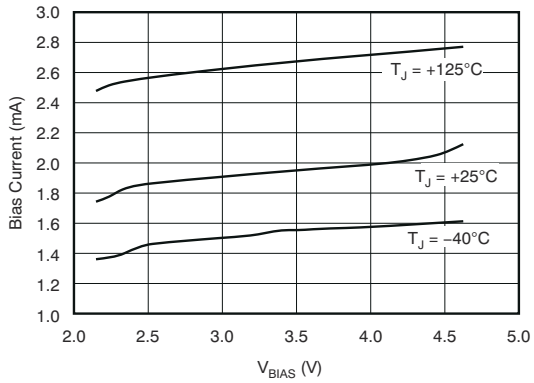
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



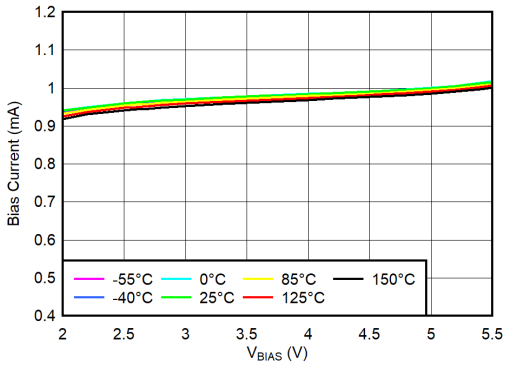
V_{IN} = 1.1V, V_{OUT} = 0.8V (new chip)

Figure 5-25. BIAS Pin Current vs Output Current and Temperature (T_J)



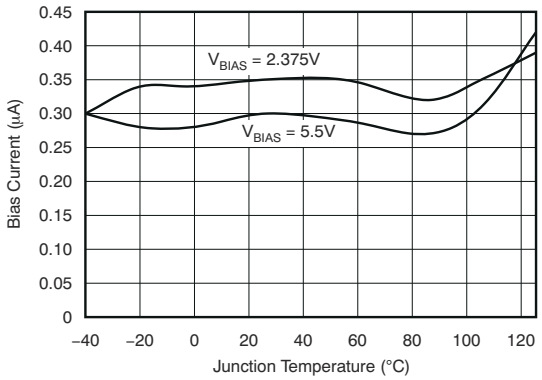
Legacy chip

Figure 5-26. I_{BIAS} vs V_{BIAS} and V_{OUT}



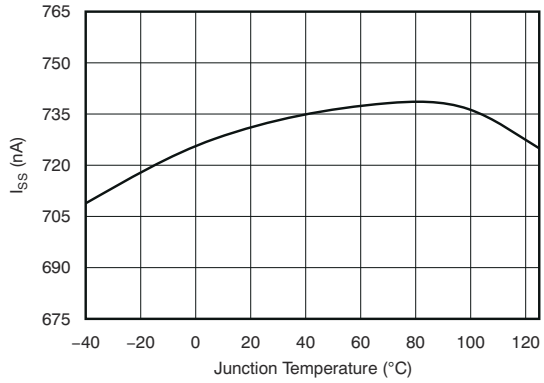
New chip

Figure 5-27. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)



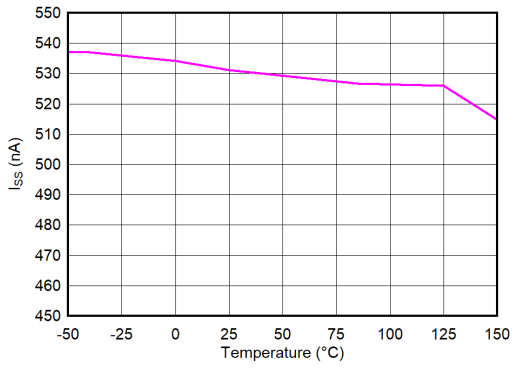
Legacy chip

Figure 5-28. I_{BIAS} Shutdown vs Temperature



Legacy chip

Figure 5-29. Soft-Start Charging Current (I_{SS}) vs Temperature



New chip

Figure 5-30. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)

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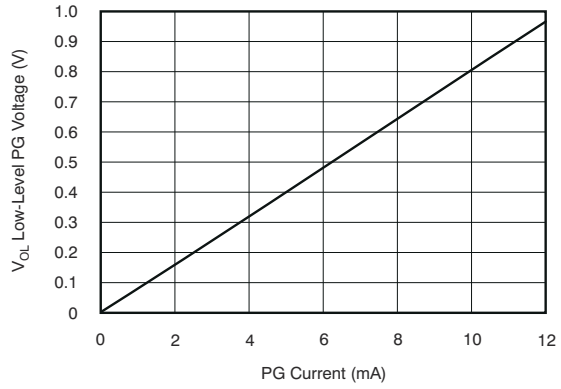
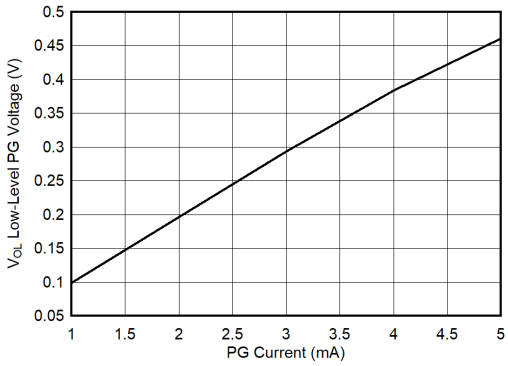
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



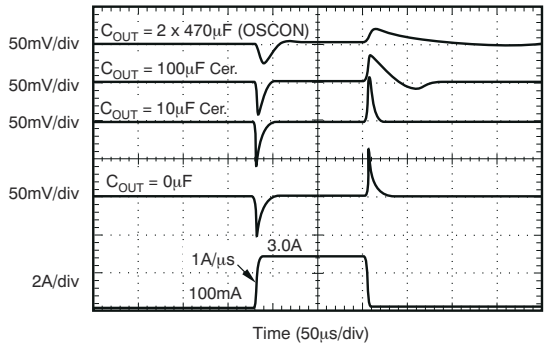
Legacy chip

Figure 5-31. Low-Level PG Voltage vs PG Current



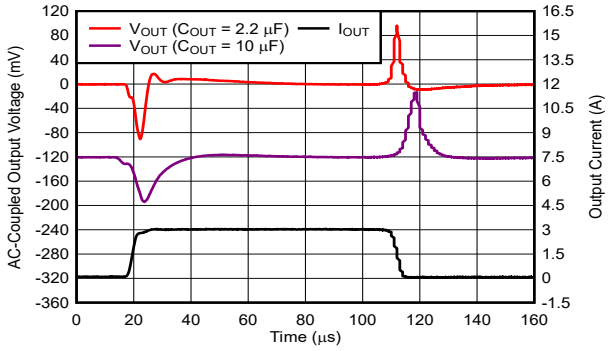
New chip

Figure 5-32. Low-Level PG Voltage vs Current



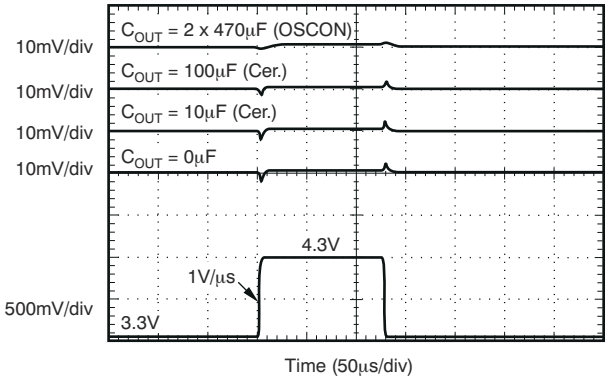
Legacy chip

Figure 5-33. Load Transient Response



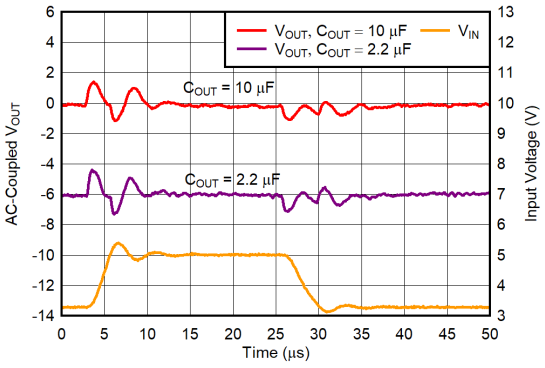
New chip

Figure 5-34. Load Transient Response



Legacy chip

Figure 5-35. V_{BIAS} Line Transient (3A)



New chip

Figure 5-36. V_{BIAS} Line Transient

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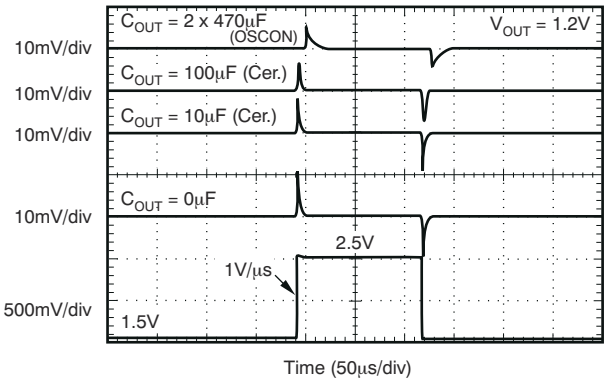
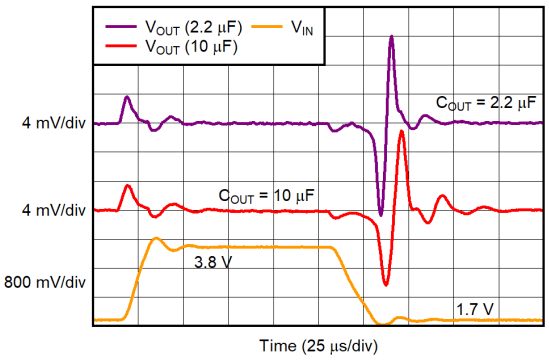
5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)



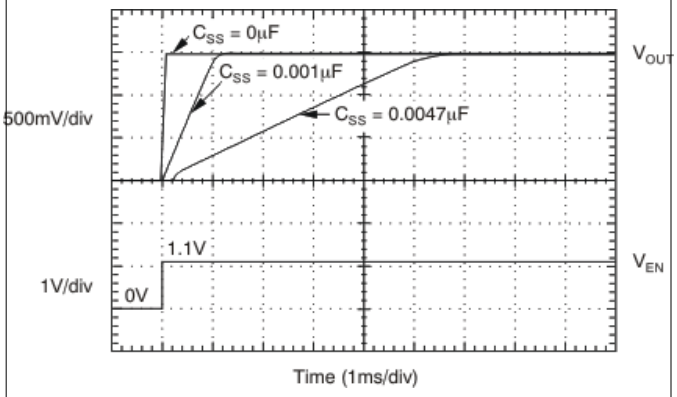
Legacy chip

Figure 5-37. V_{IN} Line Transient (3A)



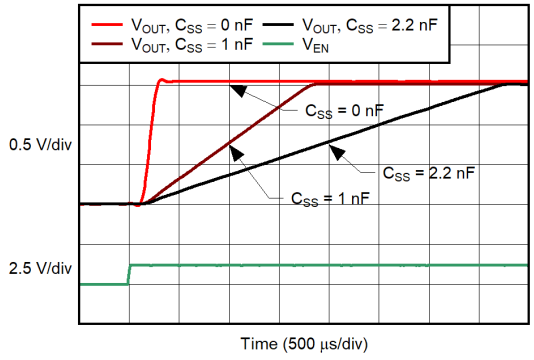
New chip

Figure 5-38. V_{IN} Line Transient



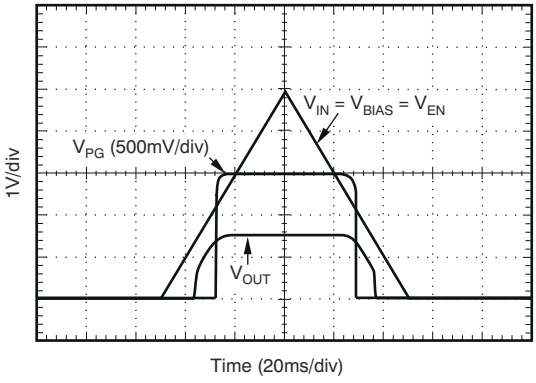
Legacy chip

Figure 5-39. Turn-On Response



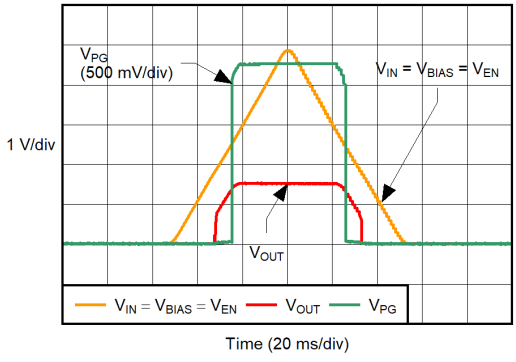
New chip

Figure 5-40. Turn-On Response



Legacy chip

Figure 5-41. Power-Up, Power-Down



New chip

Figure 5-42. Power-Up, Power-Down

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, C_{IN} = 1µF, C_{BIAS} = 1µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF for legacy chip and T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3V, V_{BIAS} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, and C_{OUT} = 10µF for new chip (unless otherwise noted)

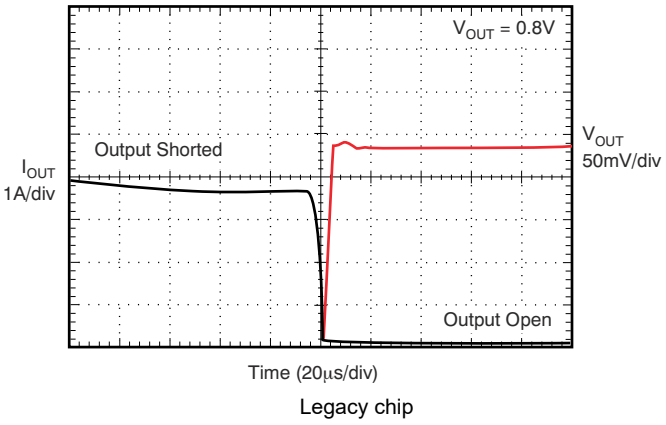

Figure 5-43. Output Short-Circuit Recovery

6 Detailed Description

6.1 Overview

The TPS74401 family of low-dropout regulators (LDOs) incorporates many features to ensure a wide range of uses. Hysteresis and deglitch on the EN input improve the ability to sequence multiple devices without worrying about false start-up. The soft-start is fully programmable and allows the user to control the start-up time of the LDO output. Hysteresis is also available on the PG comparator to confirm no false PG signals. The TPS74401 family of LDOs is designed for FPGAs, DSPs, and any other device that requires linear supply and sequencing.

6.2 Functional Block Diagrams

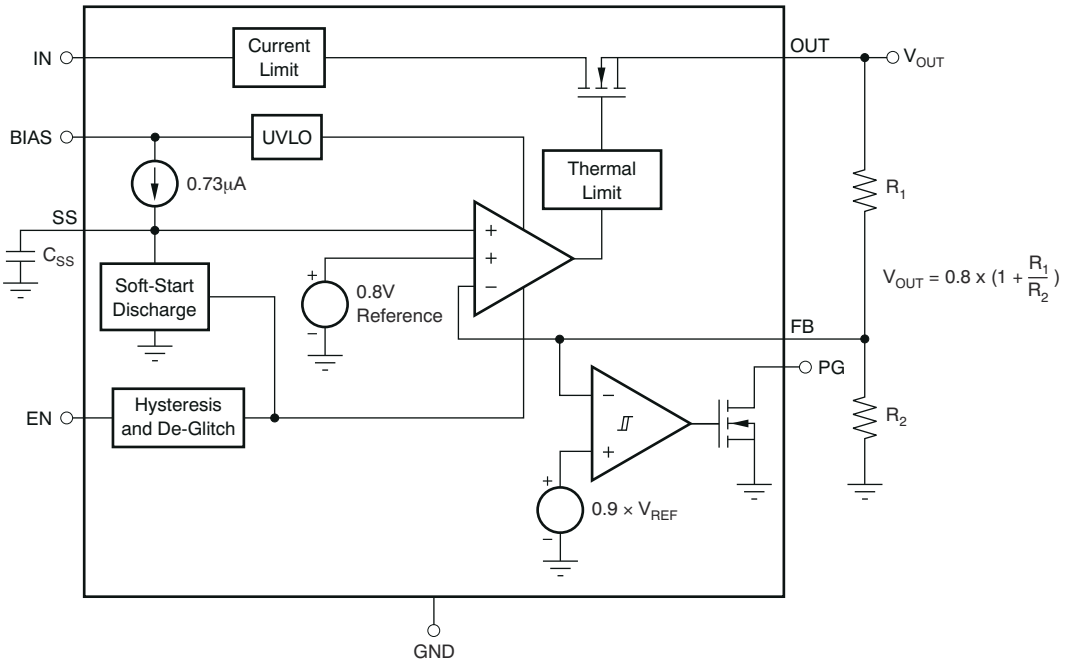

Figure 6-1. Legacy Chip Functional Block Diagram

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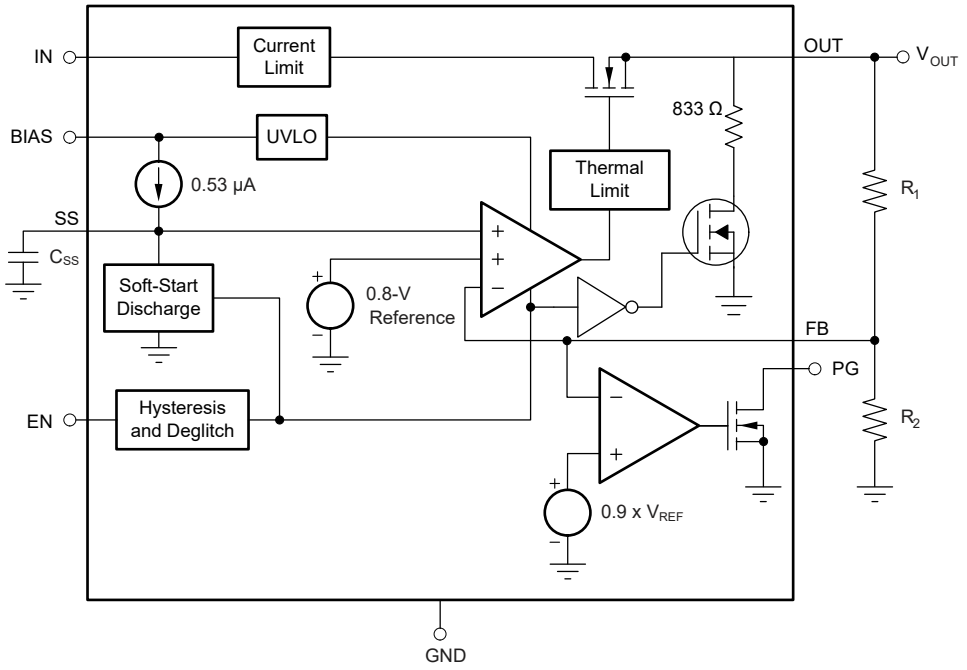

Figure 6-2. New Chip Functional Block Diagram

6.3 Feature Description

6.3.1 Enable, Shutdown

The enable (EN) pin is active high and compatible with standard digital signaling levels. V_{EN} lower than 0.4V turns the regulator off, whereas V_{EN} above 1.1V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow-ramping analog signals. This configuration allows the TPS74401 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50mV of hysteresis and a deglitch circuit to help avoid on-off cycling resulting from small glitches in the V_{EN} signal.

The enable threshold is typically 0.8V and varies with temperature and process variations. Temperature variation is approximately –1mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, use a fast rise-time signal to enable the TPS74401.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect EN as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

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6.3.2 Power-Good (VQFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5V or lower rail through an external pullup resistor. This pin requires at least 1.1V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than (V_{IT} + V_{HYS}). If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of the PG pin sink current is up to 1mA, thus the pullup resistor for PG must be in the range of 10kΩ to 1MΩ. PG is only provided on the VQFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

6.3.3 Internal Current Limit

The TPS74401 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 3.5A and maintain regulation. The current limit responds in approximately 10µs to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Figure 5-43 in the *Typical Characteristics* section for short-circuit recovery performance.

The internal current limit protection circuitry of the TPS74401 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74401 above the rated current degrades device reliability.

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 155°C for the legacy chip and 165°C for the new chip, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 30°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74401 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS74401 into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.
- The device is not operating in dropout.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

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6.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 6-1 shows the conditions that lead to the different modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ (V_{IN})	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + 1.62V$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}$ (V_{IN})	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + 1.62V$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 155°C$

6.5 Programming

6.5.1 Programmable Soft-Start

The TPS74401 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications to eliminate power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74401 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), the soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor can set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{\left[V_{OUT(nom)} \times C_{OUT}\right]}{I_{CL(min)}} \quad (2)$$

where

- $V_{OUT(nom)}$ is the nominal set output voltage as set by the user,
- C_{OUT} is the output capacitance,
- and $I_{CL(min)}$ is the minimum current limit for the device.

In applications where monotonic start-up is required, the soft-start time given by Equation 1 must be set to be greater than Equation 2.

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The maximum recommended soft-start capacitor is 0.015µF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit can not be able to fully discharge the soft-start capacitor when re-enabled. Soft-start capacitors larger than 0.015µF can be a problem in applications where the user must rapidly pulse the enable pin and also require the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Table 6-2 lists suggested soft-start capacitor values.

Table 6-2. Standard Capacitor Values for Programming the Soft-Start Time

C_{SS}	SOFT-START TIME (LEGACY CHIP)(1)	SOFT-START TIME (NEW CHIP)(1)
Open	0.1ms	0.25ms
470pF	0.5ms	0.7ms
1000pF	1ms	1.5ms
4700pF	5ms	7ms
0.01µF	10ms	15ms
0.015µF	16ms	22.6ms

(1) $$t_{SS}(s) = 0.8 \times C_{SS}(F) \div I_{SS}$$

6.5.2 Sequencing Requirements

The device can have V_{IN}, V_{BIAS}, and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} and V_{BIAS} are present is preferred, and can be accomplished using a digital output from a processor or supply supervisor. An analog signal from an external RC circuit, as shown in Figure 6-3, can also be used as long as the delay time is long enough for V_{IN} and V_{BIAS} to be present.

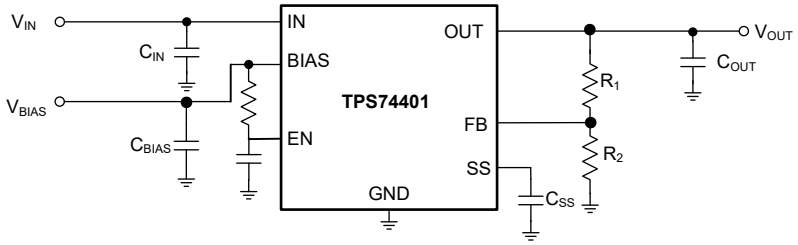

Figure 6-3. Soft-Start Delay Using an RC Circuit on Enable

If a signal is not available to enable the device after IN and BIAS, simply connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1V and the ramp rate of V_{IN} and V_{BIAS} is faster the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply less the dropout voltage until the set output voltage is reached. If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS74401 belongs to a family of ultra-low dropout regulators that feature soft-start. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low output voltages with low V_{IN} to V_{OUT} headroom.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little affect on loop stability. This architecture allows the TPS74401 to be stable with any capacitor ≥ 2.2µF. Transient response is better than PMOS topologies, particularly for low V_{IN} applications.

The TPS74401 features a programmable, voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and de-glitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

7.1.1 Input, Output, and Bias Capacitor Requirements

The legacy chip of TPS74401 does not require any output capacitor for stability, however, the new chip of TPS74401 is designed to be stable for all available types and values of output capacitors ≥ 2.2µF. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, of any type or value. This flexibility is a result of a remarkable control loop that confirms that the device is stable independent of the output capacitance.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7µF. Use good quality, low-ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close to the pins as possible for optimum performance and to help confirm stability.

7.1.2 Transient Response

The TPS74401 is designed to have transient response within 5% for most applications. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time; see Figure 5-33 in the *Typical Characteristics* section. Because the legacy chip is stable without an output capacitor and the new chip is stable with output capacitors ≥ 2.2µF, many applications can allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power can be sufficient to meet the transient requirements of the application. This design reduces the total cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

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7.1.3 Dropout Voltage

The TPS74401 offers industry-leading dropout performance, making the device excellent for high-current, low V_{IN} and low V_{OUT} applications. The extremely low dropout of the TPS74401 also allows the device to be used in place of a dc/dc converter and also achieve good efficiencies. Equation 3 provides a quick estimate of the efficiencies.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times \left(I_{IN} + I_Q\right)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} > > I_Q \tag{3}$$

This efficiency allows users to redesign the power architecture to achieve a small, simple, and low-cost option.

There are two different specifications for dropout voltage with the TPS74401. The first specification (see Figure 7-12) is referred to as *V_{IN} Dropout* and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62V above V_{OUT}; for example, when V_{BIAS} is powered by a 3.3V rail with 5% tolerance and with V_{OUT} = 1.5V. If V_{BIAS} is higher than (3.3V × 0.95) or V_{OUT} is less than 1.5V, V_{IN} dropout is less than specified.

The second specification (see Figure 7-13) is referred to as *V_{BIAS} Dropout* and is for users who wish to have V_{BIAS} < V_{IN} + 1.62V. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor and therefore must be greater than V_{OUT} + V_{DO} (V_{BIAS}). Because of this usage, IN and BIAS tied together easily consume excessive power. Pay attention and do not exceed the power rating of the IC package.

7.1.4 Output Noise

The TPS74401 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001µF soft-start capacitor, the output noise is reduced by half and is typically 19µV_{RMS} for a 1.2V output (100Hz to 100kHz). Noise is a function of the set output voltage because most of the output noise is generated by the internal reference.

The RMS noise with a 0.001µF soft-start capacitor is given in Equation 4 for the legacy chip and Equation 5 for the new chip.

$$V_N(\mu V_{RMS}) = 16\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{4}$$

$$V_N(\mu V_{RMS}) = 20\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{5}$$

The low output noise of the TPS74401 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

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7.2 Typical Applications

7.2.1 Setting the TPS74401

Figure 7-1 shows a typical application circuit for the TPS74401.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 7-1. Table 7-1 lists sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 must be ≤ 4.99kΩ.

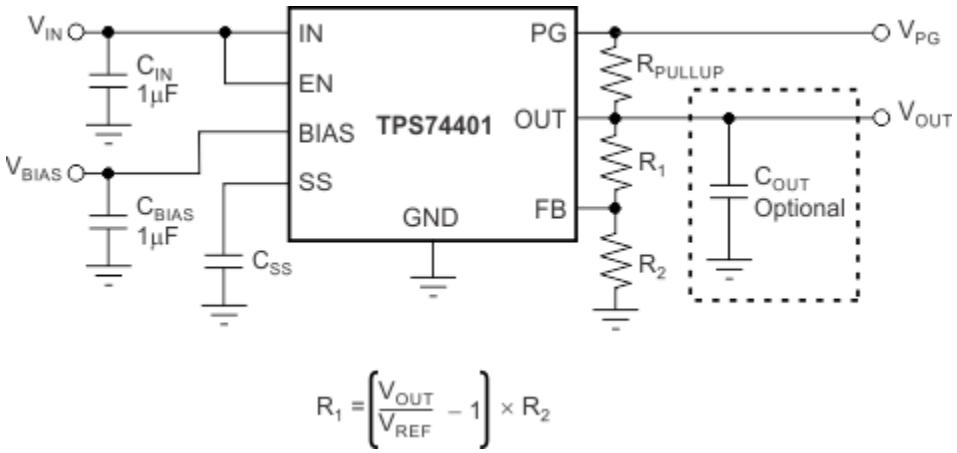

Figure 7-1. Typical Application Circuit for the TPS74401

Table 7-1. Standard 1% Resistor Values for Programming the Output Voltage

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)(1)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1 \div R_2)$

Note

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50µA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10kΩ.

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7.2.1.1 Design Requirements

The design goals are V_{IN} = 1.8V, V_{OUT} = 1.5V, and I_{OUT} = 2A maximum. The design optimizes transient response while meeting a 1ms start-up time with a start-up dominated by the soft-start feature. The input supply comes from a supply on the same circuit board. The available system rails for V_{BIAS} are 2.7V, 3.3V, and 5V.

The design space consists of C_{IN}, C_{OUT}, C_{BIAS}, C_{SS}, V_{BIAS}, R_1, R_2, and R_3, and the circuit is from Figure 7-1.

This example uses a V_{IN} of 1.8V, with a V_{BIAS} of 2.5V.

7.2.1.2 Detailed Design Procedure

The first step for this design is to examine the maximum load current along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 3A, the input dropout voltage of the TPS74401 family is a maximum of 240mV over temperature. As a result, the dropout headroom is sufficient for operation over both input and output voltage accuracy.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is (1.8V – 1.5V), giving a V_{DROP} = 300mV. The power dissipated can than be estimated by the equation $P_{DISS} = I_{L(max)} \times V_{DROP}$ = approximately 600mW. This calculation gives an efficiency of nearly 83.3% by using Equation 3.

When the power dissipated in the linear regulator is known, the corresponding junction temperature increase can be calculated. To estimate the junction temperature increase above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information, see the *Thermal Information* table. For this example, using the KTW package, the junction temperature rise is calculated to be 21.2°C. The maximum junction temperature increase is calculated by adding the junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 46.2°C. Keep in mind that the junction temperature must be less than 125°C for reliable operation. Additional ground planes, added thermal vias, and air flow all help to improve the thermal transfer characteristics of the system.

The next step is to determine the bias voltage or if a separate source is needed for the bias voltage. Because V_{IN} is less than V_{OUT} plus the V_{BIAS} dropout, V_{BIAS} must be an independent supply. $V_{BIAS} = V_{OUT} + 1.62V$ = 3.12V; the system has a 3.3V rail to use for this supply and also to provide some limited headroom for V_{BIAS}. The 5V rail is a better choice to improve the performance of the LDO, so the 5V rail is used.

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7.2.1.3 Application Curves

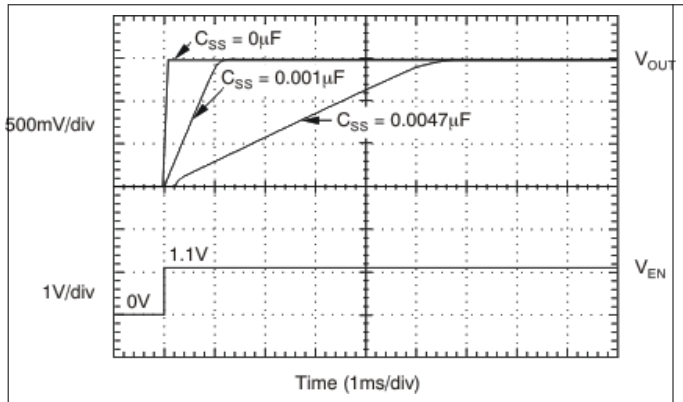

Figure 7-2. Turn-On Response

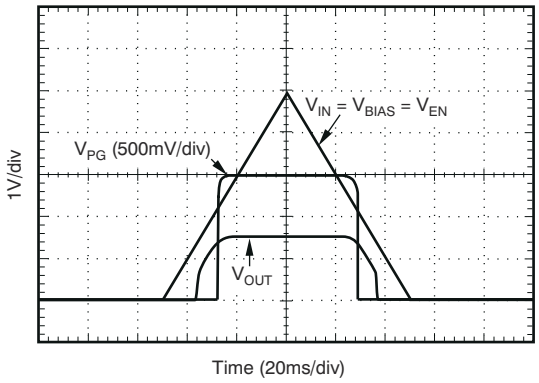

Figure 7-3. Power-Up, Power-Down

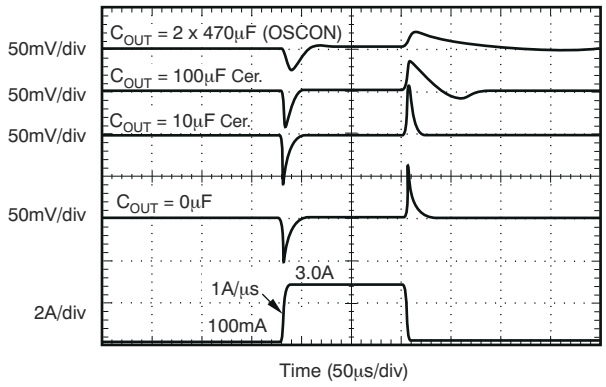

Figure 7-4. Load Transient Response

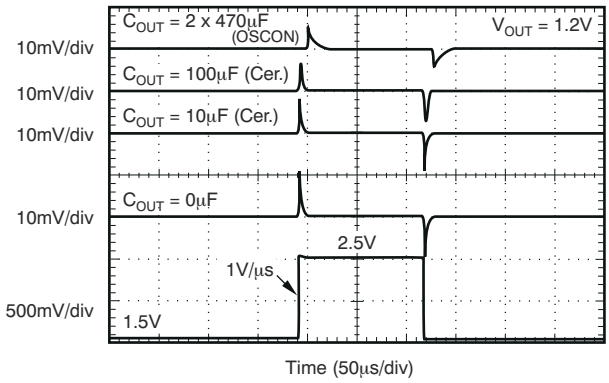

Figure 7-5. V_{IN} Line Transient (3A)

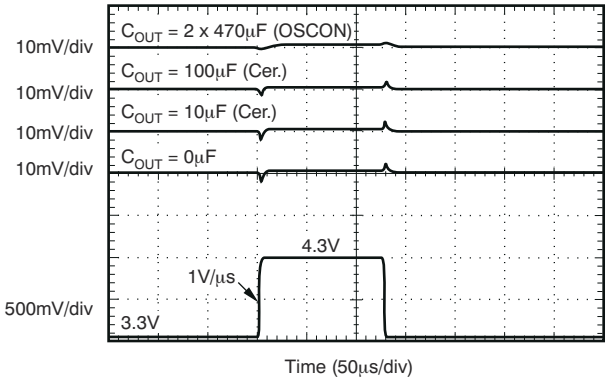

Figure 7-6. V_{BIAS} Line Transient (3A)

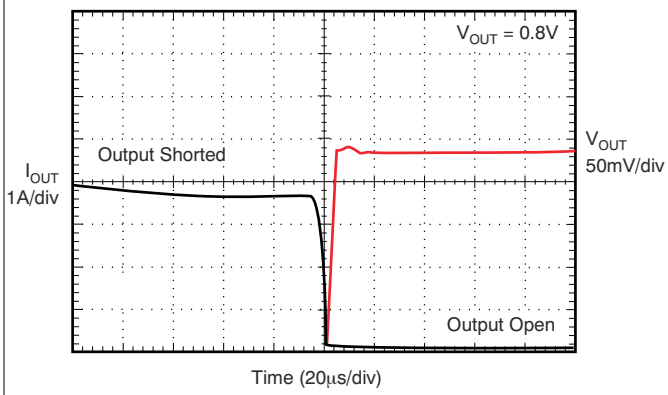

Figure 7-7. Output Short-Circuit Recovery

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7.2.1.3 Application Curves (continued)

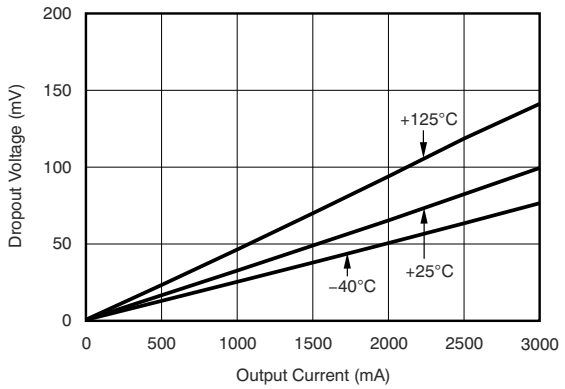

Figure 7-8. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

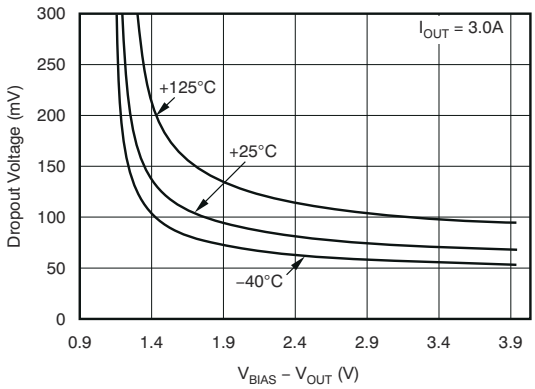

Figure 7-9. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

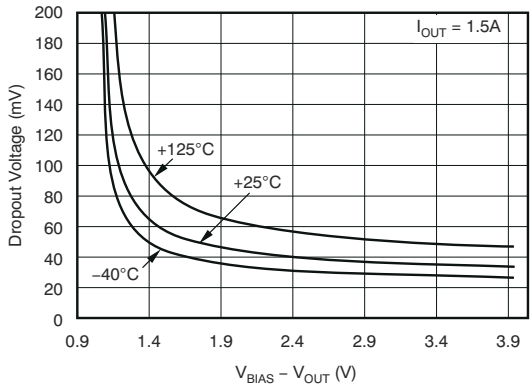

Figure 7-10. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

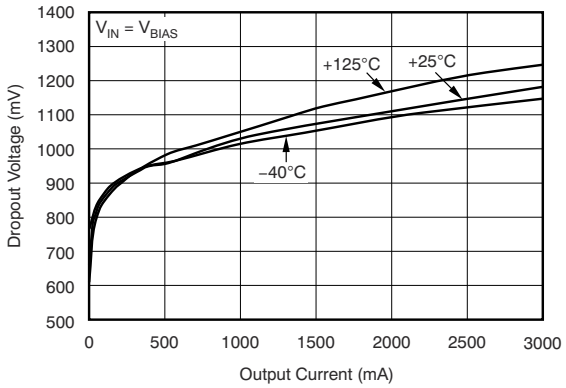

Figure 7-11. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

7.2.2 Using an Auxiliary Bias Rail

Figure 7-12 shows a typical application of the TPS74401 using an auxiliary bias rail. The auxiliary bias rail allows for the designer to specify the system to have a low V_{DO}. The bias rail supplies the error amplifier with a higher supply voltage, increasing the voltage that can be applied to the gate of the pass device.

V_{BIAS} must be at least V_{OUT} + 1.62V.

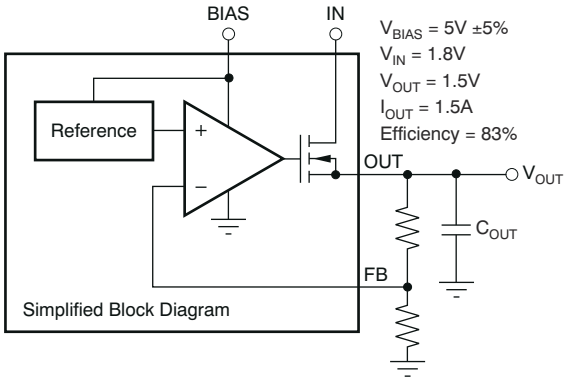

Figure 7-12. Typical Application of the TPS74401 Using an Auxiliary Bias Rail

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7.2.3 Without an Auxiliary Bias

The TPS74401 is capable of operating without a bias rail if $V_{IN} \geq V_{OUT} + V_{DO}$ (V_{BIAS}). Additional capacitance is advised for this scenario, with at least 4.7µF of capacitance near the input pin. Figure 7-13 shows a typical application of the TPS74401 without an auxiliary bias.

If using the TPS74401 in this situation and under high load conditions, check that the printed circuit board (PCB) provides adequate thermal handling capabilities to keep the device in the recommended operating range. See the *Power Supply Recommendations* section for more information.

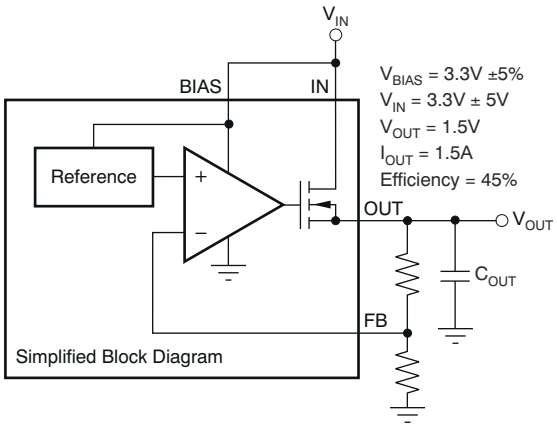

Figure 7-13. Typical Application of the TPS74401 Without an Auxiliary Bias

7.3 Power Supply Recommendations

The TPS74401 is designed to operate from an input voltage between 1.1V to 5.5V, provided the bias rail is at least 1.62V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low output impedance power supply directly to the IN pin of the TPS74401. This supply must have at least 1µF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

An excellent layout greatly improves transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve peak transient performance and accuracy, connect the top side of R_1 in Figure 7-1 as close as possible to the load. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

7.4.1.1 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and verifying reliable operation.

Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

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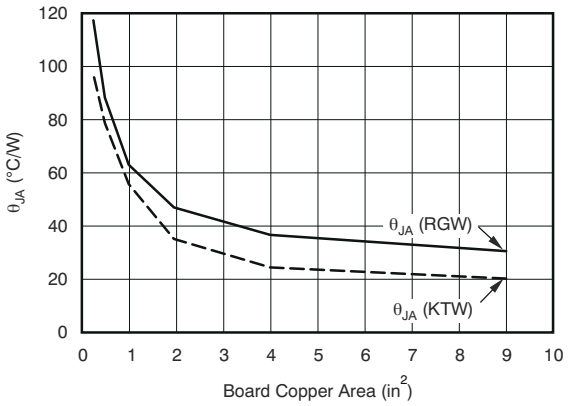
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW, RGR) packages, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or left floating; however, the pad must attach to an appropriate amount of copper PCB area to verify that the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. Connect that tab to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be estimated using Equation 7:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{7}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking is estimated using Figure 7-14.



θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

Figure 7-14. θ_{JA} versus Board Size

Figure 7-14 shows the variation of θ_{JA} as a function of ground plane copper area in the board. Figure 7-14 is intended only as a guideline to demonstrate the affects of heat spreading in the ground plane; do not use Figure 7-14 to estimate actual thermal performance in real application environments.

Note

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Thermal Information* table.

7.4.1.2 Thermal Considerations

A better method of estimating the thermal measure comes from using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with the corresponding formulas given in Equation 8.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \tag{8}$$

where

- P_D is the power dissipation shown by Equation 8,
- T_T is the temperature at the center-top of the IC package, and
- T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (see Figure 7-15).

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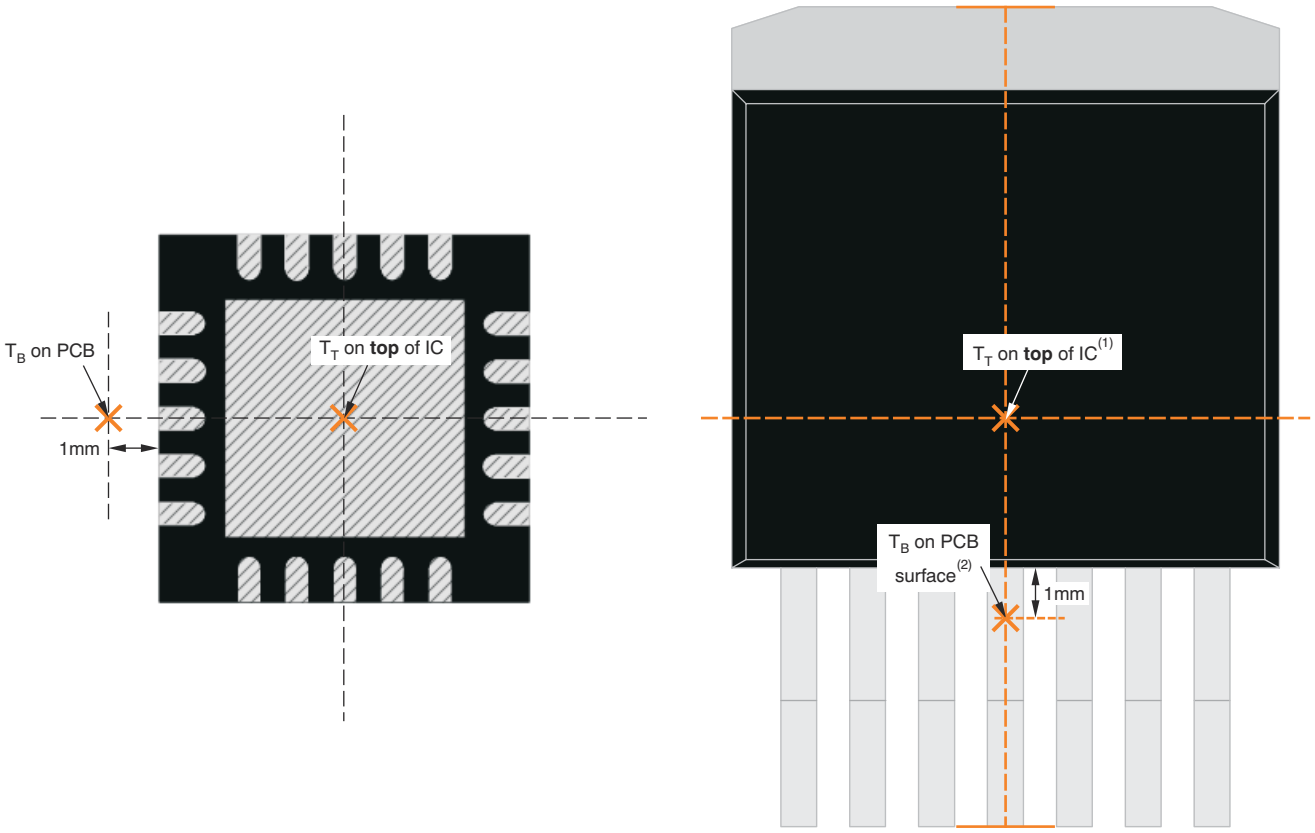
Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note.



(a) Example RGW (QFN) Package Measurement

(b) Example KTW (DDPAK) Package Measurement

A. T_T is measured at the center of both the X- and Y-dimensional axes.
B. T_B is measured ***below*** the package lead **on the PCB surface**.

Figure 7-15. Measuring Points for T_T and T_B

Compared with θ_{JA}, the thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size, but do have a small dependency on board size and layout. Figure 7-16 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Referring to Figure 7-16, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point symmetric to an IC center. In the KTW package, for example (see Figure 7-15), silicon is not beneath the measuring point of T_T which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point symmetry, device heat distribution on the PCB is not point symmetric either, so that Ψ_{JB} has a greater dependency on board size and layout.

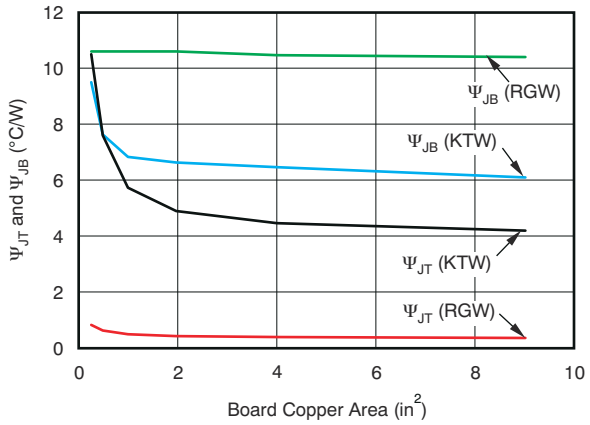


Figure 7-16. Ψ_{JT} and Ψ_{JB} versus Board Size

For a more detailed description of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note. Also, see the *IC Package Thermal Metrics* application note for further information.

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7.4.2 Layout Example

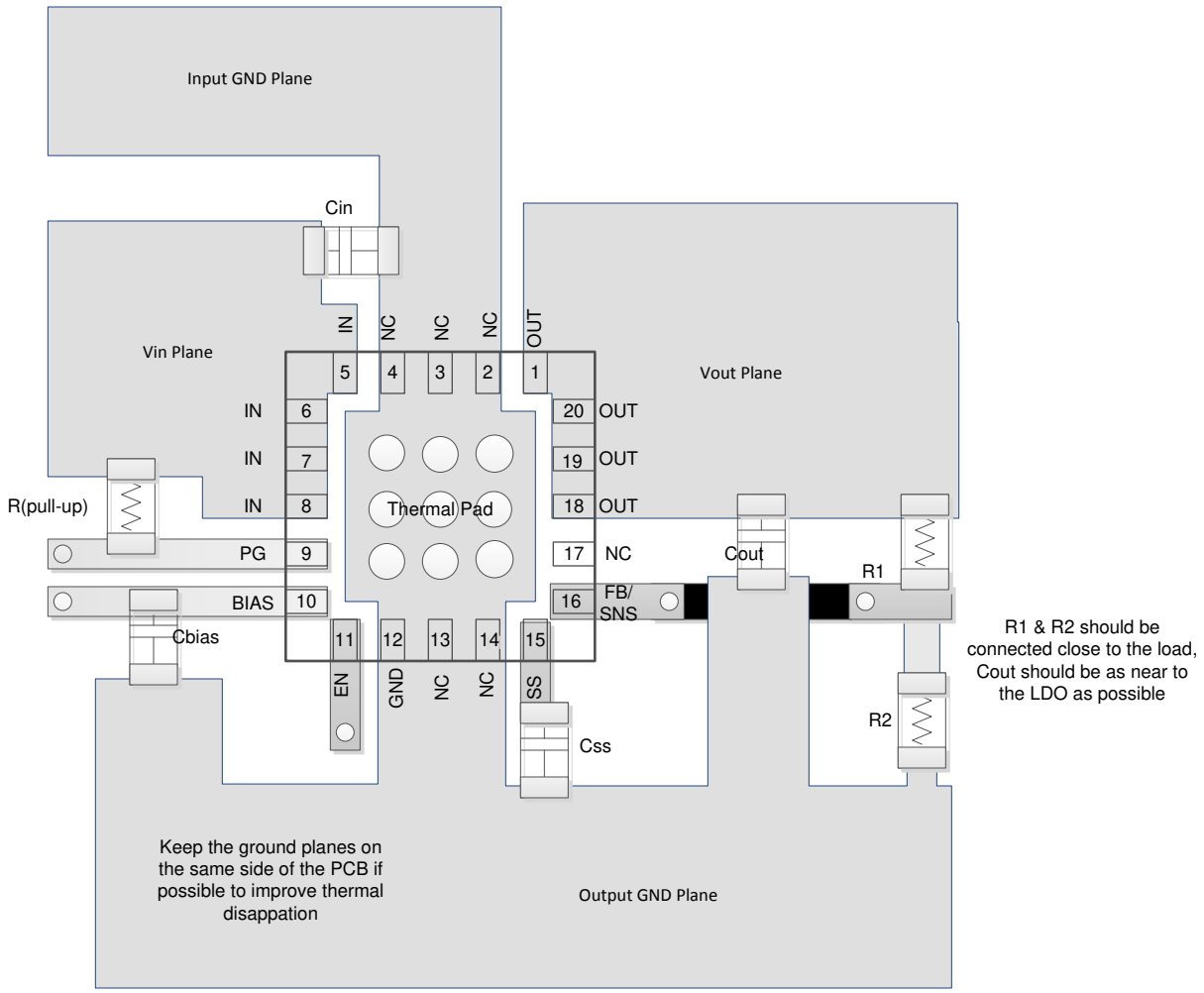

Figure 7-17. Layout Schematic (VQFN Packages)

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *6A Current-Sharing Dual LDO* design guide
- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *IC Package Thermal Metrics* application note
- Texas Instruments, *TPS74401EVM-118 Evaluation Module* user's guide

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS74401**yyyzM3**	**yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Device Support

8.2.1 Development Support

8.2.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS74401. The TPS74401EVM-118 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.2.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS74401 is available through the product folders under *Tools & Software*.

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (November 2024) to Revision T (April 2025)	Page
• Units for the New chip *Load Regulation* have been fixed to %/mA for 0mA≤ I_{OUT} ≤ 50mA test condition	5
• Units for the New chip *Load Regulation* have been fixed to %/A for 50mA ≤ I_{OUT} ≤ 3A test condition	5

Changes from Revision R (April 2017) to Revision S (November 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added notation of legacy chip and new chip throughout document	1
• Changed *Features* and *Applications* sections	1
• Changed the *Device Information* table to *Package Information*	1
• Changed *Typical Characteristics* section: Identified legacy chip plots and added new chip plots	8
• Changed *Output Noise* section	22

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74401KTWR	NRND	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TPS74401
TPS74401KTWR.A	NRND	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TPS74401
TPS74401KTWRG3	NRND	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TPS74401
TPS74401RGRR	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12KA
TPS74401RGRR.A	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12KA
TPS74401RGRT	Obsolete	Production	VQFN (RGR) | 20	-	-	Call TI	Call TI	-40 to 125	12KA
TPS74401RGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWR.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWRG4	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWRM3	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWRM3.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWT.A	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401
TPS74401RGWTG4	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS74401 :

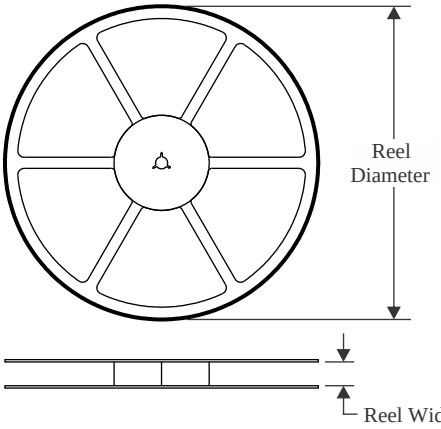
- Enhanced Product : TPS74401-EP

NOTE: Qualified Version Definitions:

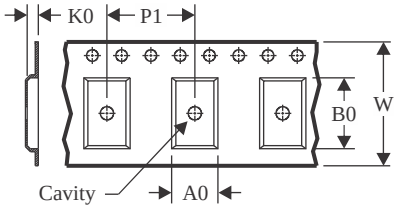
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

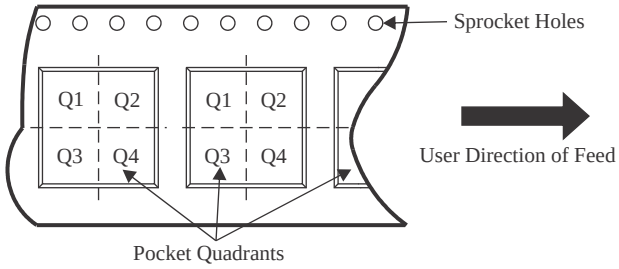


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

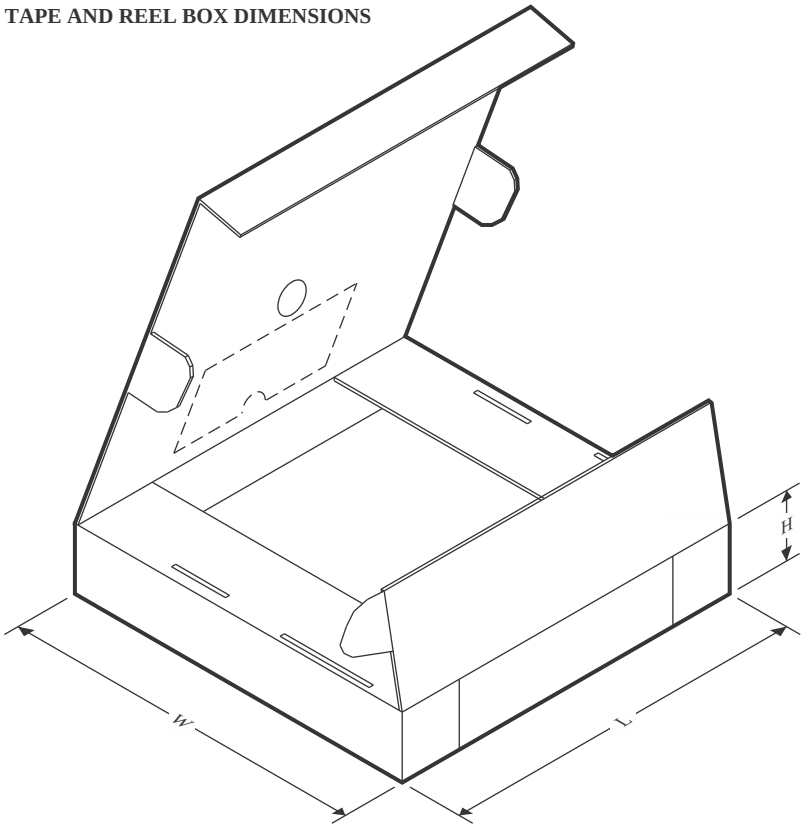
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74401KTWR	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS74401RGRR	VQFN	RGR	20	3000	330.0	12.4	3.8	3.8	1.1	8.0	12.0	Q1
TPS74401RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74401RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74401RGWRM3	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74401RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74401KTWR	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0
TPS74401RGRR	VQFN	RGR	20	3000	338.0	355.0	35.0
TPS74401RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74401RGWR	VQFN	RGW	20	3000	360.0	360.0	36.0
TPS74401RGWRM3	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74401RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

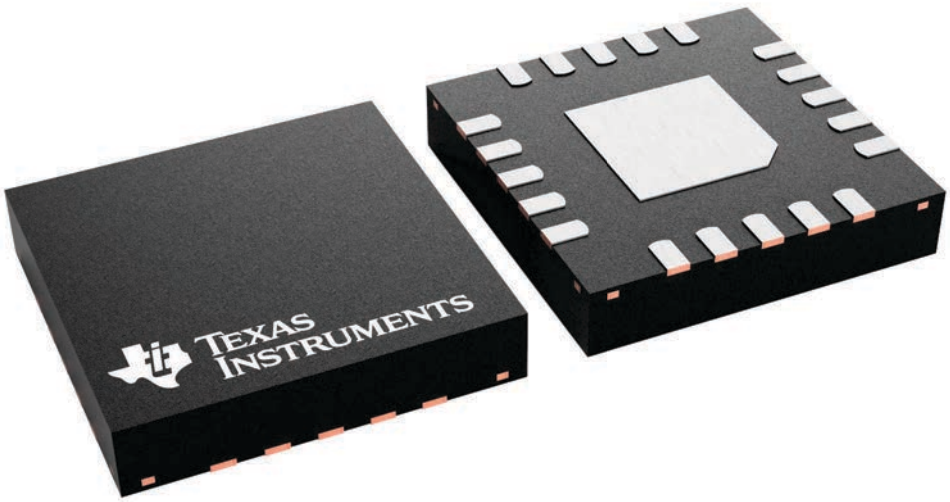
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



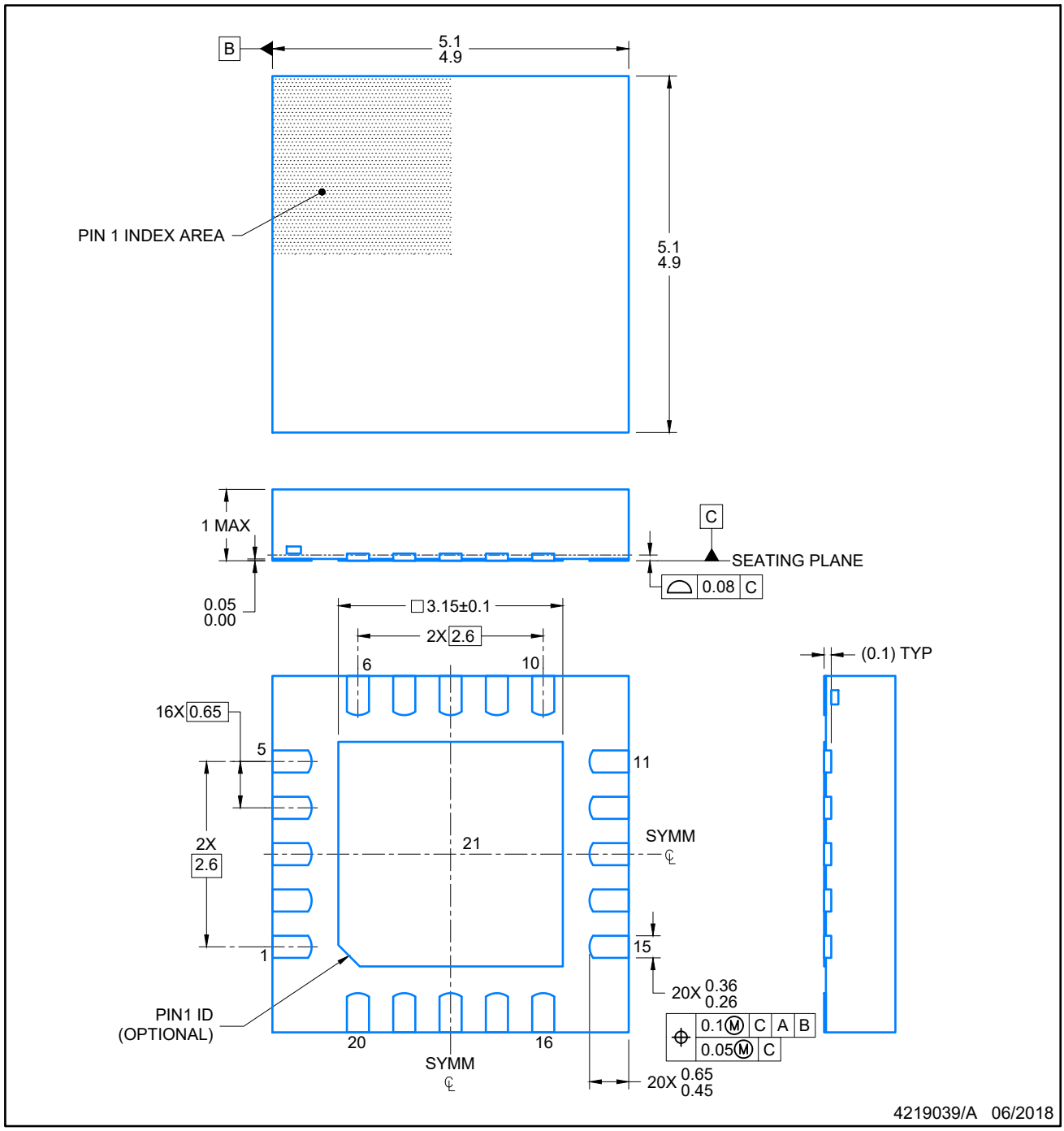
4227157/A

PACKAGE OUTLINE

RGW0020A

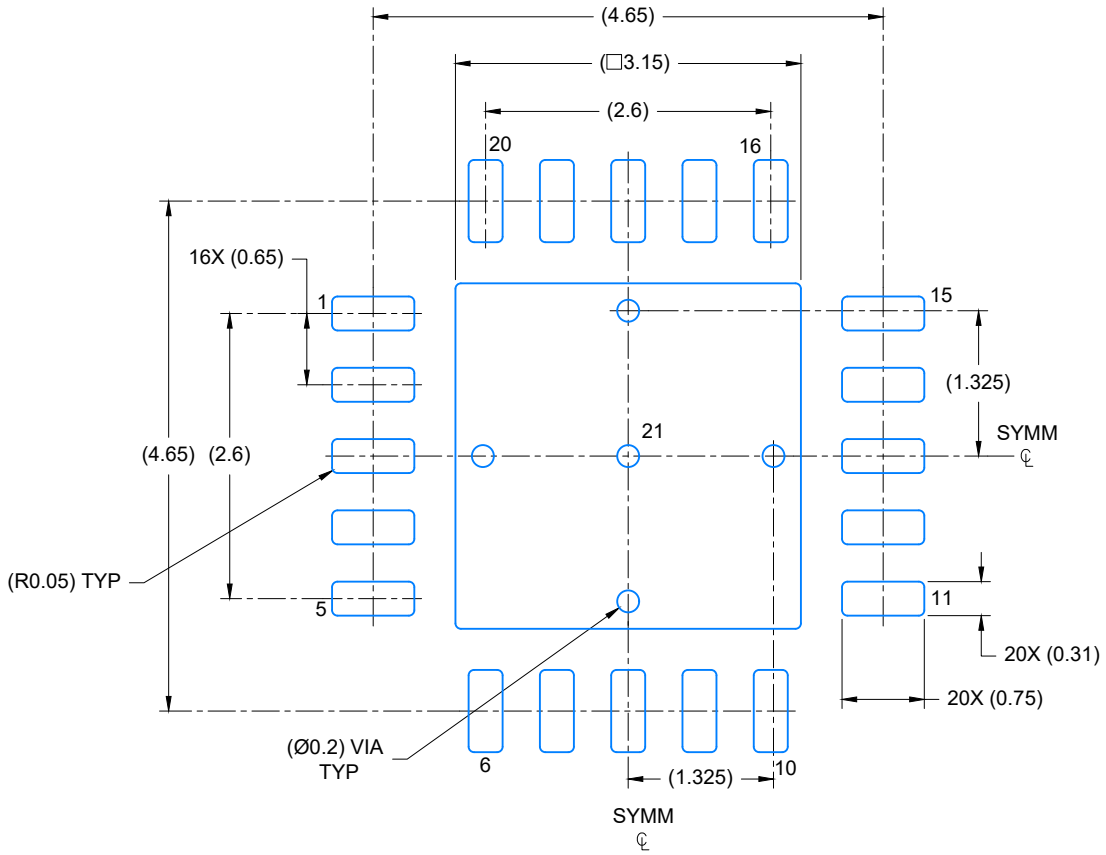
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



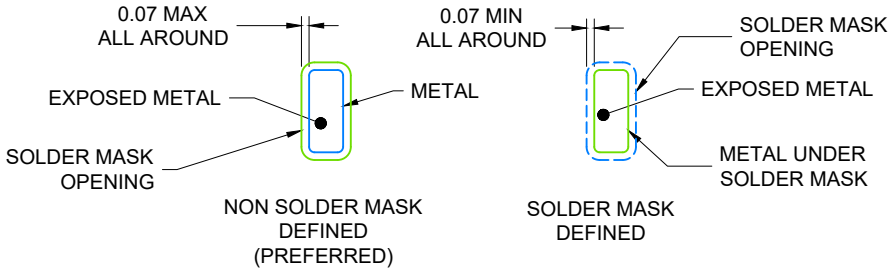
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

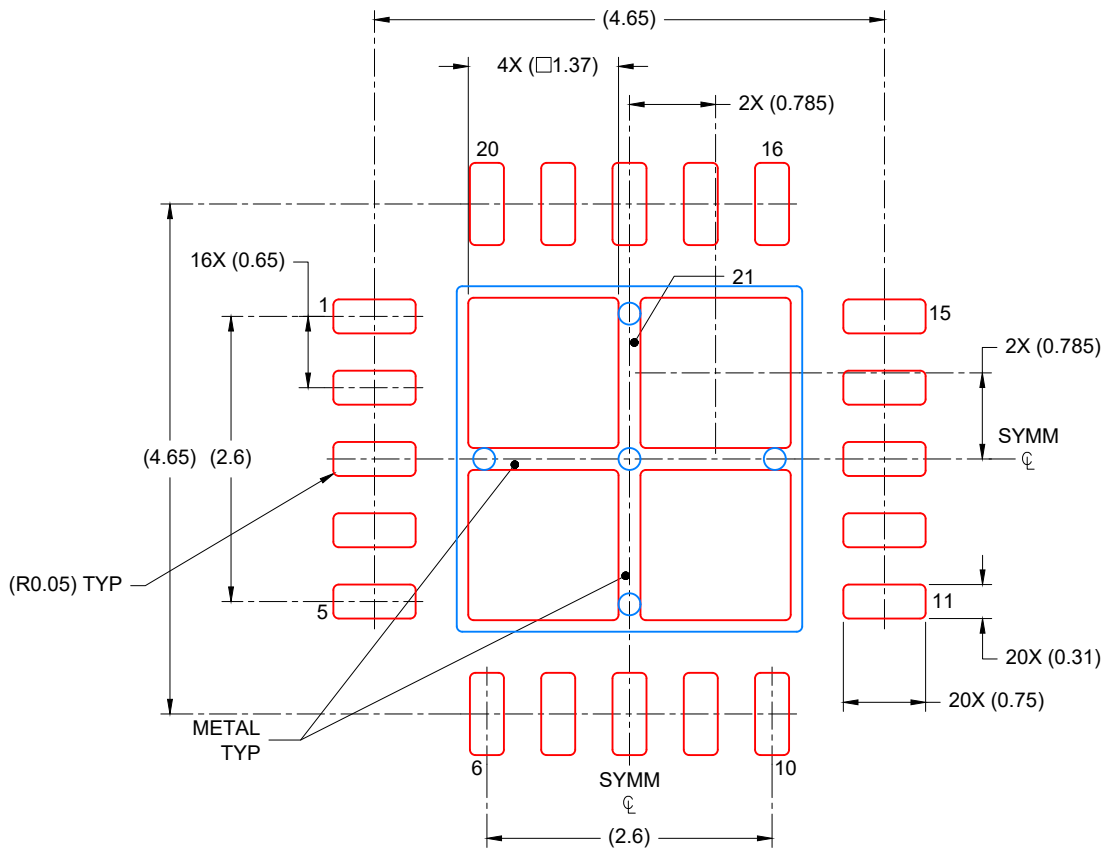


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

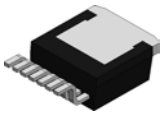
EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

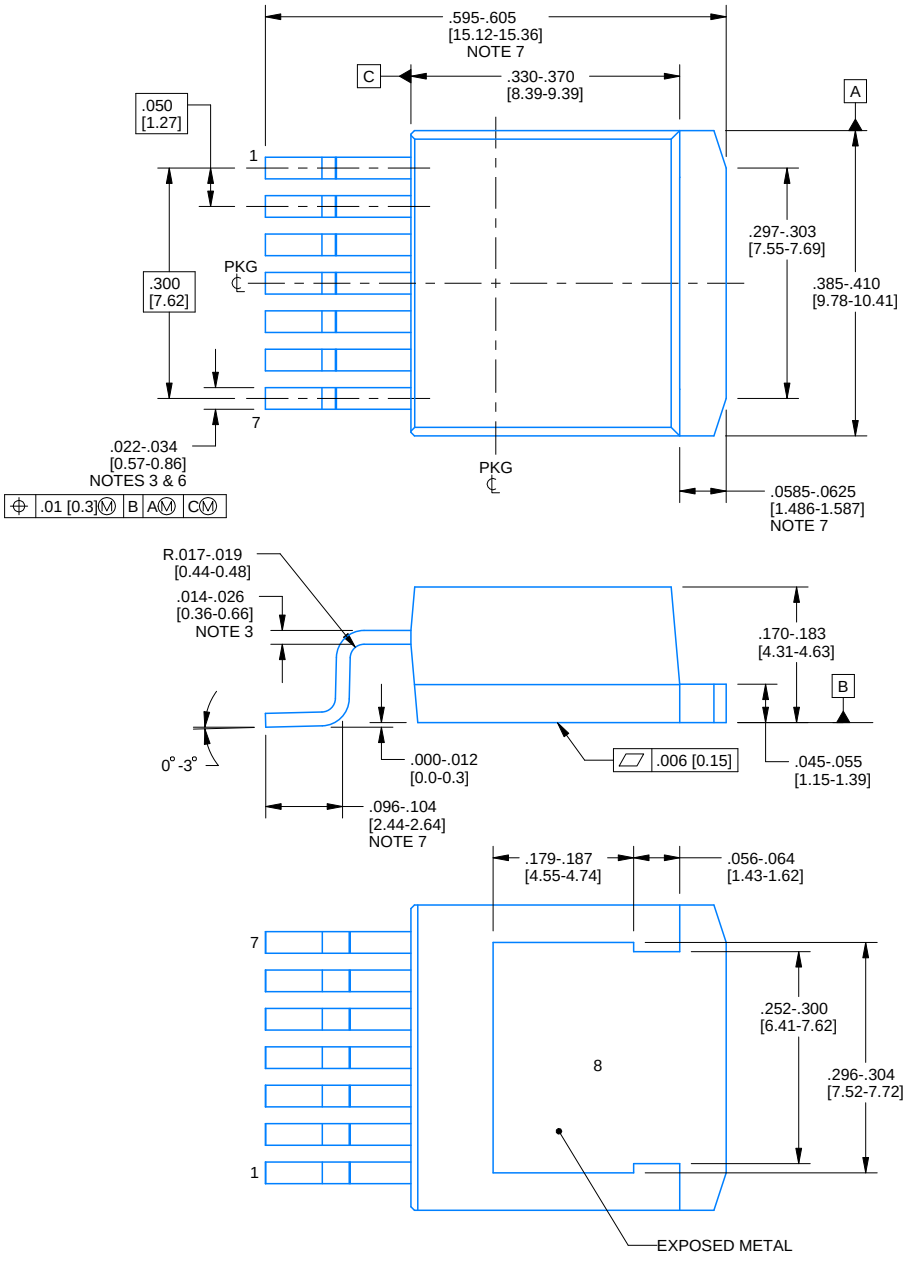
KTW0007A



PACKAGE OUTLINE

TO-263 - 5 mm max height

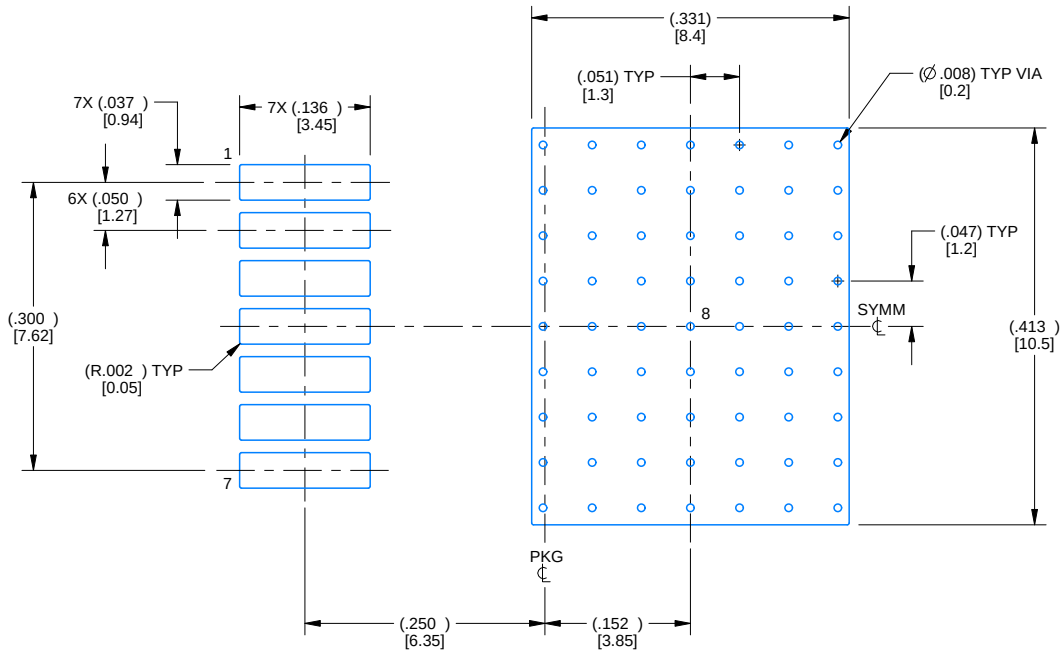
TRANSISTOR OUTLINE



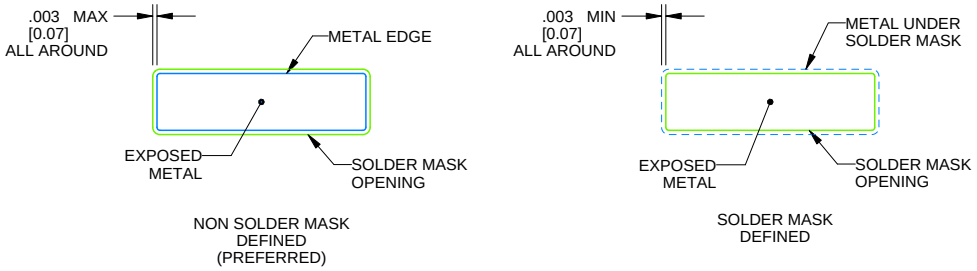
4232469/A 11/2025

NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead width and height dimensions apply to the plated lead.
4. Leads are not allowed above the Datum B.
5. Stand–off height is measured from lead tip with reference to Datum B.
6. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum bdimension by more than 0.003”.
7. Falls within JEDEC MO–169 with the exception of the dimensions indicated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X



SOLDER MASK DETAILS

4232469/A 11/2025

NOTES: (continued)

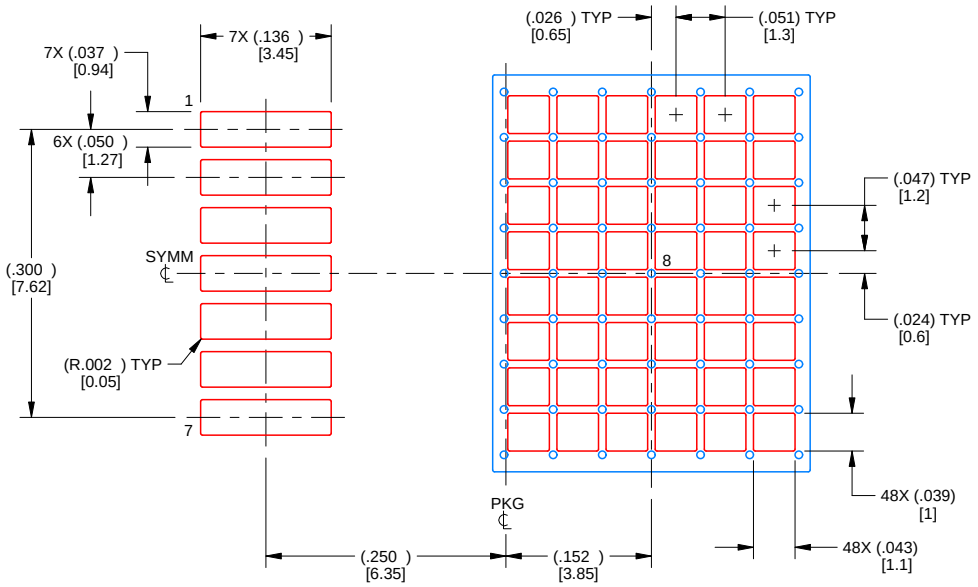
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTW0007A

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 5X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 8: 60%

4232469/A 11/2025

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

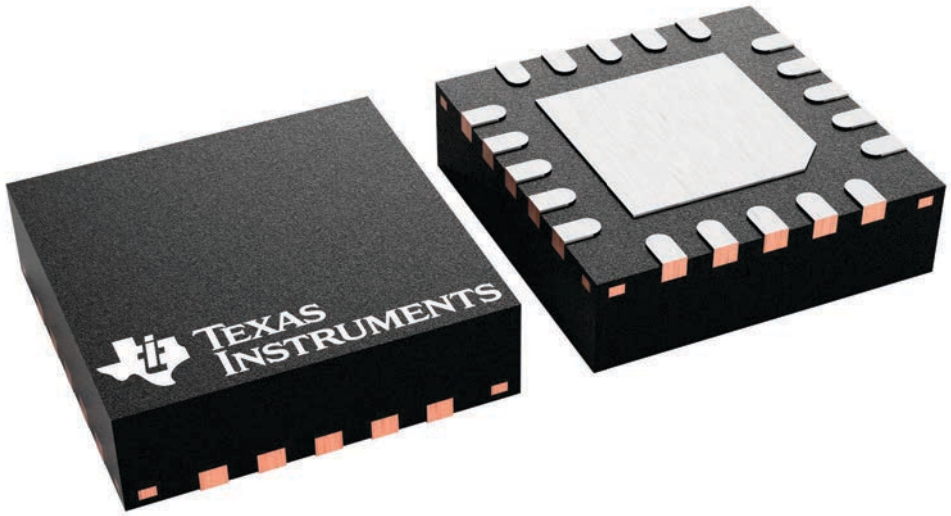
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



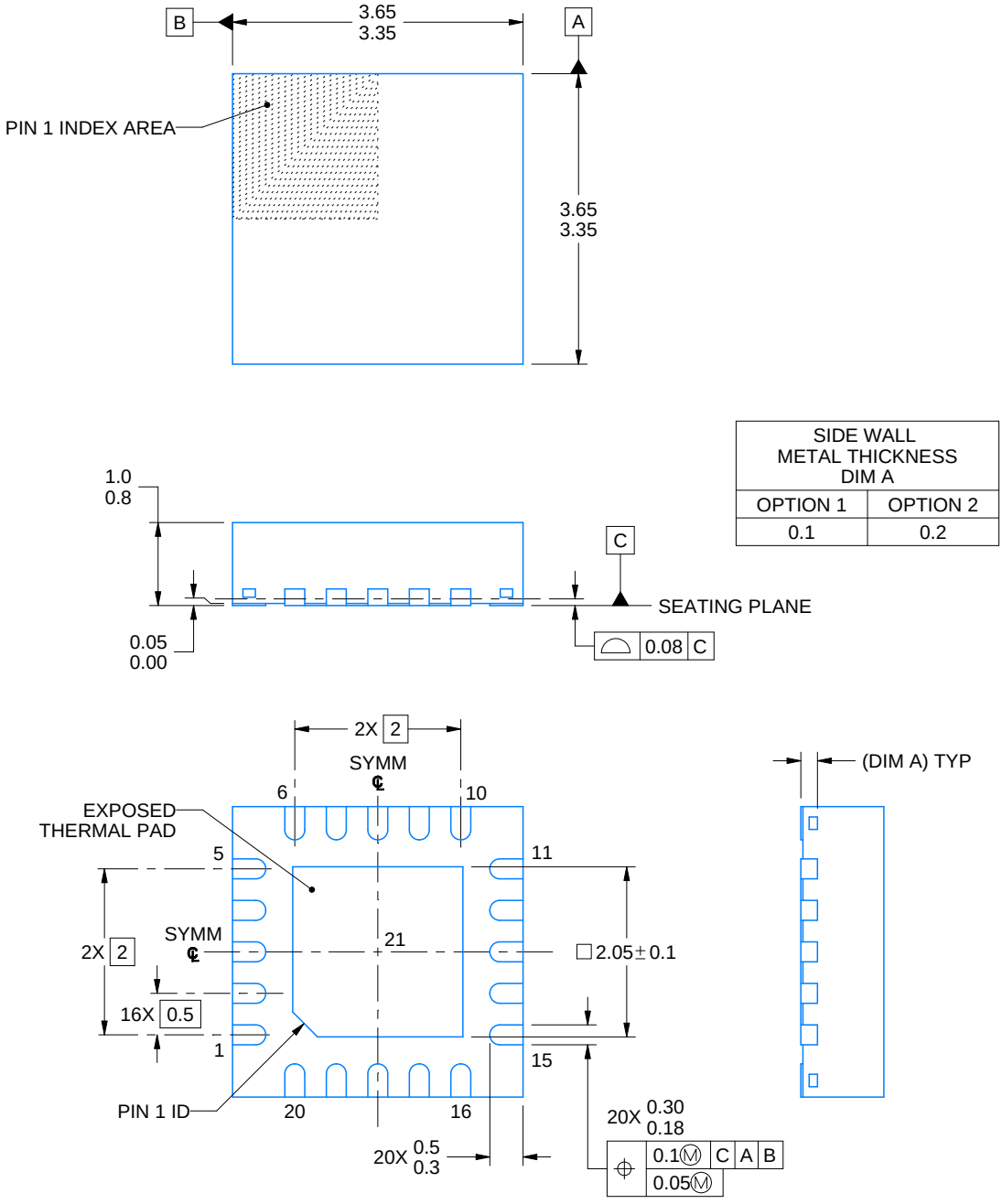
4228482/A

PACKAGE OUTLINE

RGR0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

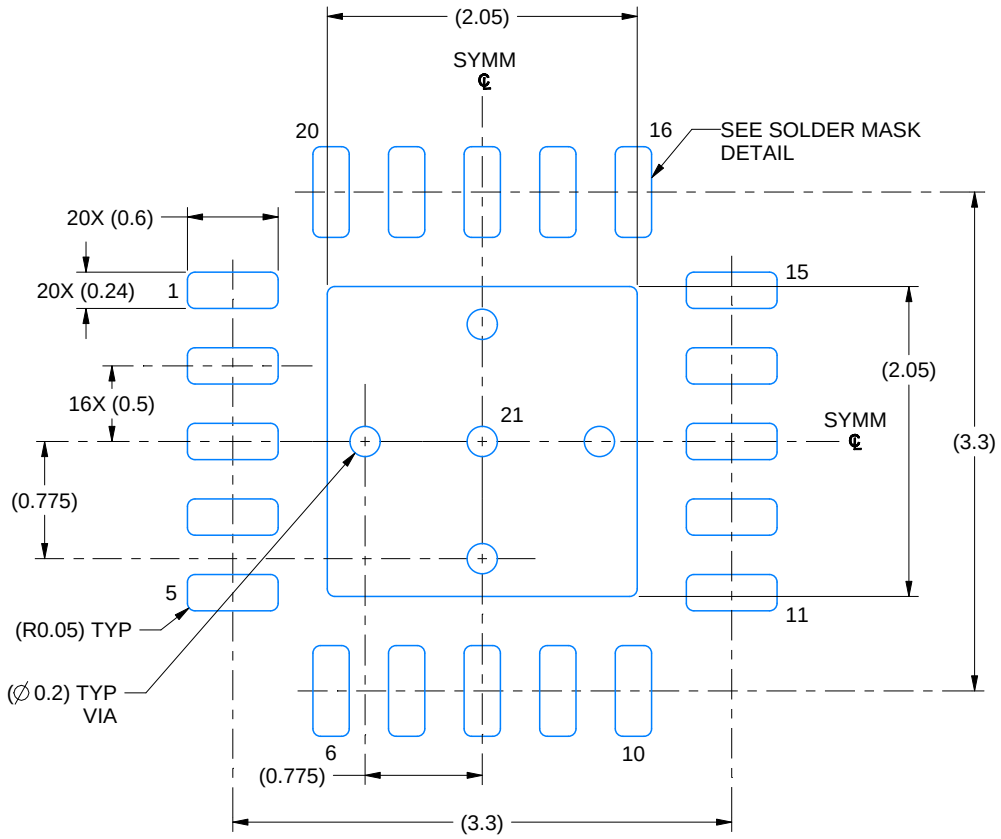


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

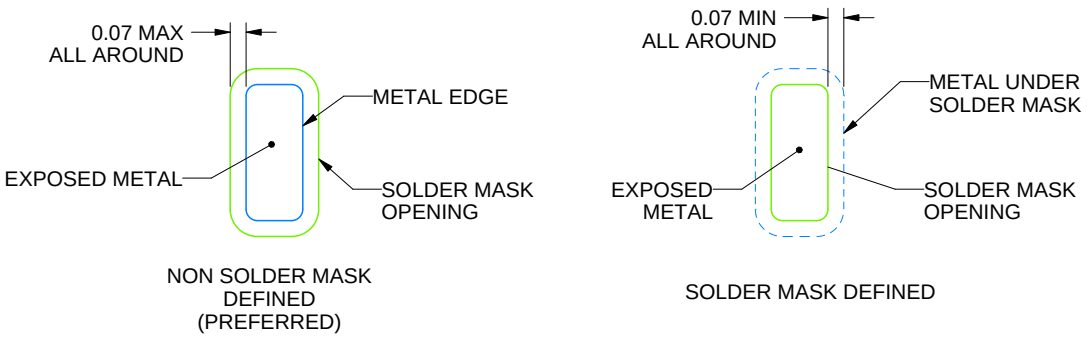
4219031/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

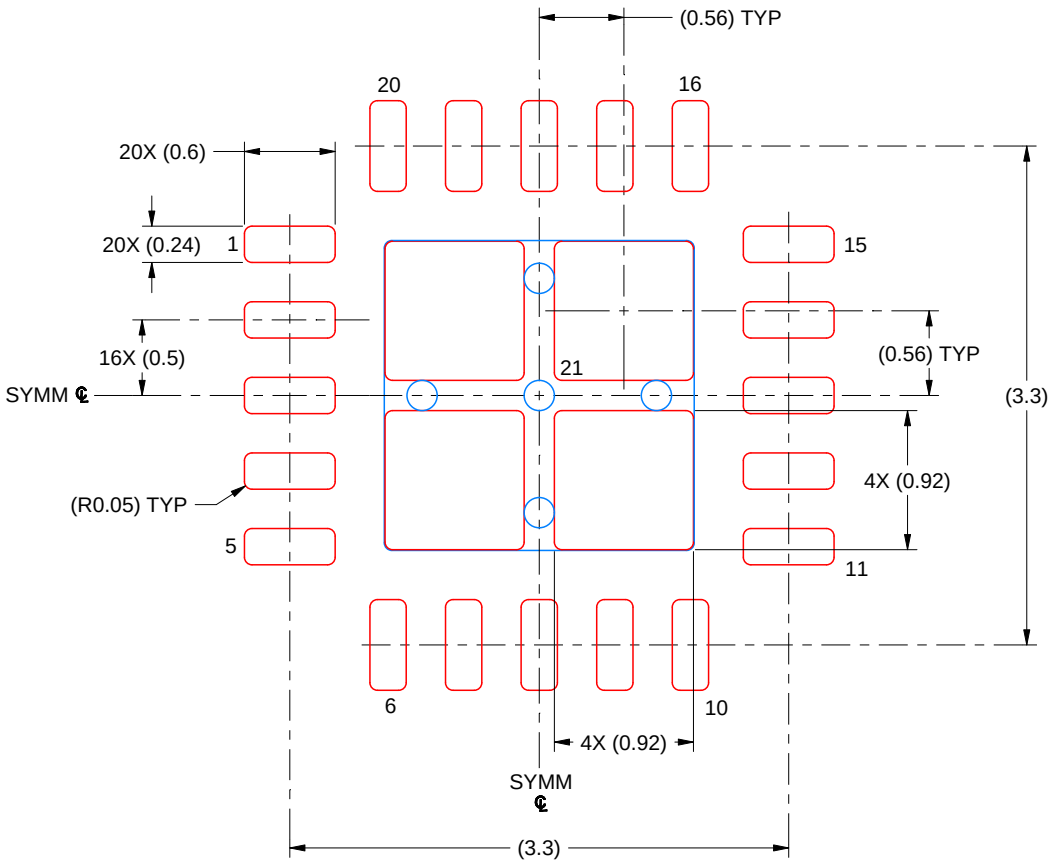


SOLDER MASK DETAILS

4219031/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219031/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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