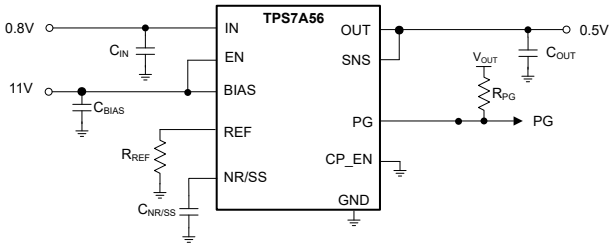
TPS7A56 6A, Low-V_{IN}, Low-Noise, High-Accuracy, Ultra-Low Dropout (LDO) Voltage Regulator

1 Features

- Input voltage range:
  - Without BIAS: 1.1V to 6.0V
  - With BIAS: 0.7V to 6.0V
- Output voltage noise: 2.45μV_{RMS}
- 1% (max) accuracy over line, load, and temperature
- Low dropout: 90mV at 6A
- Power-supply rejection ratio (6A):
  - 100dB at 1kHz
  - 78dB at 10kHz
  - 60dB at 100kHz
  - 36dB at 1MHz
- Load transient response:
  - ±3mV with a 100mA to 6A load step
- Adjustable output voltage range: 0.5V to 5.0V
- Adjustable soft-start inrush control
- BIAS rail:
  - Internal charge pump or 3V to 11V external rail
  - Internal charge pump is able to be disabled
- Open-drain, power-good (PG) output
- Package:
  - 3mm × 3mm, 16-pin WQFN
  - EVM $R_{\theta JA}$: 21.9°C/W

2 Applications

- Macro remote radio units (RRU)
- Outdoor backhaul units
- Active antenna system mMIMO (AAS)
- Ultrasound scanners
- Lab and field instrumentation
- Sensor, imaging, and radar



Typical Application Circuit

3 Description

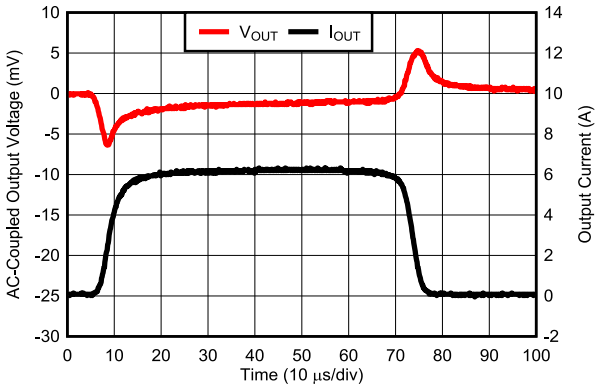
The TPS7A56 is a low-noise (2.45μV_{RMS}), ultra-low-dropout linear regulator (LDO) capable of sourcing 6A with only 90mV of dropout, independently of the output voltage. The device output voltage is adjustable from 0.5V to 5V using a single external resistor. The combination of low noise, high PSRR (36dB at 1MHz), and high output-current capability makes the TPS7A56 designed for powering noise-sensitive components. These components (such as RF amplifiers, radar sensors, SERDES, and analog chipsets) are found in radar power, communication, and imaging applications.

Digital loads requiring low-input, low-output (LILO) voltage operation also benefit from exceptional accuracy, remote sensing, transient performance, and soft-start capabilities to provide best system performance. These loads include application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs). The versatility, performance, and small footprint make this LDO an excellent choice for high-current analog loadsand digital loads such as serializer/deserializers (SerDes), FPGAs, and DSPs. High-current analog loads include analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and imaging sensors.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7A56	RTE (WQFN, 16)	3mm × 3mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS7A56 Load Transient Response

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

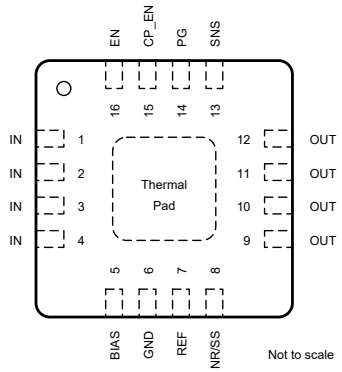

Figure 4-1. RTE Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BIAS	5	I	BIAS supply voltage pin. See the *Charge Pump Enable and BIAS Rail* section for additional information.
CP_EN	15	I	Charge pump enable pin. See the *Charge Pump Enable and BIAS Rail* section for additional information.
EN	16	I	Enable pin. See the *Precision Enable and UVLO* section for additional information.
GND	6	GND	Ground pin. See the *Layout Guidelines* section for additional information.
IN	1, 2, 3, 4	I	Input supply voltage pin. See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* section for more details.
NR/SS	8	I/O	Noise-reduction pin. See the *Programmable Soft-Start (NR/SS Pin)* and *Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)* sections for additional information.
OUT	9, 10, 11, 12	O	Regulated output pin. See the *Output Voltage Setting and Regulation* and *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* sections for more details.
PG	14	O	Open-drain, power-good indicator pin for the low-dropout regulator (LDO) output voltage. See the *Power-Good Pin (PG Pin)* section for additional information.
REF	7	I/O	Reference pin. See the *Output Voltage Setting and Regulation* section for additional information.
SNS	13	I	Output sense pin. See the *Output Voltage Setting and Regulation* section for additional information.
Thermal Pad	—	GND	Connect the pad to GND for best possible thermal performance. See the *Layout* section for more information.

(1) I = input, O = output, I/O = input or output, G = ground.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	BIAS	–0.3	11.2	V
	IN, PG, EN, CP_EN	–0.3	6.5	
	REF, NR/SS, SNS	–0.3	6	
	OUT	–0.3	V_{IN} + 0.3 (2)	
Current	OUT	Internally limited		A
	PG (sink current into the device)		5	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.0V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage	0.7		6	V
V_{REF}	Reference voltage	0.5		5	V
V_{OUT}	Output voltage	0.5		5	V
V_{BIAS}	Bias voltage	3		11	V
I_{OUT}	Output current	0		6	A
C_{IN}	Input capacitor	4.7	10	1000	µF
C_{OUT}	Output capacitor (1)	22		3000	µF
C_{OUT_ESL}	Output capacitor ESR	2		20	mΩ
Z_{OUT_ESL}	Total impedance ESL	0.2		1	nH
C_{BIAS}	Bias pin capacitor	0	1	100	µF
$C_{NR/SS}$	Noise-reduction capacitor	0.1	4.7	10	µF
R_{PG}	Power-good pullup resistance	10		100	kΩ
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 15 µF minimum required for stability

5.4 Thermal Information

THERMAL METRIC (1)		TPS7A56		UNIT
		RTE (WQFN) (2)	RTE (WQFN) (3)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	21.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.0	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	–	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application note.
(2) Evaluated using JEDEC standard (2s2p).
(3) Evaluated using EVM.

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5.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, $C_{NR/SS}$ = 100nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(IN)}$	Input supply UVLO with BIAS	V_{IN} rising, V_{CP_EN} = 1.8V (3V ≤ V_{BIAS} ≤ 11V) and V_{CP_EN} = 0V (V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V)		0.67	0.7	V
$V_{HYS(UVLO_IN)}$	Input supply UVLO hysteresis with BIAS	V_{CP_EN} = 1.8V (3V ≤ V_{BIAS} ≤ 11V) and V_{CP_EN} = 0V (V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V)		50		mV
$V_{UVLO(IN)}$	Input supply UVLO without BIAS	V_{IN} rising, V_{CP_EN} = 1.8V		1.07	1.1	V
$V_{HYS(UVLO_IN)}$	Input supply UVLO hysteresis without BIAS	V_{CP_EN} = 1.8V		50		mV
$V_{UVLO(BIAS)}$ – V_{REF}	BIAS UVLO relative to V_{REF} without CP	V_{BIAS} rising, V_{CP_EN} = 0V, 1.4V ≤ V_{REF} ≤ 5.2V		2.1	2.95	V
$V_{HYS(UVLO_BIAS - REF)}$	BIAS UVLO relative to V_{REF} hysteresis without CP	V_{CP_EN} = 0V, 1.4V ≤ V_{REF} ≤ 5.2V		240		mV
$V_{UVLO(BIAS)}$	BIAS UVLO with CP	V_{BIAS} rising, V_{CP_EN} = 1.8V, 0.7V ≤ V_{IN} < 1.1V		2.8	2.95	V
$V_{HYS(UVLO_BIAS)}$	BIAS UVLO hysteresis with CP	V_{CP_EN} = 1.8V, 0.7V ≤ V_{IN} < 1.1V		115		mV
$I_{NR/SS}$	NR/SS fast start-up charging current	$V_{NR/SS}$ = GND, V_{IN} = 1.1V		0.2		mA
V_{OUT}	Output voltage accuracy (1)	0.5V ≤ V_{OUT} ≤ 5.2V, 0A ≤ I_{OUT} ≤ 6A, V_{CP_EN} = 0V, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V; 0.7V ≤ V_{IN} ≤ 6V (2), V_{CP_EN} = 1.8V, 3V ≤ V_{BIAS} ≤ 11V, 0.7V ≤ V_{IN} ≤ 6V (2), V_{CP_EN} = 1.8V, no BIAS, 1.1V ≤ V_{IN} ≤ 6V	–1		1	%
I_{REF}	REF current pin	V_{IN} = 1.1V, V_{CP_EN} = 1.8V, V_{OUT} = 0.5V, I_{LOAD} = 0A, V_{BIAS} = 0V		50		µA
		V_{CP_EN} = 0V (CP disabled), 0.7V ≤ V_{IN} ≤ 6V (1) (2), 0.5V ≤ V_{OUT} ≤ 5.2V, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V, 0A ≤ I_{OUT} ≤ 6A	–1		1	%
		V_{CP_EN} = 1.8V (CP enabled, V_{BIAS} = 0V), 1.1V ≤ V_{IN} ≤ 6V (1), 0.5V ≤ V_{OUT} ≤ 5.2V, 0A ≤ I_{OUT} ≤ 6A (2)	–1		1	
		V_{CP_EN} = 1.8V (CP enabled), 0.7V ≤ V_{IN} ≤ 6V (1), 0.5V ≤ V_{OUT} ≤ 5.2V, 3V ≤ V_{BIAS} ≤ 11V, 0A ≤ I_{OUT} ≤ 6A	–1		1	
V_{OS}	Output offset voltage ($V_{NR/SS}$ - V_{OUT})	V_{IN} = 0.7V, V_{OUT} = 0.5V, I_{OUT} = 0A, V_{CP_EN} = 1.8V, 3V ≤ V_{BIAS} ≤ 11V, V_{CP_EN} = 0V, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V	–1		1	mV
		0.7V ≤ V_{IN} ≤ 6V (1) (2), 0.5V ≤ V_{OUT} ≤ 5.2V, V_{CP_EN} = 1.8V, 3V ≤ V_{BIAS} ≤ 11V, 0A ≤ I_{OUT} ≤ 6A	–2		2	
		1.1V ≤ V_{IN} ≤ 6.0V (1) (2), 0.5V ≤ V_{OUT} ≤ 5.2V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, 0A ≤ I_{OUT} ≤ 6A	–2		2	
		0.7V ≤ V_{IN} ≤ 6V (1) (2), 0.5V ≤ V_{OUT} ≤ 5.2V, V_{CP_EN} = 0V, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V, 0A ≤ I_{OUT} ≤ 6A	–2		2	
$\Delta I_{REF(\Delta VBIAS)}$	Line regulation: ΔI_{REF}	V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V, V_{IN} = 0.7V, V_{OUT} = 0.5V, V_{CP_EN} = 0V, I_{OUT} = 0A		0.15		nA/V
$\Delta V_{OS(\Delta VBIAS)}$	Line regulation: ΔV_{OS}	V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V, V_{IN} = 0.7V, V_{OUT} = 0.5V, V_{CP_EN} = 0V, I_{OUT} = 0A		0.06		µV/V
$\Delta I_{REF(\Delta VIN)}$	Line regulation: ΔI_{REF}	1.1V ≤ V_{IN} ≤ 6V, V_{OUT} = 0.5 V, V_{CP_EN} = 1.8 V, I_{OUT} = 0 A, V_{BIAS} = 0 V		0.03		nA/V
$\Delta V_{OS(\Delta VIN)}$	Line regulation: ΔV_{OS}	1.1V ≤ V_{IN} ≤ 6V, V_{OUT} = 0.5V, V_{CP_EN} = 1.8V, I_{OUT} = 0A, V_{BIAS} = 0V		0.01		µV/V
$\Delta V_{OS(\Delta IOUT)}$	Load regulation: ΔV_{OS}	V_{IN} = 0.7V, V_{OUT} = 0.5V, V_{CP_EN} = 0V, 0A ≤ I_{OUT} ≤ 6A, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V		5		µV/A
		V_{OUT} = 5.0V, V_{CP_EN} = 1.8V, 0A ≤ I_{OUT} ≤ 6A, V_{BIAS} = 0V		175		

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5.5 Electrical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, $C_{NR/SS}$ = 100nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Change in I_{REF} vs V_{REF}	0.5V ≤ V_{REF} ≤ 5.2V, V_{IN} = 6V, I_{OUT} = 0A, V_{CP_EN} = 1.8V, V_{BIAS} = 0V		4.4		nA
	Change in V_{OS} vs V_{REF}			0.25		mV
V_{DO}	Dropout voltage (3)	1.1V ≤ V_{IN} ≤ 5.3V, I_{OUT} = 6A, V_{CP_EN} = 1.8V, –40°C ≤ T_J ≤ +125°C		90	132	mV
		1.1V ≤ V_{IN} ≤ 5.3V, I_{OUT} = 6A, V_{CP_EN} = 1.8V, –40°C ≤ T_J ≤ +85°C			120	
		0. V ≤ V_{IN} ≤ 1.1V, I_{OUT} = 6A, V_{CP_EN} = 1.8V, V_{BIAS} = 3V, –40°C ≤ T_J ≤ +125°C		90	132	
		0. V ≤ V_{IN} ≤ 1.1V, I_{OUT} = 6A, V_{CP_EN} = 1.8V, V_{BIAS} = 3V, –40°C ≤ T_J ≤ +85°C			120	
		0.7V ≤ V_{IN} ≤ 5.3V, I_{OUT} = 6A, V_{CP_EN} = 0V, V_{BIAS} = V_{IN} + 3.2V, –40°C ≤ T_J ≤ +125°C		90	132	
		0.7V ≤ V_{IN} ≤ 5.3V, I_{OUT} = 6A, V_{CP_EN} = 0V, V_{BIAS} = V_{IN} + 3.2V, –40°C ≤ T_J ≤ +85°C			120	
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 5.0V, V_{IN} = $V_{OUT(NOM)}$ + 400mV, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V	6.2	7.2	8.4	A
I_{SC}	Short circuit current limit	R_{LOAD} = 10mΩ, under foldback operation		5		A
I_{BIAS}	BIAS pin current	V_{IN} = 6V, I_{OUT} = 0A, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V, V_{OUT} = 5.2V	1	1.5	2.5	mA
		V_{IN} = 0.7V, I_{OUT} = 6A, V_{OUT} = 0.5V, V_{CP_EN} = 1.8V, 3.0V ≤ V_{BIAS} ≤ 11V	8	11	18	
I_{GND}	GND pin current	V_{IN} = 6V, I_{OUT} = 0A, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V, V_{OUT} = 5.2V	3.5	5	8	mA
		V_{IN} = 5.6V, I_{OUT} = 6A, V_{OUT} = 5.0V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V		18		
		V_{IN} = 1.1V, I_{OUT} = 6A, V_{OUT} = 0.5V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V	12	18	27	
		V_{IN} = 0.7V, I_{OUT} = 6A, V_{OUT} = 0.5V, V_{CP_EN} = 1.8V, 3V ≤ V_{BIAS} ≤ 11V	11	18	26	
		V_{IN} = 0.7V, I_{OUT} = 6A, V_{OUT} = 0.5V, V_{CP_EN} = 0V, V_{OUT} + 3.2V ≤ V_{BIAS} ≤ 11V	5	7	12	
I_{SDN}	Shutdown GND pin current	PG = (open), V_{IN} = 6V, V_{EN} = 0.4V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V		100	300	µA
		PG = (open), V_{IN} = 6V, V_{EN} = 0.4V, V_{CP_EN} = 0.4V, V_{BIAS} = 11V		150	450	
I_{EN}	EN pin current	V_{IN} = 6V, 0V ≤ V_{EN} ≤ 6V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V	-5		5	µA
$V_{IH(EN)}$	EN trip point rising (turn-on)	V_{IN} = 1.1V (V_{CP_EN} = 1.8V) or V_{BIAS} ≥ 3V (V_{CP_EN} = 0V)	0.62	0.65	0.68	V
$V_{HYS(EN)}$	EN trip point hysteresis	V_{IN} = 1.1V (V_{CP_EN} = 1.8V) or V_{BIAS} ≥ 3V (V_{CP_EN} = 0V)		40		mV
I_{CP_EN}	CP_EN pin current	V_{IN} = 6.0V, 0 V ≤ V_{CP_EN} ≤ 6V	–5		5	µA
$V_{IH(CP_EN)}$	CP_EN trip point rising (turn-on)	1.1V ≤ V_{IN} ≤ 6V, V_{EN} = 1.8V, V_{BIAS} = 0V, 0.7V ≤ V_{IN} ≤ 1.1V, V_{EN} = 1.8 V, V_{BIAS} = 3V	0.57	0.6	0.63	V
$V_{HYS(CP_EN)}$	CP_EN trip point hysteresis	1.1V ≤ V_{IN} ≤ 6V, V_{EN} = 1.8V, V_{BIAS} = 0V, 0.7V ≤ V_{IN} ≤ 1.1V, V_{EN} = 1.8V, V_{BIAS} = 3V		56		mV
$V_{IT(PG)}$	PG pin threshold	For PG transitioning low with falling V_{OUT}, V_{IN} = 1.1V, V_{BIAS} = 0V, V_{CP_EN} = 1.8V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)	87	90	93	%
$V_{HYS(PG)}$	PG pin hysteresis	V_{IN} = 1.1V, V_{BIAS} = 0V, V_{CP_EN} = 1.8V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)		2		%
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} = 1.1V, V_{BIAS} = 0V, V_{CP_EN} = 1.8V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)			0.4	V
$I_{LKG(PG)}$	PG pin leakage current	V_{PG} = 6V, V_{OUT} > $V_{IT(PG)}$, V_{IN} = 1.1V, V_{BIAS} = 0V, V_{CP_EN} = 1.8V			1	µA

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5.5 Electrical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, I_{OUT} = 0A, V_{EN} = 1.8V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, $C_{NR/SS}$ = 100nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply ripple rejection	f = 1MHz, V_{IN} = 0.8V, $V_{OUT(NOM)}$ = 0.5V, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF		40		dB
		f = 1MHz, V_{IN} = 0.9V, $V_{OUT(NOM)}$ = 0.5V, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF		40		
		f = 1MHz, V_{IN} = 5.3V, $V_{OUT(NOM)}$ = 5V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF		40		
		f = 1MHz, V_{IN} = 5.4V, $V_{OUT(NOM)}$ = 5V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF		36		
V_n	Output noise voltage	BW = 10Hz to 100kHz, 0.7V ≤ V_{IN} ≤ 6V, 0.5V ≤ V_{OUT} ≤ 5.2V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V		2.49		μV_{RMS}
		BW = 10Hz to 100kHz, 1.1V ≤ V_{IN} ≤ 6V, 0.5V ≤ V_{OUT} ≤ 5.2V, I_{OUT} =6A, $C_{NR/SS}$ = 4.7µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V		2.49		
	Noise spectral density	f = 100Hz, 0.7V ≤ V_{IN} ≤ 6V, 0.5V ≤ V_{OUT} ≤ 5.2V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V		20		$nV/\sqrt{Hz}$
		f = 1kHz, 0.7V ≤ V_{IN} ≤ 6V, 0.5V ≤ V_{OUT} ≤ 5.2V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V		9		
		f = 10kHz, 0.7V ≤ V_{IN} ≤ 6V, 0.5V ≤ V_{OUT} ≤ 5.2V, I_{OUT} = 6A, $C_{NR/SS}$ = 4.7µF, V_{CP_EN} = 0V, V_{BIAS} = V_{OUT} + 3.2V		6		
R_{DIS}	Output pin active discharge resistance	V_{IN} = 1.1V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{EN} = 0V		110		Ω
R_{NR/SS_DIS}	NR/SS pin active discharge resistance	V_{IN} = 1.1V, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{EN} = 0V		100		Ω
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		150		°C

(1) Max power dissipation of 2W.
(2) Limited by pulse max power dissipation. For 0mA ≤ I_{OUT} ≤ 2.5A, V_{IN} = 6V, 0mA ≤ I_{OUT} ≤ 6A, V_{IN} = 5.6V.
(3) V_{REF} = V_{IN}, V_{SNS} = 97% × V_{REF}.

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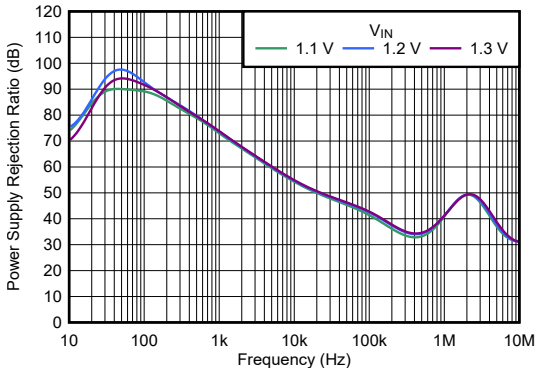
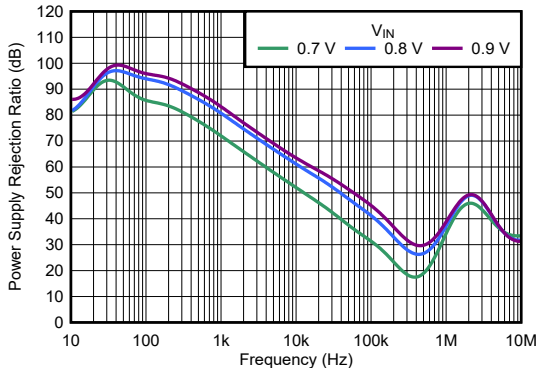
5.6 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



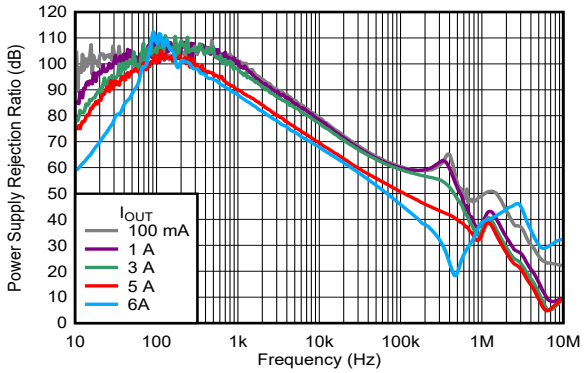
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = V_{EN}, V_{OUT} = 0.9V, V_{BIAS} = 0V, I_{OUT} = 6A

Figure 5-1. PSRR vs Frequency and V_{IN} for CP Enabled, No Bias



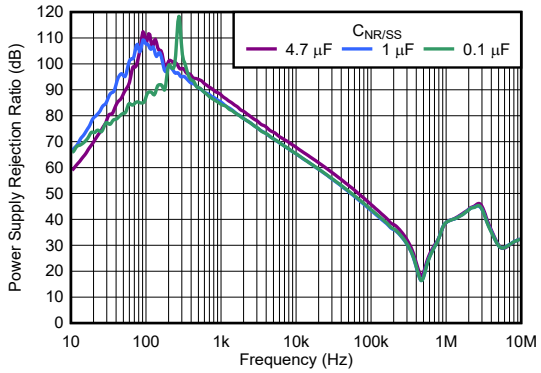
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = V_{EN}, V_{OUT} = 0.5V, V_{BIAS} = 3V, I_{OUT} = 6A

Figure 5-2. PSRR vs Frequency and V_{IN} for CP Enabled, Minimum Bias



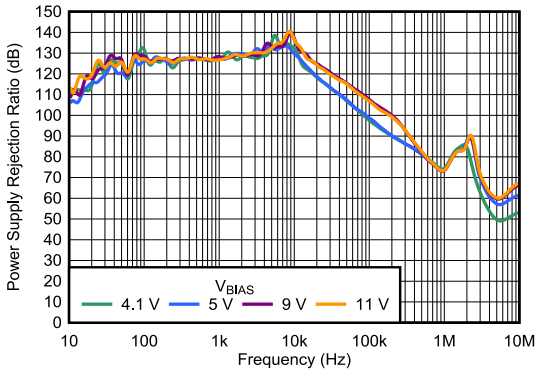
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{IN} = 1.2V, V_{OUT} = 0.9V, V_{BIAS} = 0V

Figure 5-3. PSRR vs Frequency and I_{OUT} for CP Enabled, No Bias



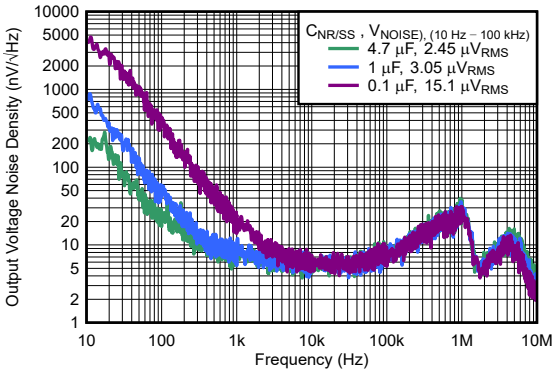
C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{IN} = 1.2V, V_{OUT} = 0.9V, V_{BIAS} = 11V, I_{OUT} = 6A

Figure 5-4. PSRR vs Frequency and $C_{NR/SS}$ for CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{IN} = 1.2V, V_{OUT} = 0.9V, I_{OUT} = 6A

Figure 5-5. BIAS PSRR vs Frequency and V_{BIAS} for CP Disabled, V_{IN} = 1.2V



C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = V_{EN}, V_{IN} = 5.3V, V_{OUT} = 5V, I_{OUT} = 6A

Figure 5-6. Output Voltage Noise Density vs Frequency and $C_{NR/SS}$ for CP Enabled

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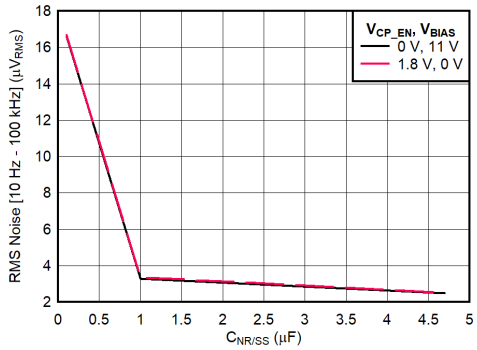
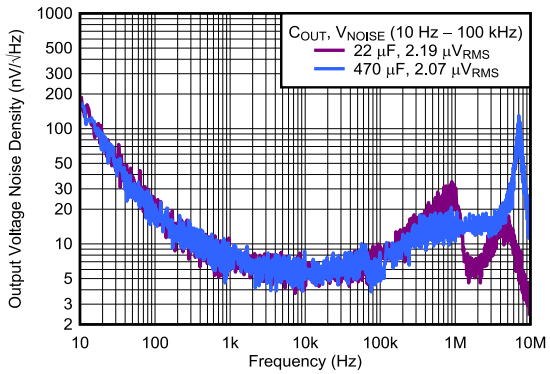
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



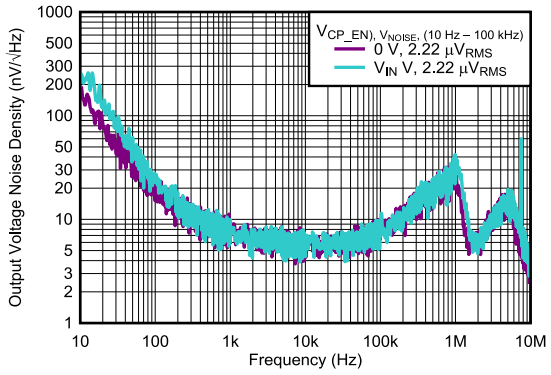
$C_{NR/SS}$ = C_{IN} = 4.7µF, V_{IN} = 5.3V, V_{OUT} = 5V

Figure 5-7. RMS Noise vs $C_{NR/SS}$



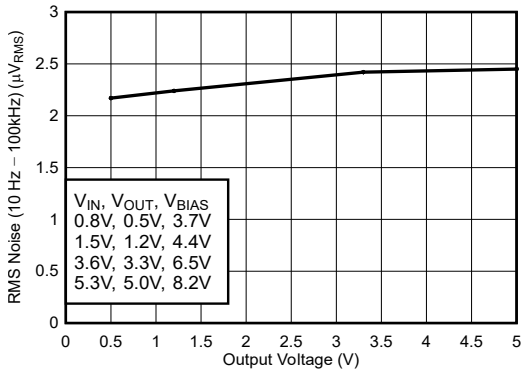
$C_{NR/SS}$ = C_{IN} = 4.7µF, CP_EN = GND, V_{IN} = 0.8V, V_{OUT} = 0.5V, V_{BIAS} = 3.7V

Figure 5-8. Output Voltage Noise Density vs Frequency and C_{OUT}



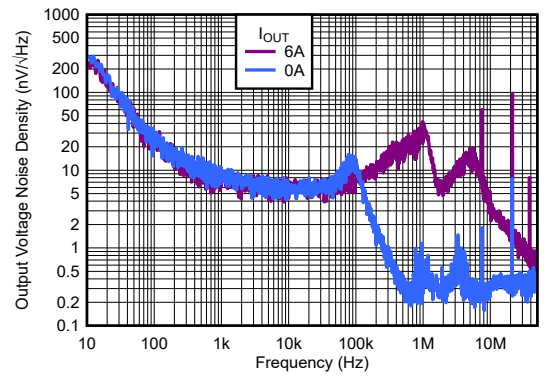
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{IN} = 0.8V, V_{BIAS} = 3.7V, I_{OUT} = 6A

Figure 5-9. Output Voltage Noise Density vs Frequency and V_{CP_EN} for V_{OUT} = 0.5V



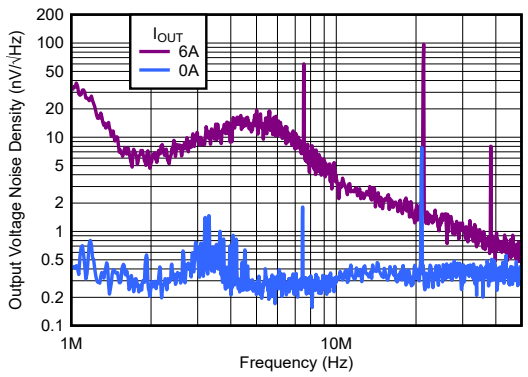
$C_{NR/SS}$ = C_{IN} = 4.7µF, V_{CP_EN} = 0V, C_{OUT} = 22µF, I_{OUT} = 6A

Figure 5-10. RMS Noise vs V_{OUT} for CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, V_{CP_EN} = V_{EN}, C_{OUT} = 22µF, V_{IN} = V_{OUT} + 0.3V

Figure 5-11. Output Voltage Noise Density vs Frequency and V_{OUT} for CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{IN} = V_{OUT} + 0.3V, V_{CP_EN} = V_{EN}, V_{BIAS} = 0V, V_{OUT} = 5V

Figure 5-12. Charge Pump Output Voltage Noise Density vs Frequency and I_{OUT}

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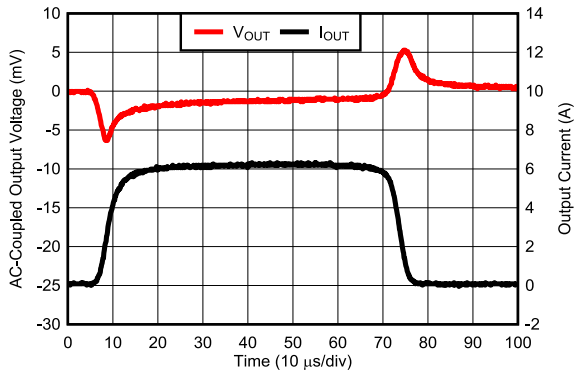
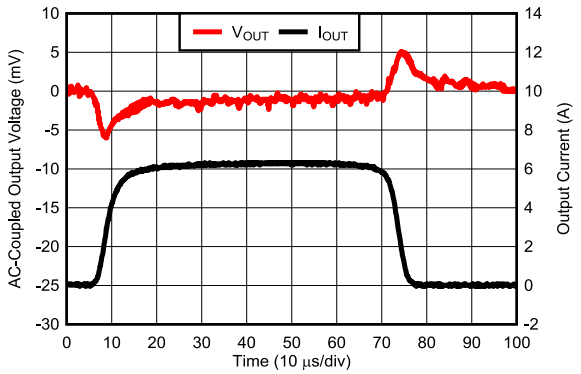
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



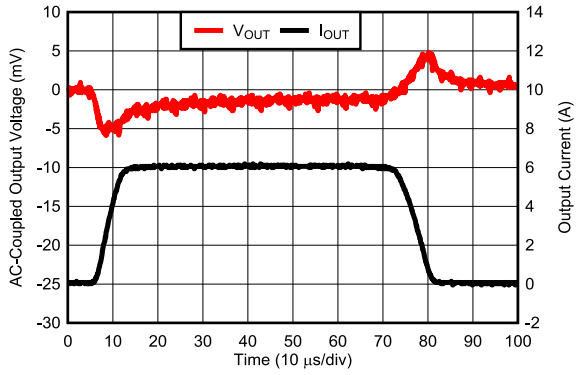
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 3V, V_{IN} = 0.8V, SR = 1A/µs

Figure 5-13. Load Transient for V_{OUT} = 0.5V, I_{OUT} = 100mA to 6A, CP Enabled



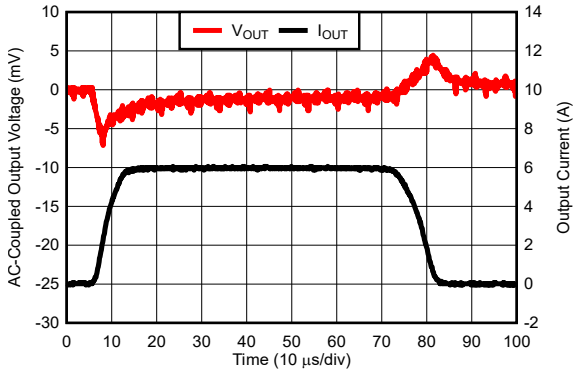
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{IN} = 1.1V, SR = 1A/µs

Figure 5-14. Load Transient for V_{OUT} = 0.5V, I_{OUT} = 100mA to 6A, CP Enabled



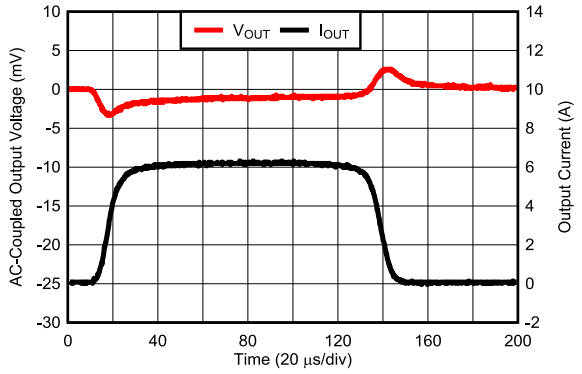
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{IN} = 3.6V, SR = 1A/µs

Figure 5-15. Load Transient for V_{OUT} = 3.3V, I_{OUT} = 100mA to 6A, CP Enabled



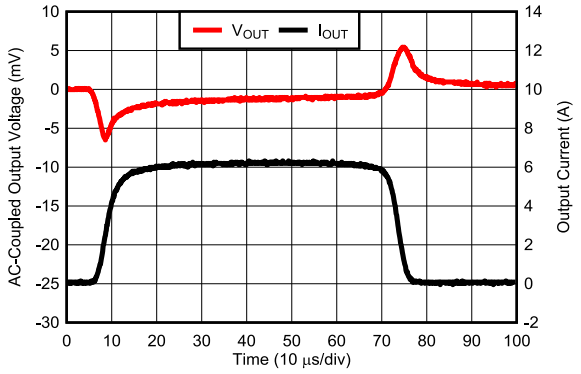
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{IN} = 5.5V, SR = 1A/µs

Figure 5-16. Load Transient for V_{OUT} = 5.2V, I_{OUT} = 100mA to 6A, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V, V_{IN} = 0.8V

Figure 5-17. Load Transient for V_{OUT} = 0.5V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 0.5A/µs



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V, V_{IN} = 0.8V

Figure 5-18. Load Transient for V_{OUT} = 0.5V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 1A/µs

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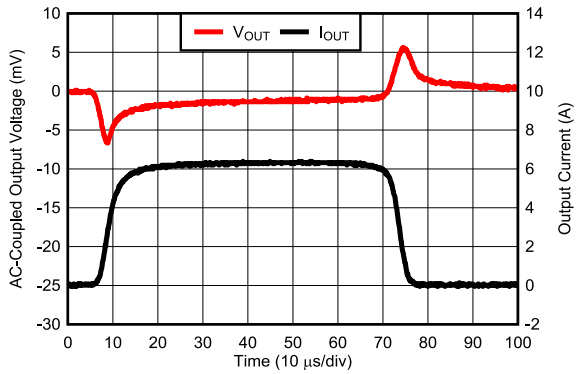
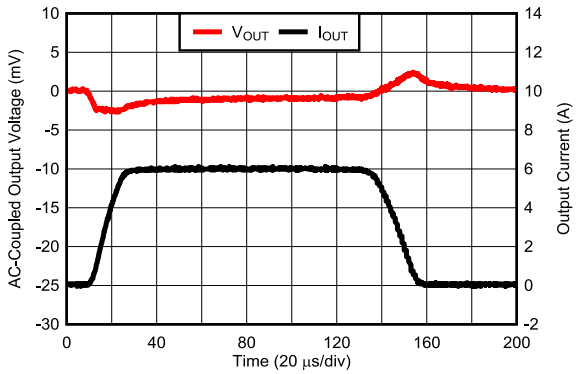
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



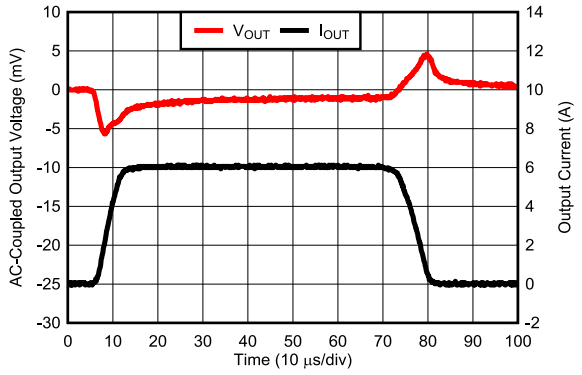
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 11V, V_{IN} = 0.8V

Figure 5-19. Load Transient for V_{OUT} = 0.5V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 1A/µs, V_{BIAS} = 11V



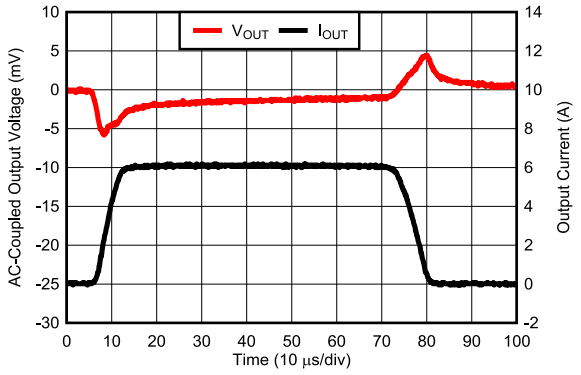
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 6.5V, V_{IN} = 3.6V

Figure 5-20. Load Transient for V_{OUT} = 3.3V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 0.5A/µs, V_{BIAS} = 6.5V



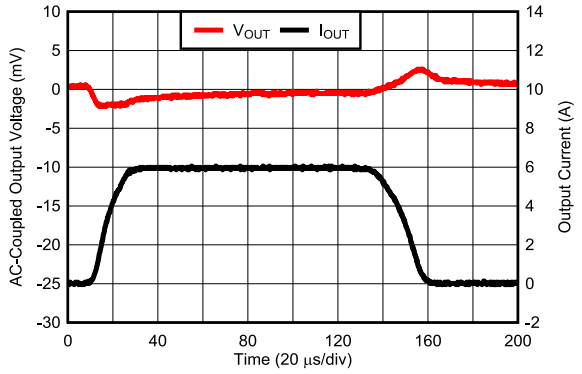
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 6.5V, V_{IN} = 3.6V

Figure 5-21. Load Transient for V_{OUT} = 3.3V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 1A/µs, V_{BIAS} = 6.5V



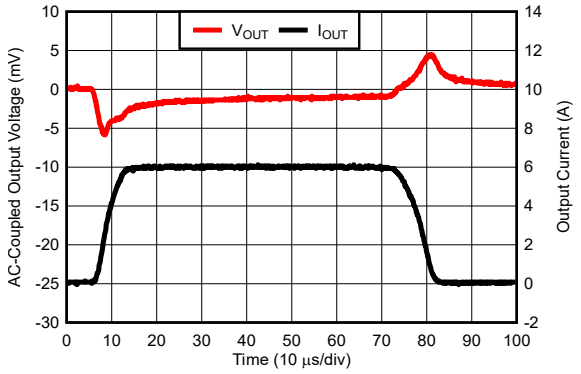
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 11V, V_{IN} = 3.6V

Figure 5-22. Load Transient for V_{OUT} = 3.3V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 1A/µs, V_{BIAS} = 11V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 8.4V, V_{IN} = 5.5V

Figure 5-23. Load Transient for V_{OUT} = 5.2V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 0.5A/µs, V_{BIAS} = 8.4V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 8.4V, V_{IN} = 5.5V

Figure 5-24. Load Transient for V_{OUT} = 5.2V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 1A/µs, V_{BIAS} = 8.4V

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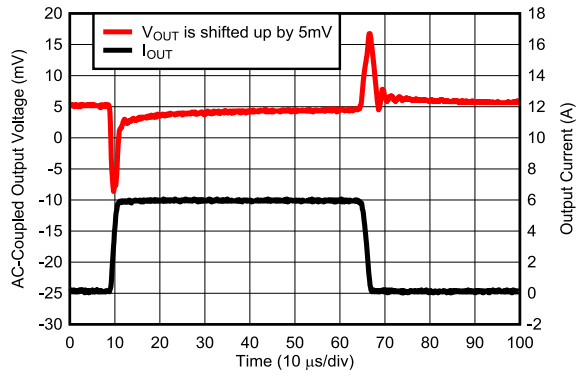
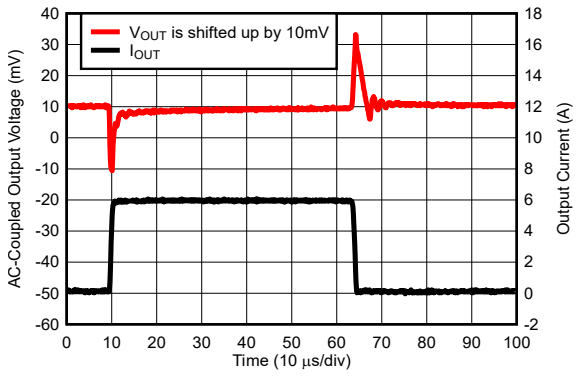
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



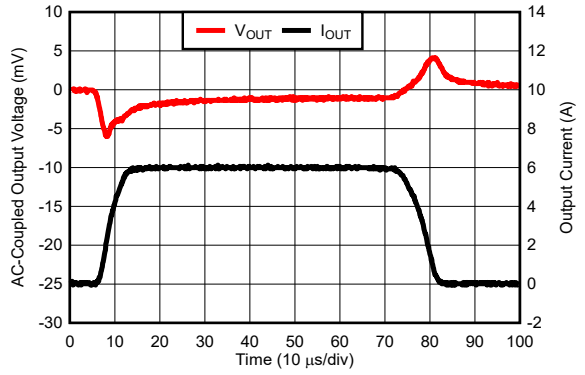
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 8.4V, V_{IN} = 5.5V

Figure 5-25. Load Transient for V_{OUT} = 5.2V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 5A/µs, V_{BIAS} = 8.4V



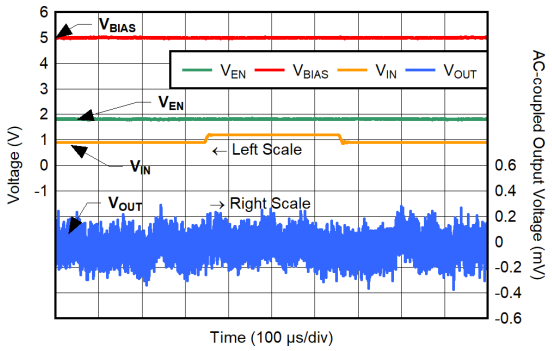
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 8.4V, V_{IN} = 5.5V

Figure 5-26. Load Transient for V_{OUT} = 5.2V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 10A/µs, V_{BIAS} = 8.4V



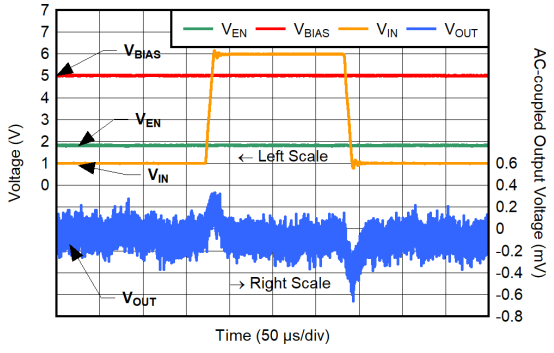
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 11V, V_{IN} = 5.5V

Figure 5-27. Load Transient for V_{OUT} = 5.2V, I_{OUT} = 100mA to 6A, CP Disabled, SR = 1A/µs, V_{BIAS} = 11V



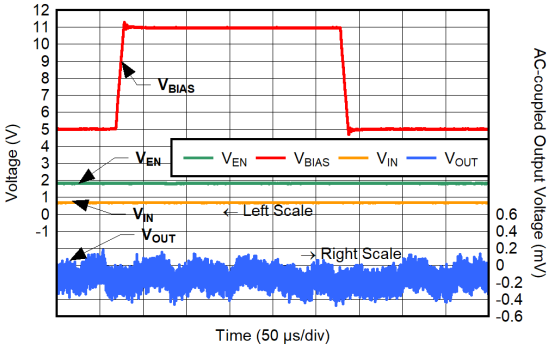
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 100mA, SR = 1V/µs

Figure 5-28. IN Line Transient for V_{IN} = 0.9V to 1.2V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 100mA, SR = 1V/µs

Figure 5-29. IN Line Transient for V_{IN} = 0.9V to 6V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{IN} = 0.8V, V_{OUT} = 0.5V, SR = 1V/µs

Figure 5-30. BIAS Line Transient for V_{IN} = 0.9V to 6V, I_{OUT} = 100mA

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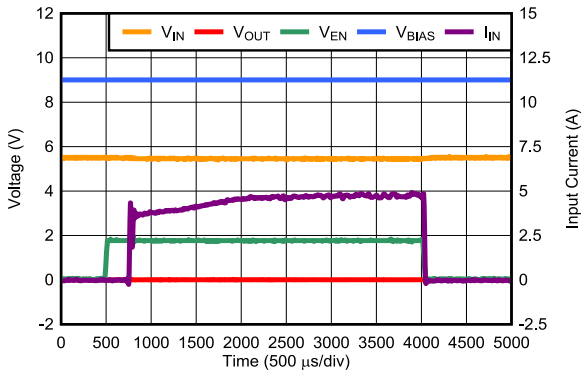
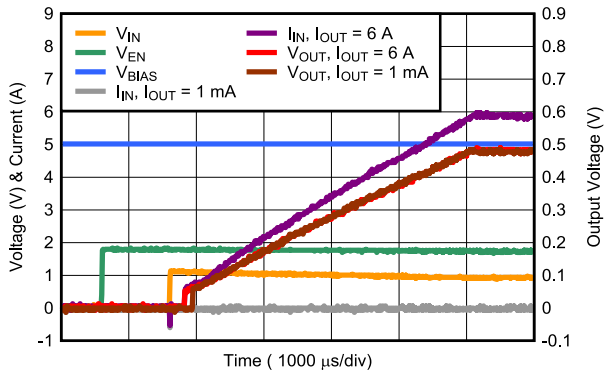
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



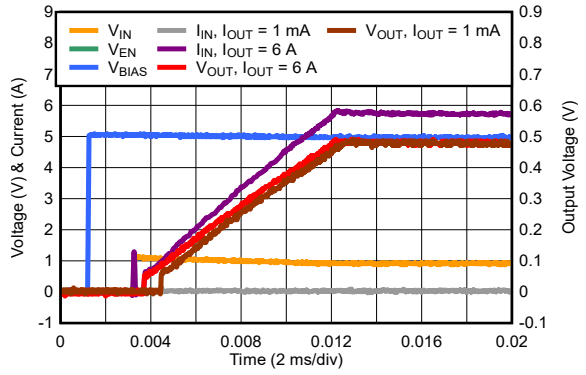
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 9V, V_{IN} = 5.5V, $V_{OUT(nom)}$ = 5.2V

Figure 5-31. Start-Up Undercurrent Limit



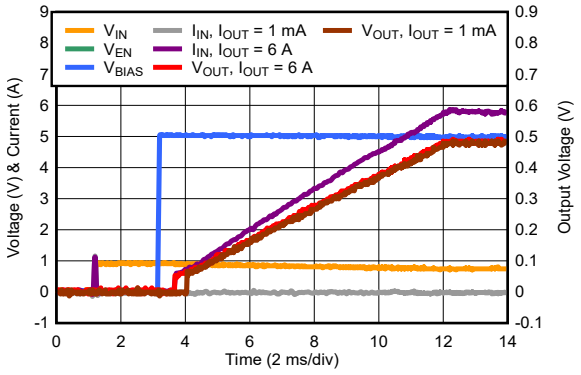
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{IN} = 0.8V, V_{OUT} = 0.5V

Figure 5-32. Start-Up for BIAS-EN-IN Rail Sequence for CP Disabled



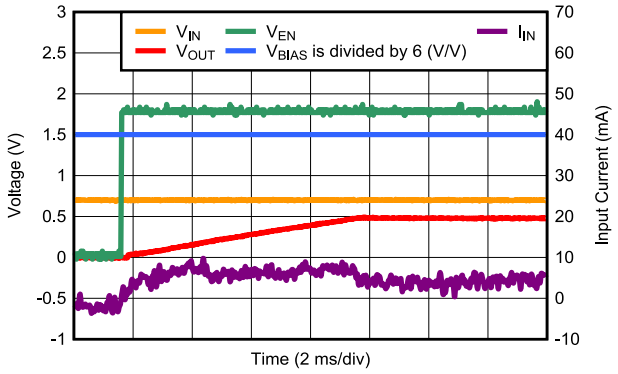
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{IN} = 0.8V, V_{OUT} = 0.5V

Figure 5-33. Start-Up for EN-BIAS-IN Rail Sequence for CP Disabled



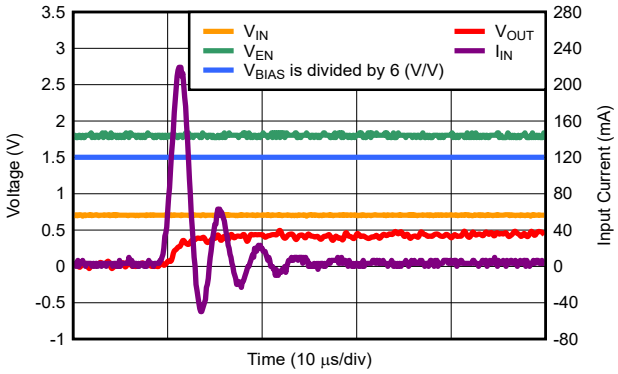
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{IN} = 0.8V, V_{OUT} = 0.5V

Figure 5-34. Start-Up for EN-IN-BIAS Rail Sequence for CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{IN} = 0.7V, V_{OUT} = 0.5V

Figure 5-35. Inrush Current for CP Disabled, V_{OUT} = 0.5V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 5V, V_{IN} = 0.7V, V_{OUT} = 0.5V

Figure 5-36. Inrush Current for CP Disabled, V_{OUT} = 0.5V, First 500µs

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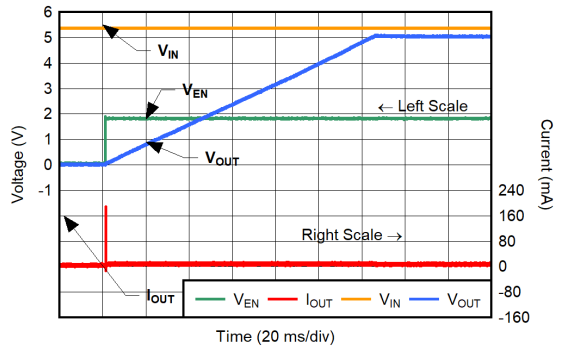
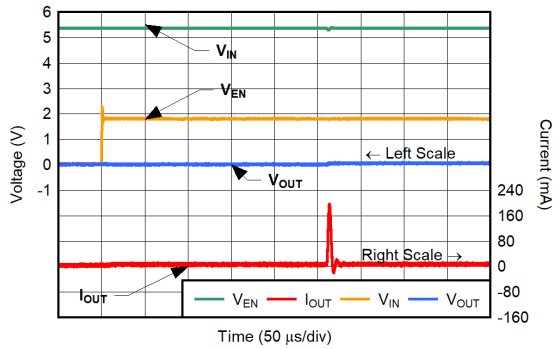
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



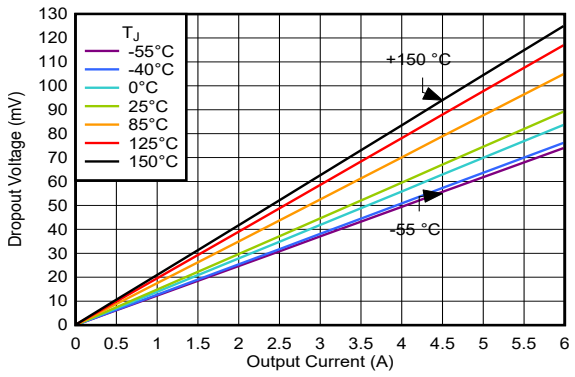
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 9V, V_{IN} = 5.5V, V_{OUT} = 5.2V

Figure 5-37. Inrush Current for CP Disabled, V_{OUT} = 5.2V



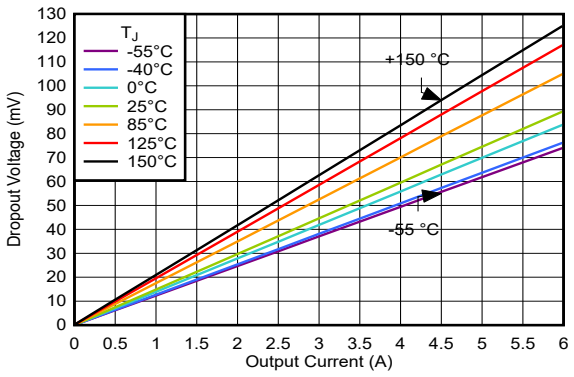
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 9V, V_{IN} = 5.5V, V_{OUT} = 5.2V

Figure 5-38. Inrush Current for CP Disabled, V_{OUT} = 5.2V, First 500µs



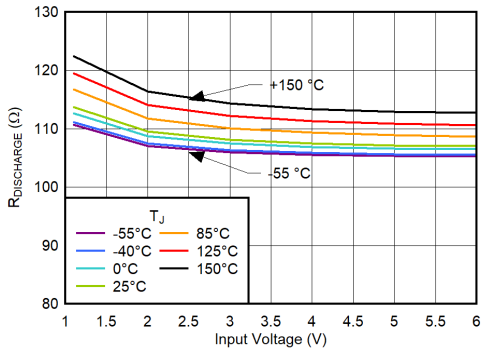
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V

Figure 5-39. Dropout Voltage vs I_{OUT} for CP Disabled, V_{IN} = 0.7V, V_{BIAS} = 3.9V



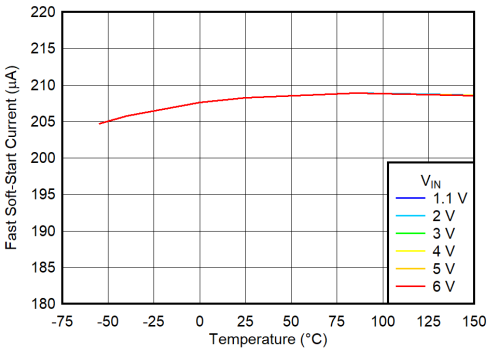
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V

Figure 5-40. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 1.1V, No Bias



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V

Figure 5-41. Output Discharge Resistor vs V_{IN}



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 0V

Figure 5-42. Fast Soft-Start Current vs Temperature and V_{IN}

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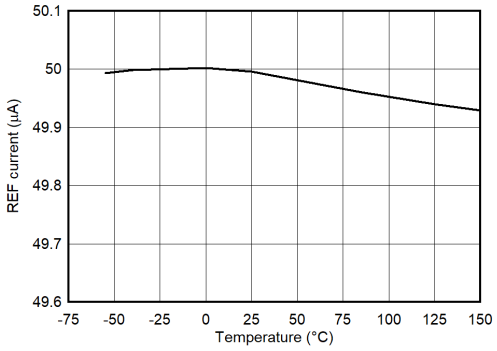
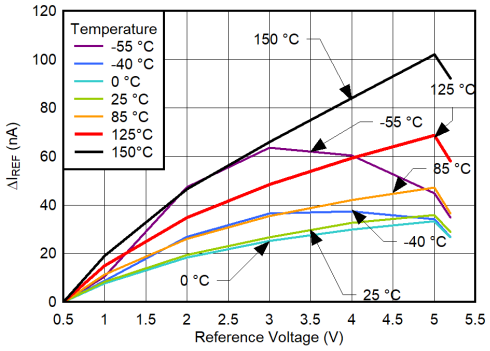
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



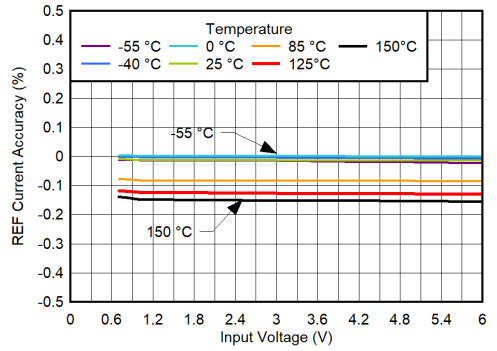
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{IN} = 1.1V

Figure 5-43. Reference Current vs Temperature



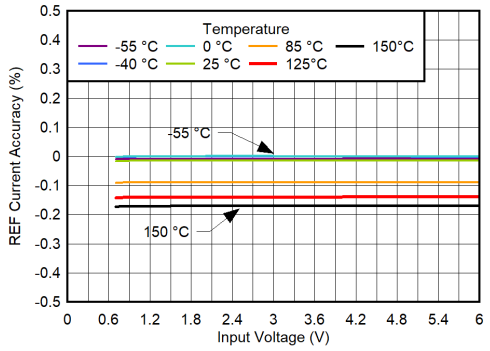
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{IN} = 6V, I_{OUT} = 0A

Figure 5-44. Change in Reference Current vs V_{REF}



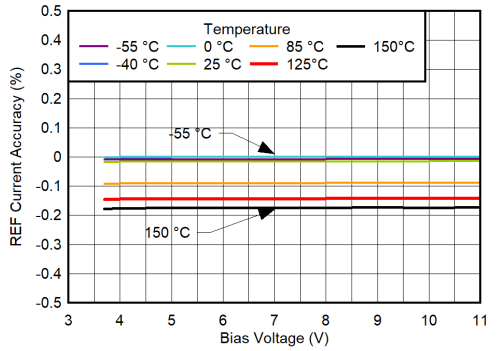
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 3V, V_{OUT} = 0.5V

Figure 5-45. Reference Current Accuracy vs V_{IN} for CP Enabled



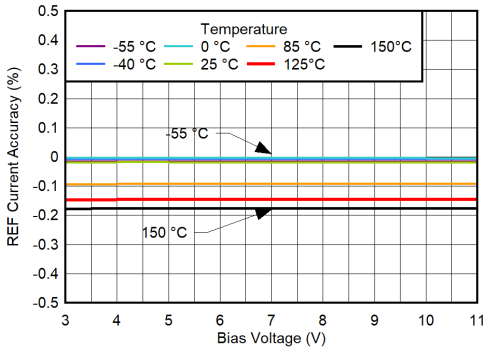
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V, V_{OUT} = 0.5V

Figure 5-46. Reference Current Accuracy vs V_{IN} for CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{IN} = 0.7V, V_{OUT} = 0.5V

Figure 5-47. Reference Current Accuracy vs V_{BIAS} for CP Disabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{IN} = 0.7V, V_{OUT} = 0.5V

Figure 5-48. Reference Current Accuracy vs V_{BIAS} for CP Enabled, I_{OUT} = 0A

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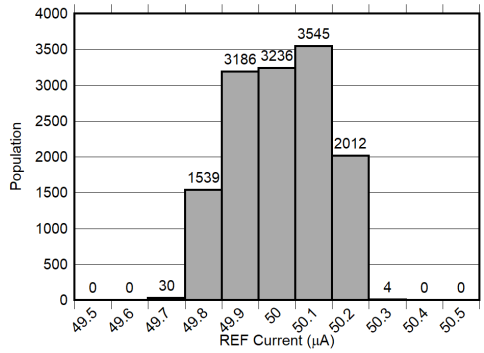
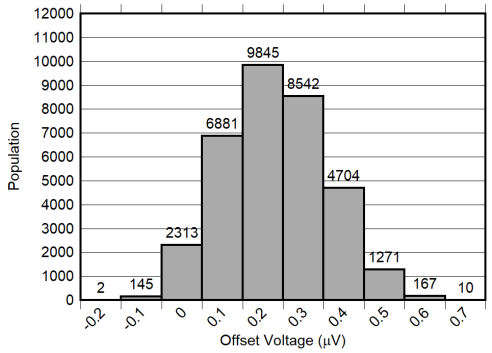
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



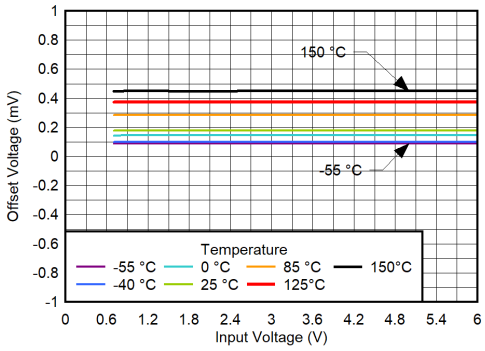
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-49. I_{REF} Distribution



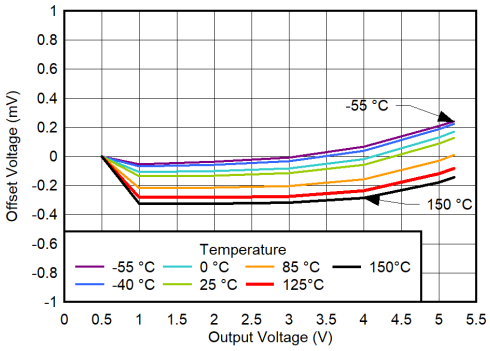
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-50. V_{OS} Distribution



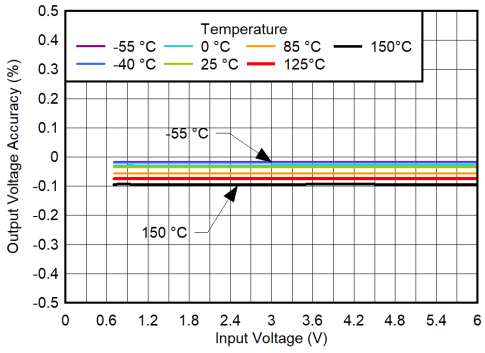
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-51. Offset Voltage vs V_{IN}



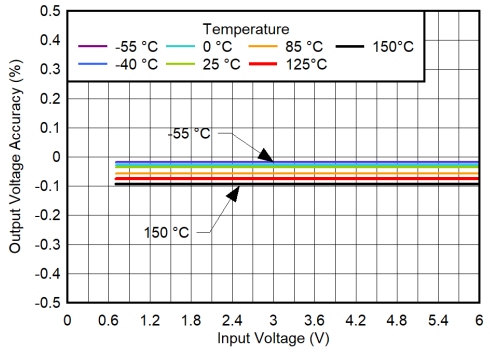
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 0V, V_{IN} = 6V, I_{OUT} = 0A

Figure 5-52. Offset Voltage vs V_{OUT}



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 11V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-53. Output Voltage Accuracy vs V_{IN} for V_{BIAS} = 11V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-54. Output Voltage Accuracy vs V_{IN} for V_{BIAS} = 3.7V, CP Disabled

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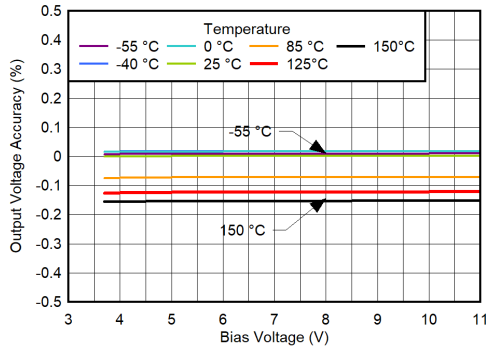
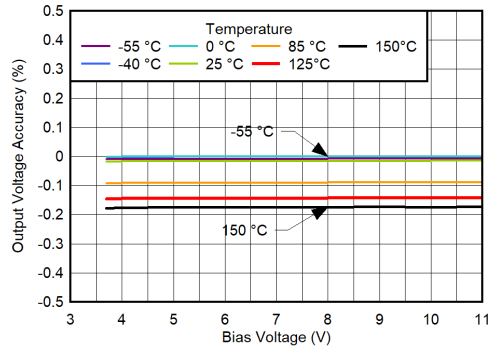
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



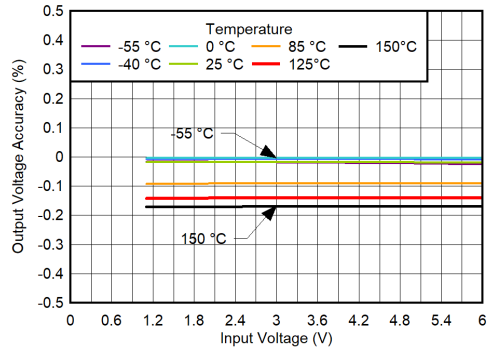
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{IN} = 6V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-55. Output Voltage Accuracy vs V_{BIAS} for V_{IN} = 6V, CP Disabled



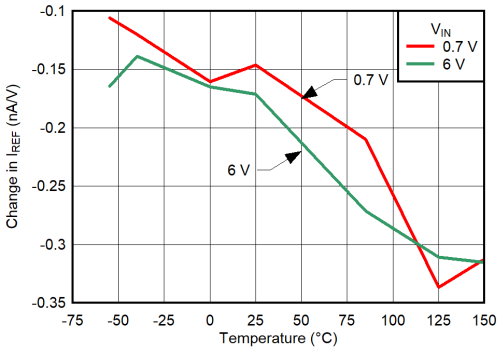
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{IN} = 0.7V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-56. Output Voltage Accuracy vs V_{BIAS} for V_{IN} = 0.7V, CP Disabled



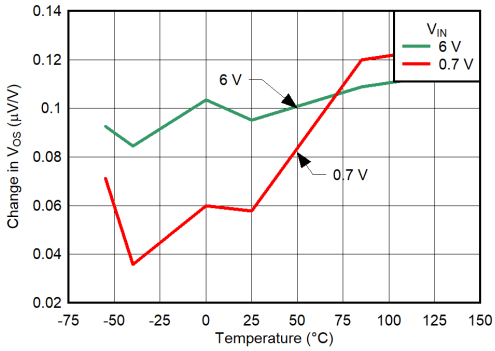
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{BIAS} = 0V, V_{IN} = 0.7V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-57. Output Voltage Accuracy vs V_{IN} for CP Enabled



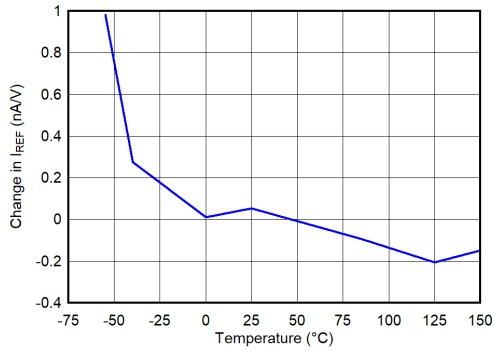
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V to 11V, V_{OUT} = 0.5V

Figure 5-58. I_{REF} BIAS Rail Line Regulation



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{BIAS} = 3.7V to 11V, V_{OUT} = 0.5V

Figure 5-59. V_{OS} BIAS Rail Line Regulation



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{IN} = 1.1V to 6V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-60. I_{REF} IN Rail Line Regulation

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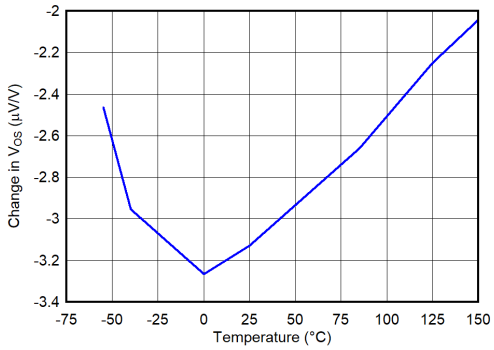
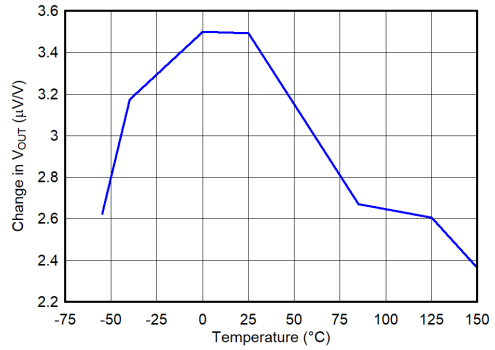
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



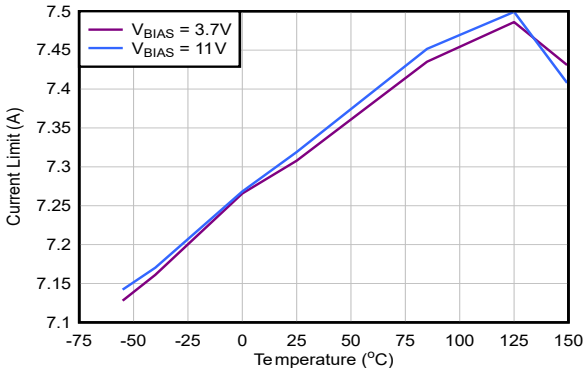
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{IN} = 1.1V to 6V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-61. V_{OS} IN Rail Line Regulation



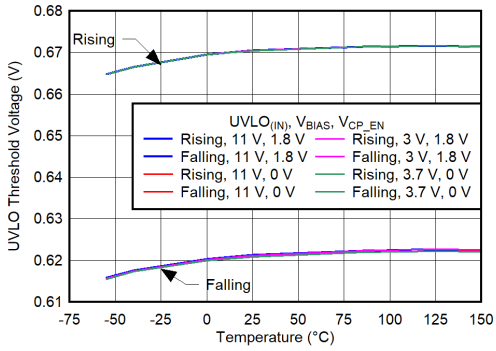
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{IN} = 1.1V to 6V, V_{OUT} = 0.5V, I_{OUT} = 0A

Figure 5-62. V_{OUT} IN Rail Line Regulation



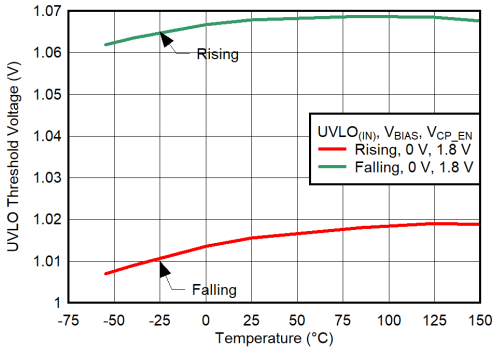
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-63. I_{LIMIT} vs Temperature



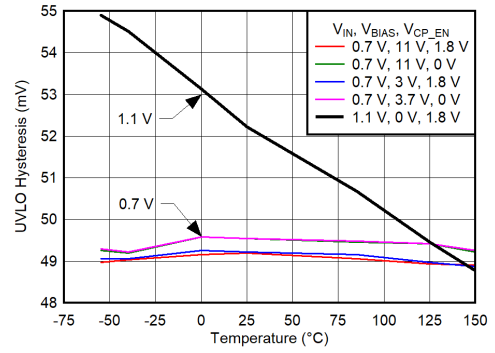
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-64. $UVLO_{IN}$ Threshold vs Temperature With BIAS Rail



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-65. $UVLO_{IN}$ Threshold vs Temperature Without BIAS Rail



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-66. $UVLO_{IN}$ Hysteresis vs Temperature

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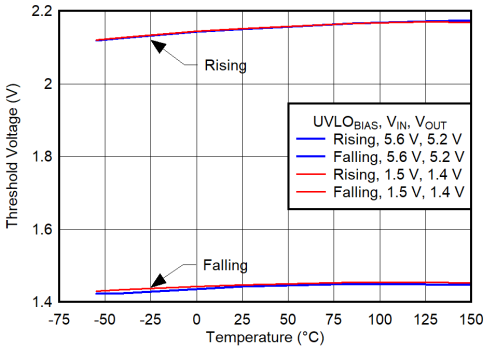
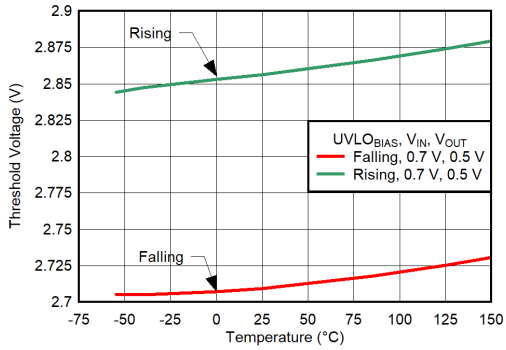
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



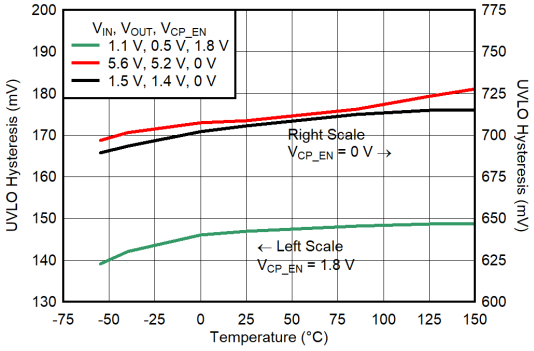
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-67. $UVLO_{BIAS}$ Threshold vs Temperature for CP Disabled



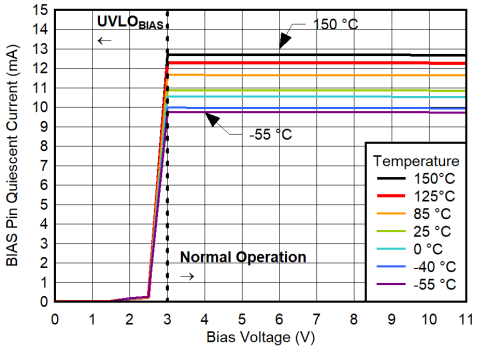
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-68. $UVLO_{BIAS}$ Threshold vs Temperature for CP Enabled



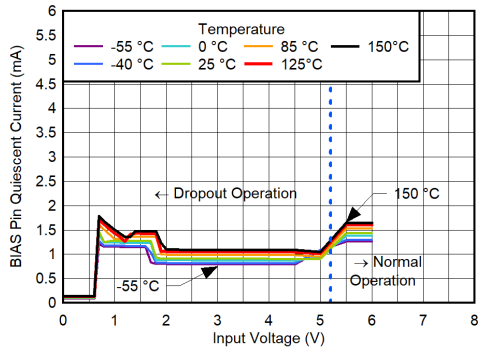
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-69. $UVLO_{IN}$ Hysteresis vs Temperature



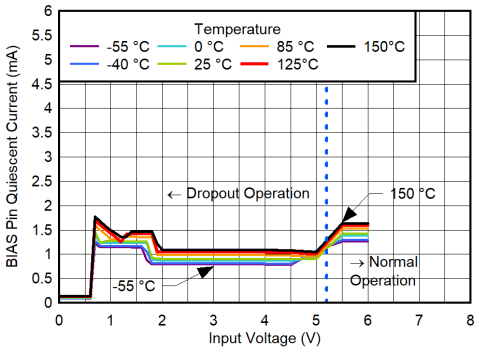
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-70. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, CP Enabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-71. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2V, V_{BIAS} = 11V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-72. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2V, V_{BIAS} = 8.4V, CP Disabled

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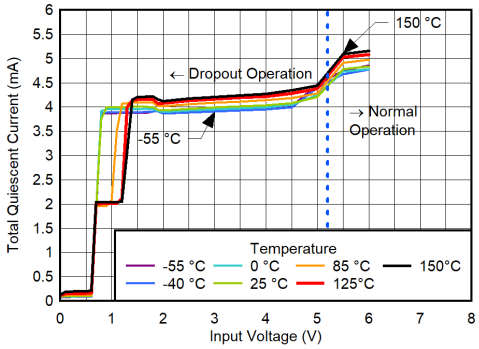
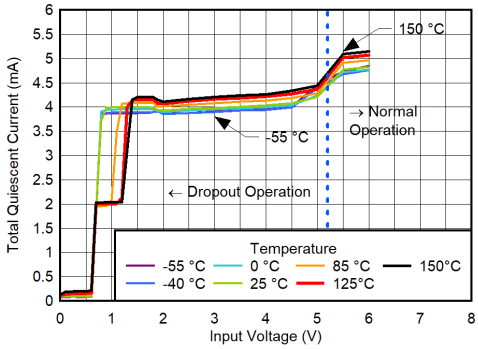
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



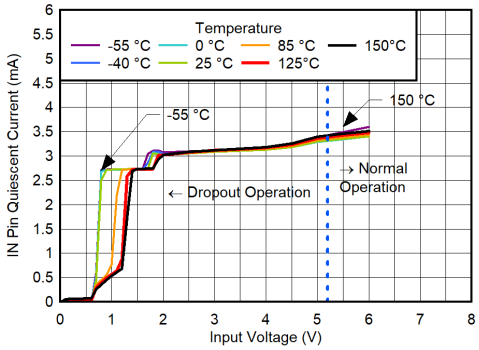
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-73. Total BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2V, V_{BIAS} = 11V, CP Disabled



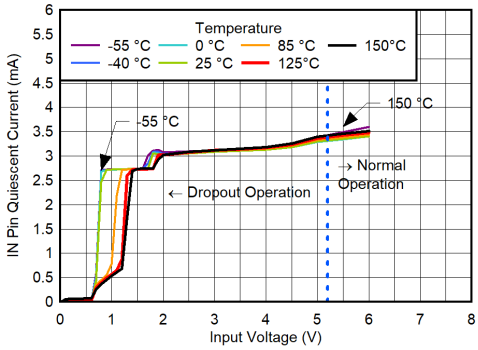
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-74. Total Quiescent Current vs V_{IN} for V_{OUT} = 5.2V, V_{BIAS} = 8.4V, CP Disabled



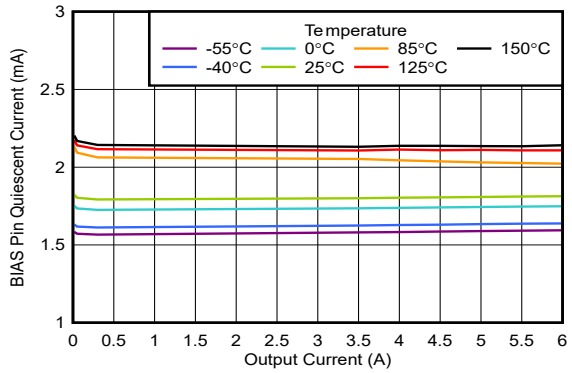
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-75. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2V, V_{BIAS} = 11V, CP Disabled



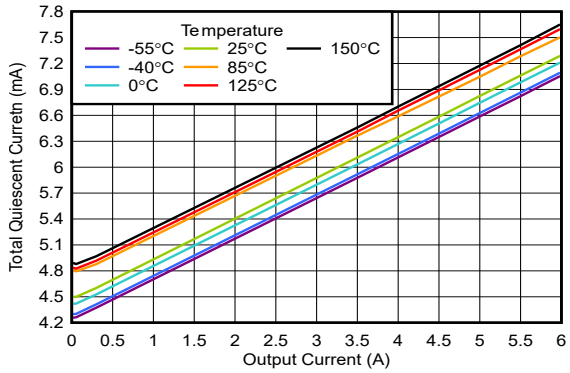
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-76. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2V, V_{BIAS} = 8.4V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{IN} = 0.7V

Figure 5-77. BIAS Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{IN} = 0.7V

Figure 5-78. Total Quiescent Current vs I_{OUT} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled

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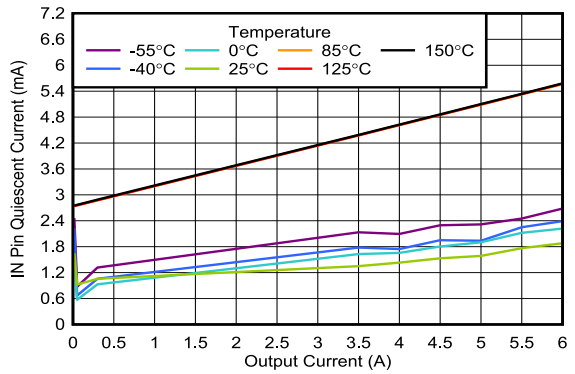
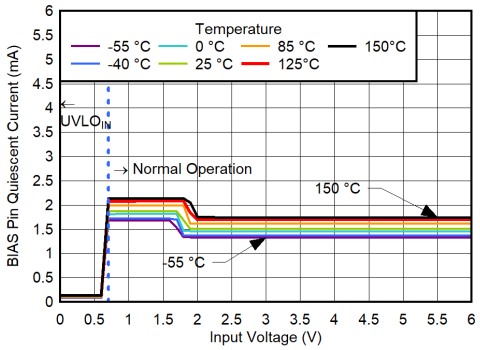
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



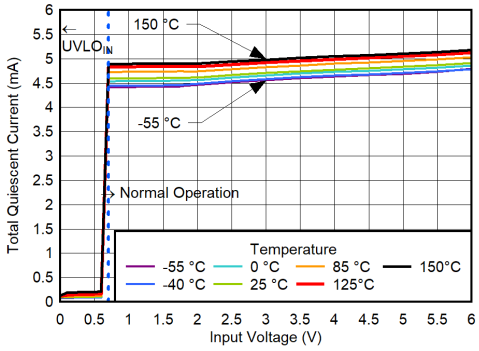
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{IN} = 6V

Figure 5-79. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



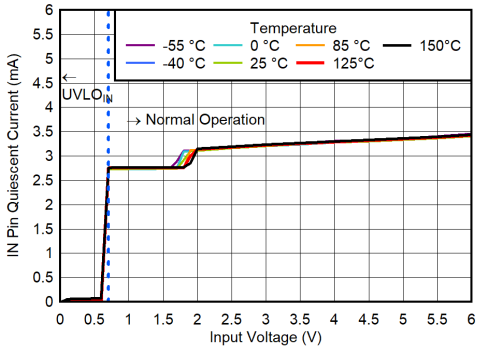
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-80. BIAS Pin Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



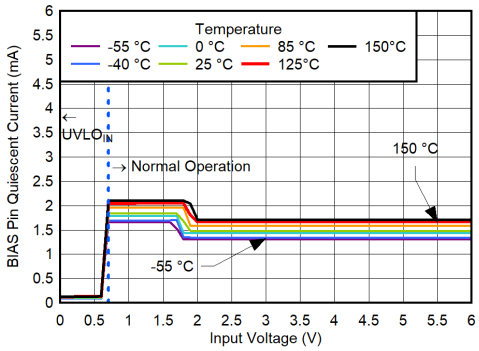
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-81. Total Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



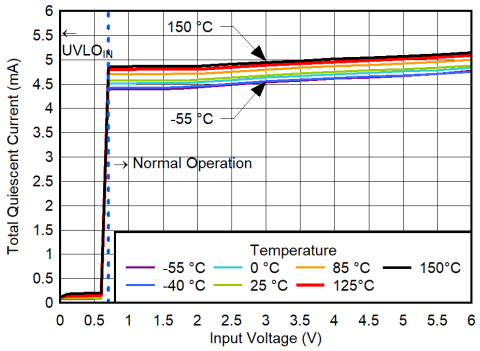
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-82. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-83. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3.7V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-84. Total Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3.7V, CP Disabled

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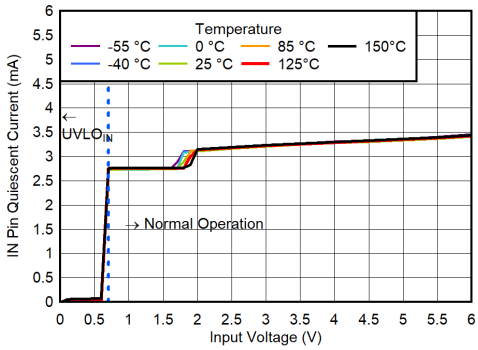
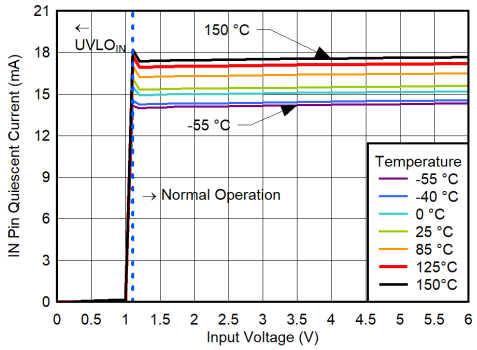
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



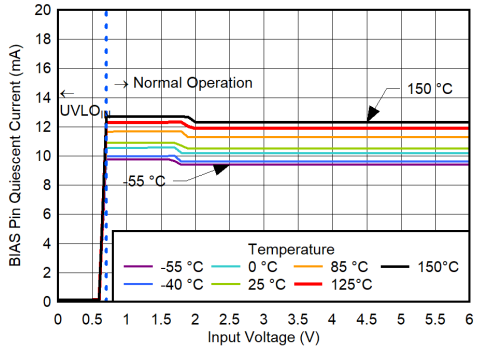
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-85. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3.7V, CP Disabled



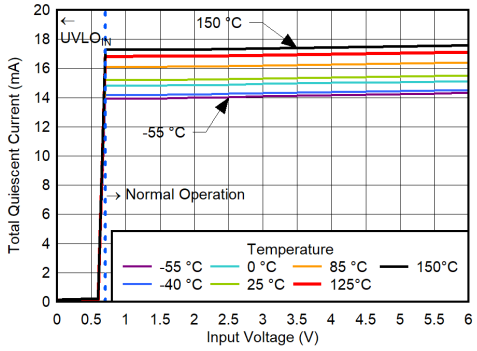
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-86. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, No BIAS, CP Enabled, I_{OUT} = 0A



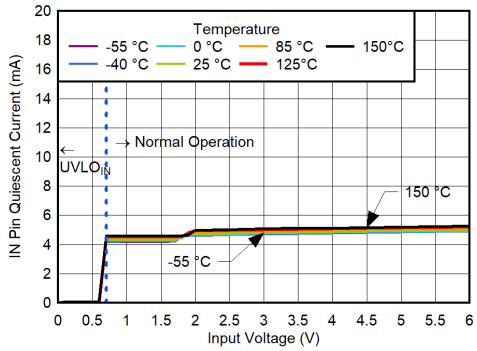
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-87. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3V, CP Enabled, I_{OUT} = 0A



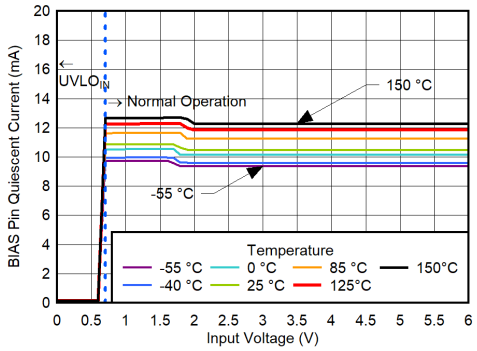
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-88. Total Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3V, CP Enabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-89. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3V, CP Enabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-90. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Enabled, I_{OUT} = 0A

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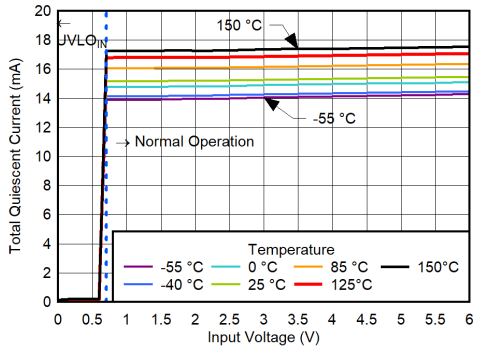
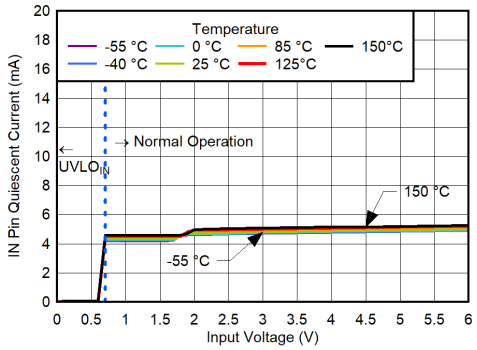
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



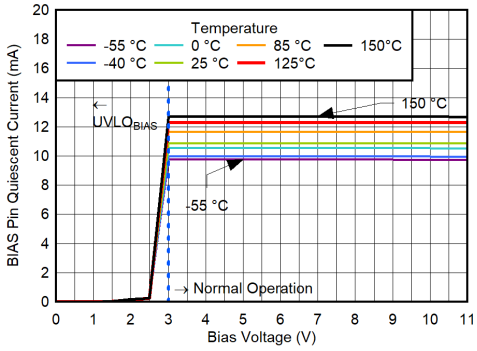
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-91. Total Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Enabled, I_{OUT} = 0A



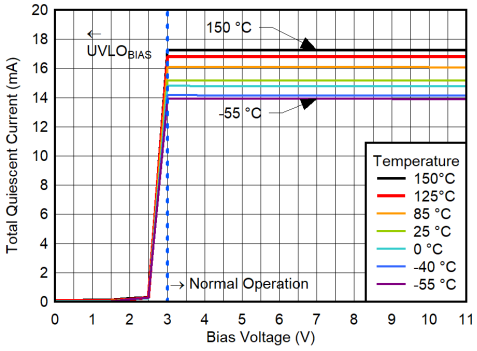
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-92. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Enabled, I_{OUT} = 0A



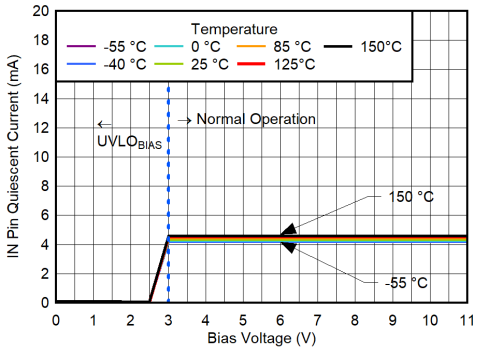
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-93. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 0.7V, CP Enabled, I_{OUT} = 0A



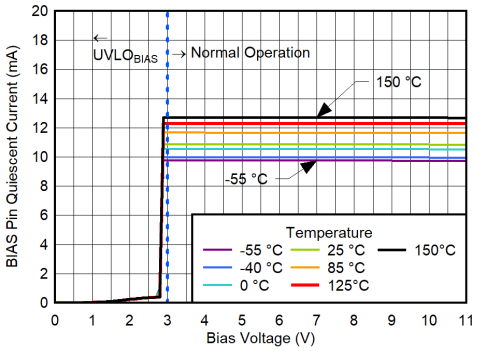
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-94. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 0.7V, CP Enabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-95. IN Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 0.7V, CP Enabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-96. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 1.1V, CP Enabled, I_{OUT} = 0A

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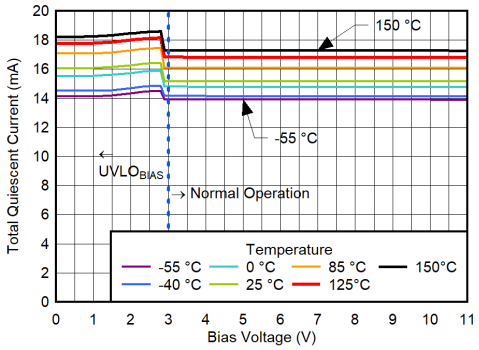
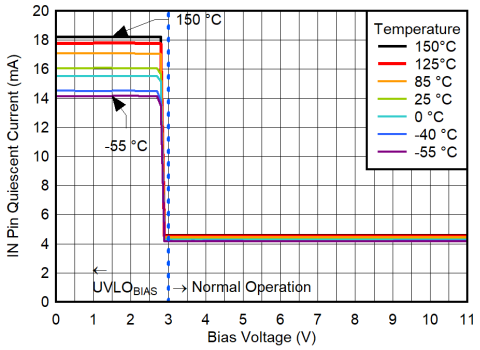
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



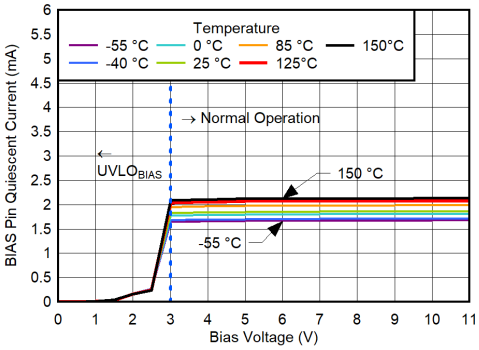
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-97. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 1.1V, CP Enabled, I_{OUT} = 0A



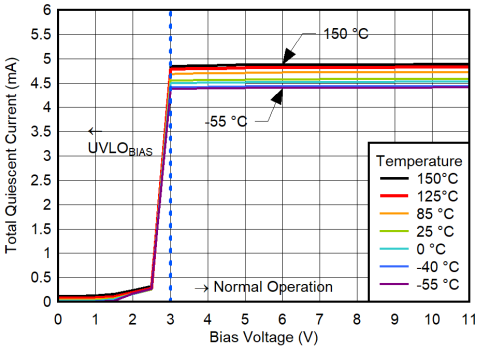
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-98. IN Pin Quiescent Current vs Bias Voltage for V_{OUT} = 0.5V, V_{IN} = 1.1V, CP Enabled, I_{OUT} = 0A



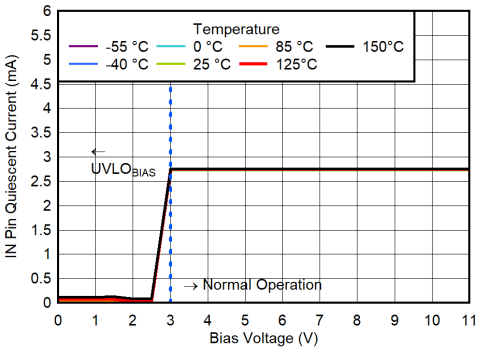
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-99. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 0.7V, CP Disabled, I_{OUT} = 0A



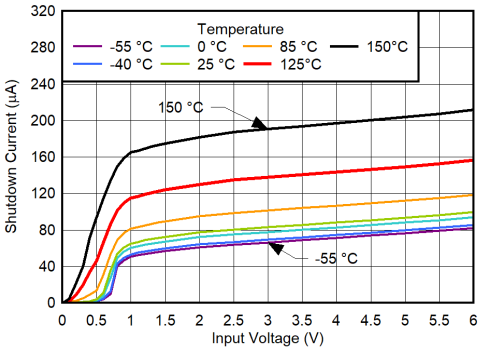
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-100. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 0.7V, CP Disabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-101. IN Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5V, V_{IN} = 0.7V, CP Disabled, I_{OUT} = 0A



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-102. Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 0V, CP Enabled

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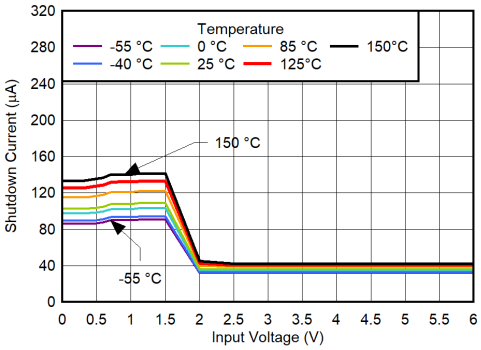
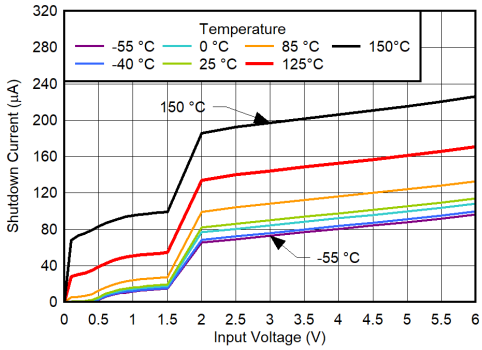
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



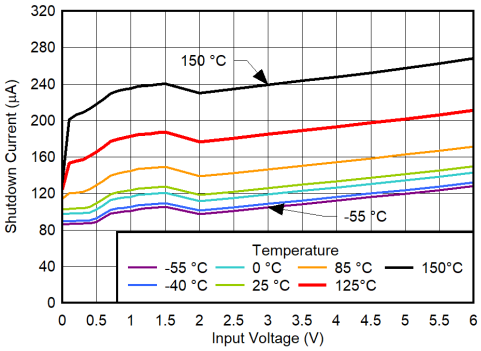
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0.4V, V_{EN} = 0.4V

Figure 5-103. BIAS Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



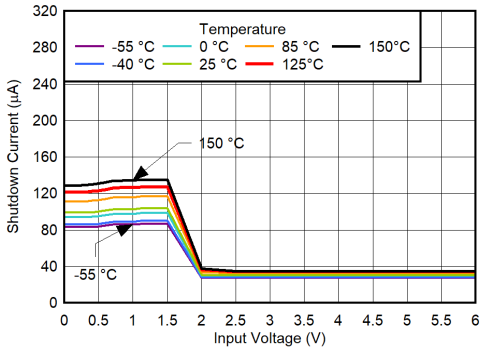
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0.4V, V_{EN} = 0.4V

Figure 5-104. IN Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



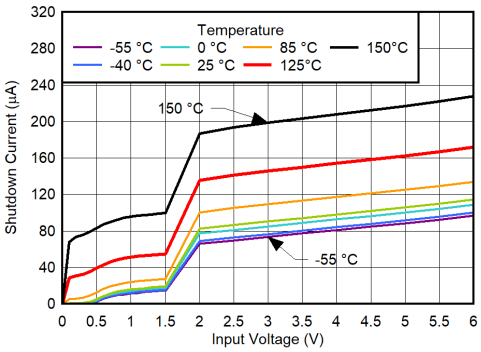
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0.4V, V_{EN} = 0.4V

Figure 5-105. Total Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 11V, CP Disabled



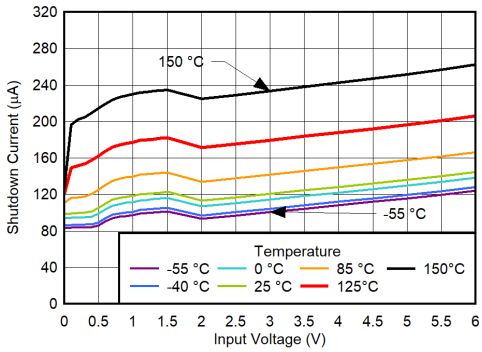
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-106. BIAS Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3V, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-107. IN Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3V, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-108. Total Shutdown Current vs V_{IN} for V_{OUT} = 0.5V, V_{BIAS} = 3V, CP Enabled

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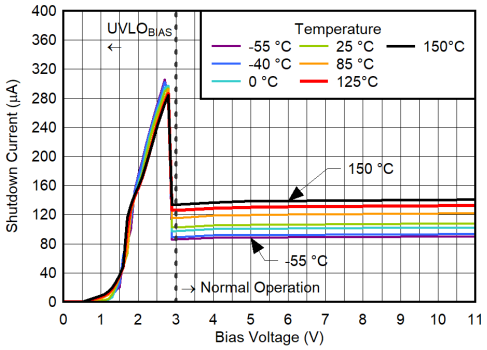
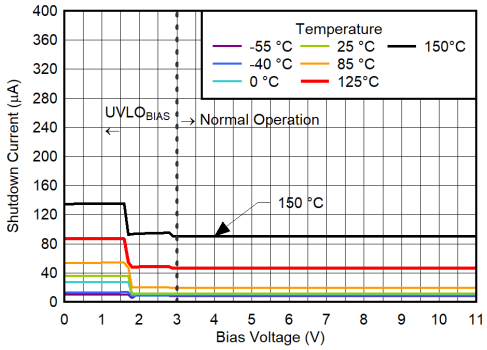
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



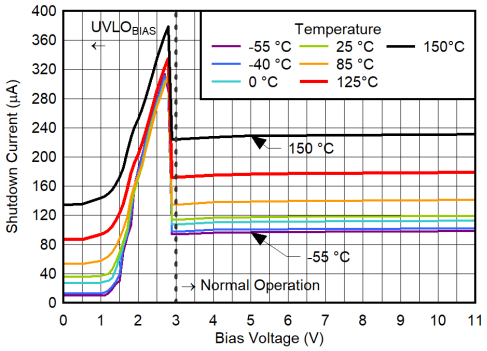
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-109. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7V, V_{OUT} = 0.5V, CP Enabled



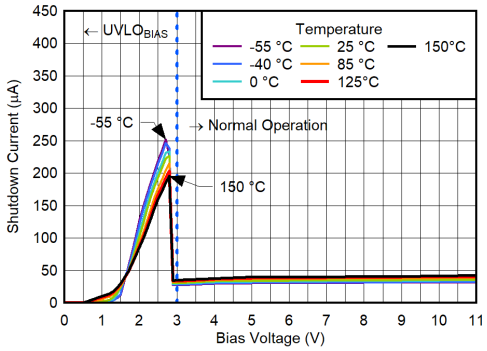
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-110. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7V, V_{OUT} = 0.5V, CP Enabled



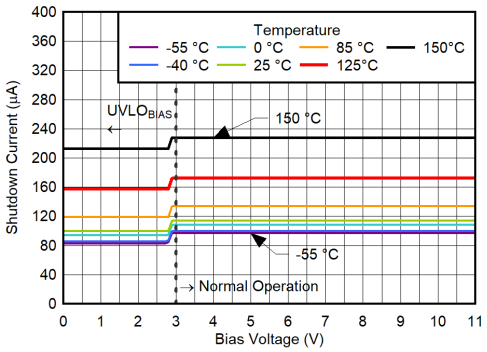
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-111. Total Shutdown Current vs V_{BIAS} for V_{IN} = 0.7V, V_{OUT} = 0.5V, CP Enabled



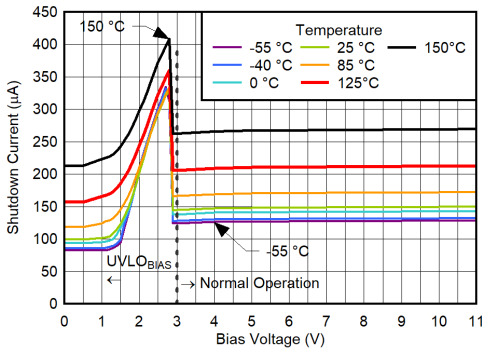
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-112. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 6V, $V_{OUT(nom)}$ = 0.5V, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-113. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 6V, $V_{OUT(nom)}$ = 0.5V, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 1.8V, V_{EN} = 0.4V

Figure 5-114. Total Shutdown Current vs V_{BIAS} for V_{IN} = 6V, $V_{OUT(nom)}$ = 0.5V, CP Enabled

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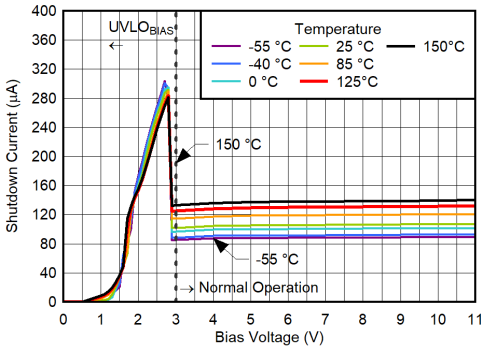
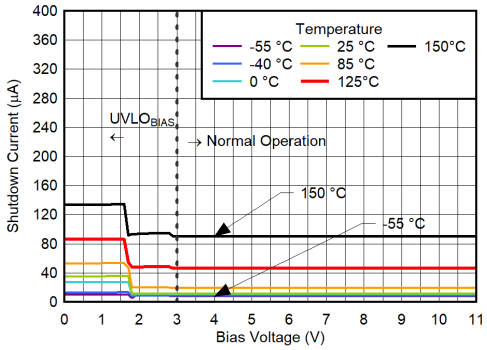
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



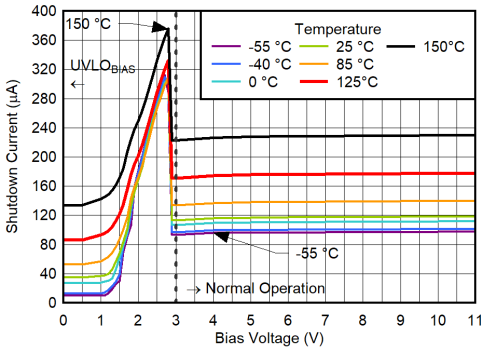
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{EN} = 0.4V

Figure 5-115. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7V, $V_{OUT(nom)}$ = 0.5V, CP Disabled



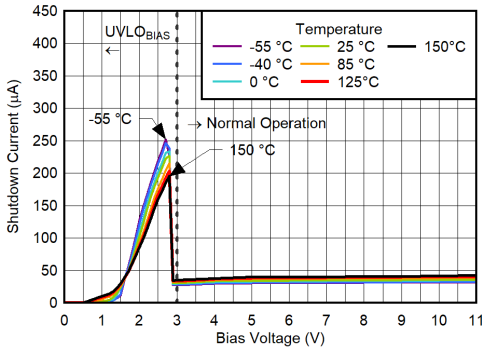
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{EN} = 0.4V

Figure 5-116. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7V, $V_{OUT(nom)}$ = 0.5V, CP Disabled



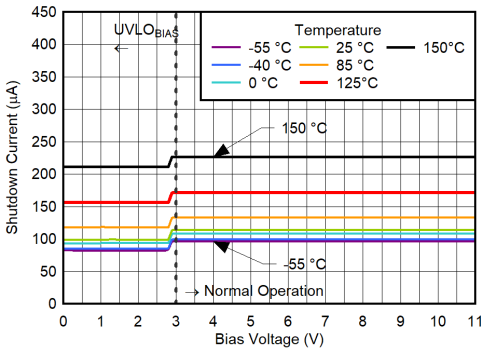
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{EN} = 0.4V

Figure 5-117. Total Shutdown Current vs V_{BIAS} for V_{IN} = 0.7V, $V_{OUT(nom)}$ = 0.5V, CP Disabled



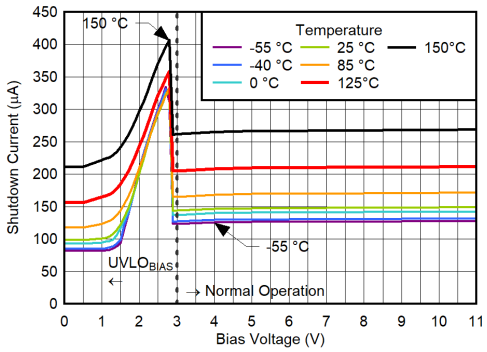
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{EN} = 0.4V

Figure 5-118. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 6V, $V_{OUT(nom)}$ = 0.5V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{EN} = 0.4V

Figure 5-119. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 6V, $V_{OUT(nom)}$ = 0.5V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = 0V, V_{EN} = 0.4V

Figure 5-120. Total Shutdown Current vs V_{BIAS} for V_{IN} = 6V, $V_{OUT(nom)}$ = 0.5V, CP Disabled

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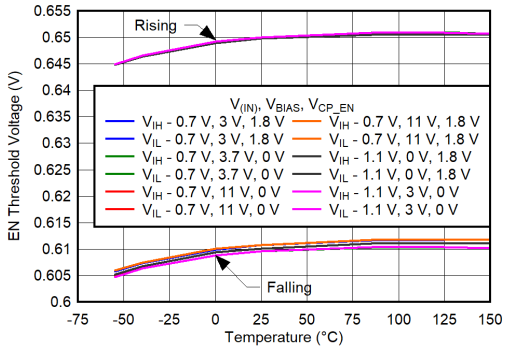
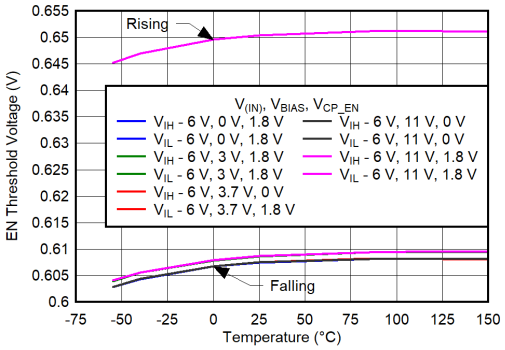
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



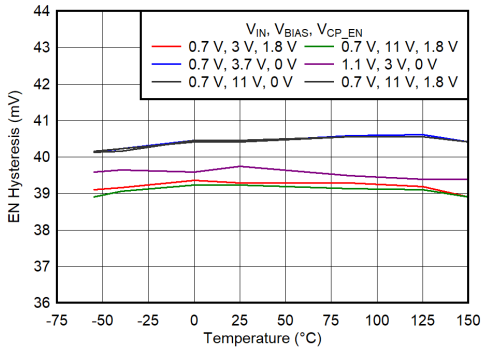
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-121. EN Threshold Voltage vs Temperature for V_{IN} = 0.7V and 1.1V, V_{OUT} = 0.5V



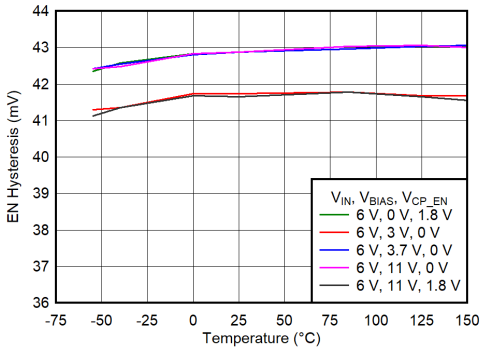
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-122. EN Threshold Voltage vs Temperature for V_{IN} = 6V, V_{OUT} = 0.5V



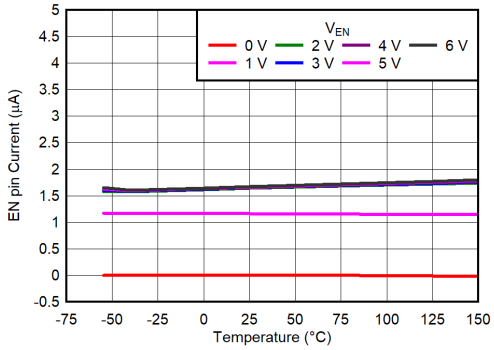
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-123. EN Hysteresis vs Temperature for V_{IN} = 0.7V and 1.1V, V_{OUT} = 0.5V



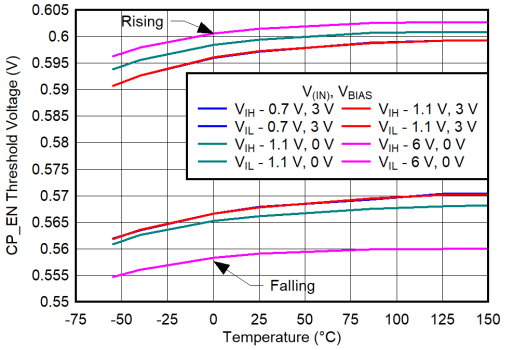
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-124. EN Hysteresis vs Temperature for V_{IN} = 6V, V_{OUT} = 0.5V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-125. EN Pin Current vs Temperature



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-126. CP_EN Threshold Voltage vs Temperature

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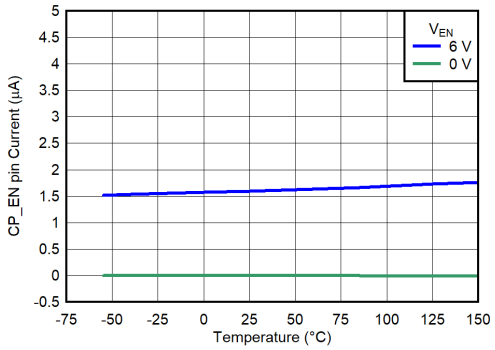
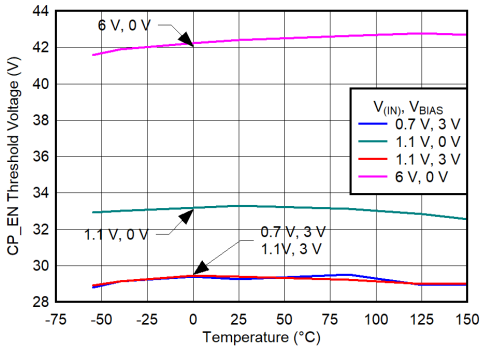
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



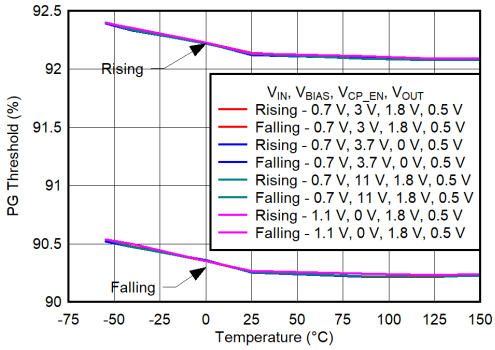
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-127. CP_EN Pin Current vs Temperature



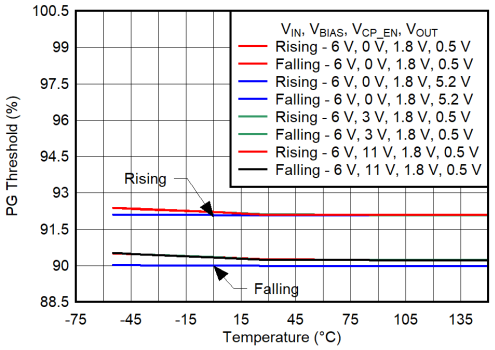
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-128. CP_EN Hysteresis vs Temperature



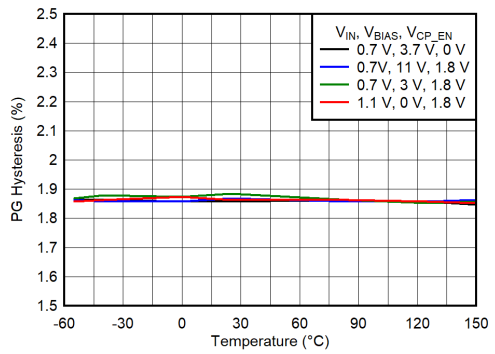
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-129. PG Threshold Voltage vs Temperature for V_{IN} = 0.7V and 1.1V



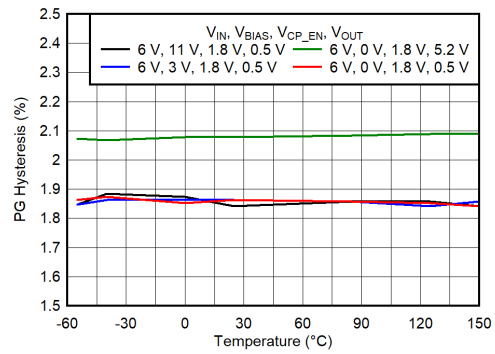
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-130. PG Threshold Voltage vs Temperature for V_{IN} = 6V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-131. PG Hysteresis vs Temperature for V_{IN} = 0.7V and 1.1V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-132. PG Hysteresis vs Temperature for V_{IN} = 6V

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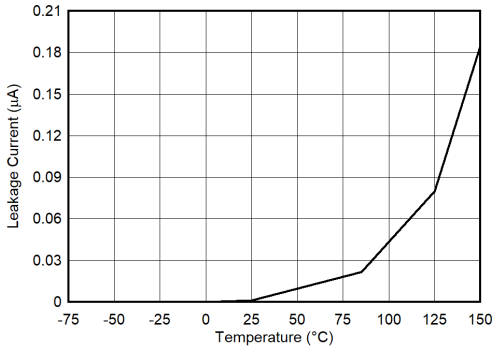
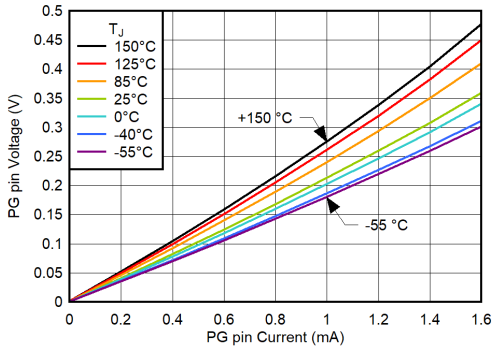
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



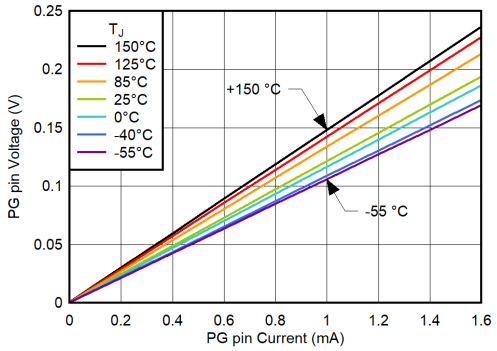
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF

Figure 5-133. PG Leakage Current vs Temperature



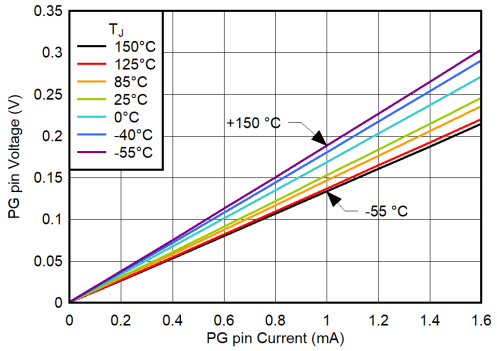
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{BIAS} = 0V, V_{OUT} = 0.5V, V_{CP_EN} = 1.8V

Figure 5-134. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 1.1V, No BIAS



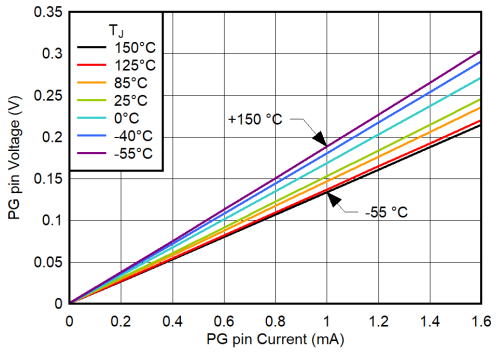
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{BIAS} = 0V, V_{OUT} = 0.5V, V_{CP_EN} = 1.8V

Figure 5-135. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 6V, No BIAS



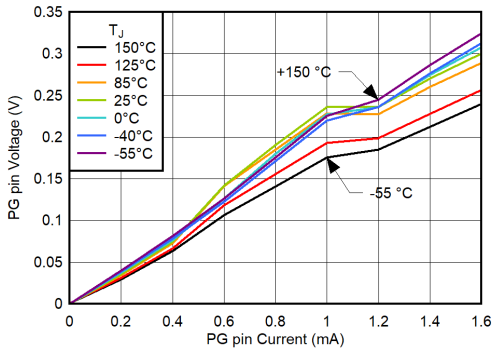
$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-136. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7V, V_{BIAS} = 3.7V, V_{CP_EN} = 0V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-137. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7V, V_{BIAS} = 11V, V_{CP_EN} = 0V



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-138. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7V, V_{BIAS} = 3V, V_{CP_EN} = 1.8V

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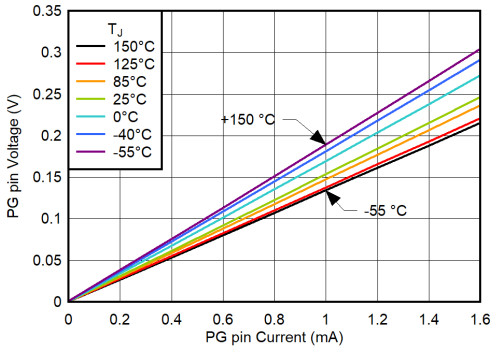
5.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4V, V_{EN} = 1.8V, V_{CP_EN} = 1.8V, C_{IN} = 10µF, $C_{NR/SS}$ = 4.7µF, C_{OUT} = 22µF, C_{BIAS} = 0nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted); typical values are at T_J = 25°C



$C_{NR/SS}$ = C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{OUT} = 0.5V

Figure 5-139. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7V, V_{BIAS} = 11V, V_{CP_EN} = 1.8V

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6 Detailed Description

6.1 Overview

The TPS7A56 is a low-noise (2.45μV_{RMS} over 10Hz to 100kHz bandwidth), ultra-high PSRR (> 36dB to 1MHz), high-accuracy (1%), ultra-low-dropout (LDO) linear voltage regulator. This device has an input range of 0.7V to 6.0V and an output voltage range from 0.5V to 5.0V. This device uses innovative circuitry to achieve wide bandwidth and high loop gain, resulting in ultra-high PSRR even with very low operational headroom. This headroom is calculable as [V_{OpHr} = (V_{IN} – V_{OUT})]. At a high level, the device has two main primary features and a few secondary features. The primary features are the current reference and the unity-gain LDO buffer. The secondary features are the adjustable soft-start inrush control, precision enable, charge pump enable, and PG pin.

The current reference is controlled by the REF pin. This pin sets the output voltage with a single resistor.

The NR/SS pin sets the start-up time and filters the noise generated by the reference and external set resistor.

The unity-gain LDO buffer controls the output voltage. The low noise does not increase with output voltage and provides wideband PSRR. As such, the SNS pin is only used for remote sensing of the load.

Use the low-noise current reference, 50μA typical, in conjunction with an external resistor (R_{REF}) to set the output voltage. This process allows the output voltage range to be set from 0.5V to 5.0V. To achieve low noise and allow for a soft-start inrush, place an external capacitor, $C_{NR/SS}$ (typically 4.7μF), on the NR/SS pin. When start-up is completed and the switch between REF and NR/SS is closed, the $C_{NR/SS}$ capacitor is in parallel with the R_{REF} resistor. This resistor attenuates the band-gap noise and sets the output voltage. This unity-gain LDO provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

The EN pin sets the precision enable feature; a resistor divider on this pin selects the optimal input voltage at which the device starts. There are three independent undervoltage lockout (UVLO) voltages in this device. These voltages are the internal fixed UVLO thresholds for the IN and BIAS rails, and the externally adjustable UVLO threshold using the EN pin.

The CP_EN pin enables or disables the internal charge pump. The TPS7A56 does not allow operation below 1.1V without a BIAS rail. If the charge pump is disabled, a minimum operating headroom between OUT and BIAS is required.

This regulator offers current limit, thermal protection, and is fully specified from –40°C to +125°C. This device is offered in a 16-pin WQFN, 3mm × 3mm thermally efficient package.

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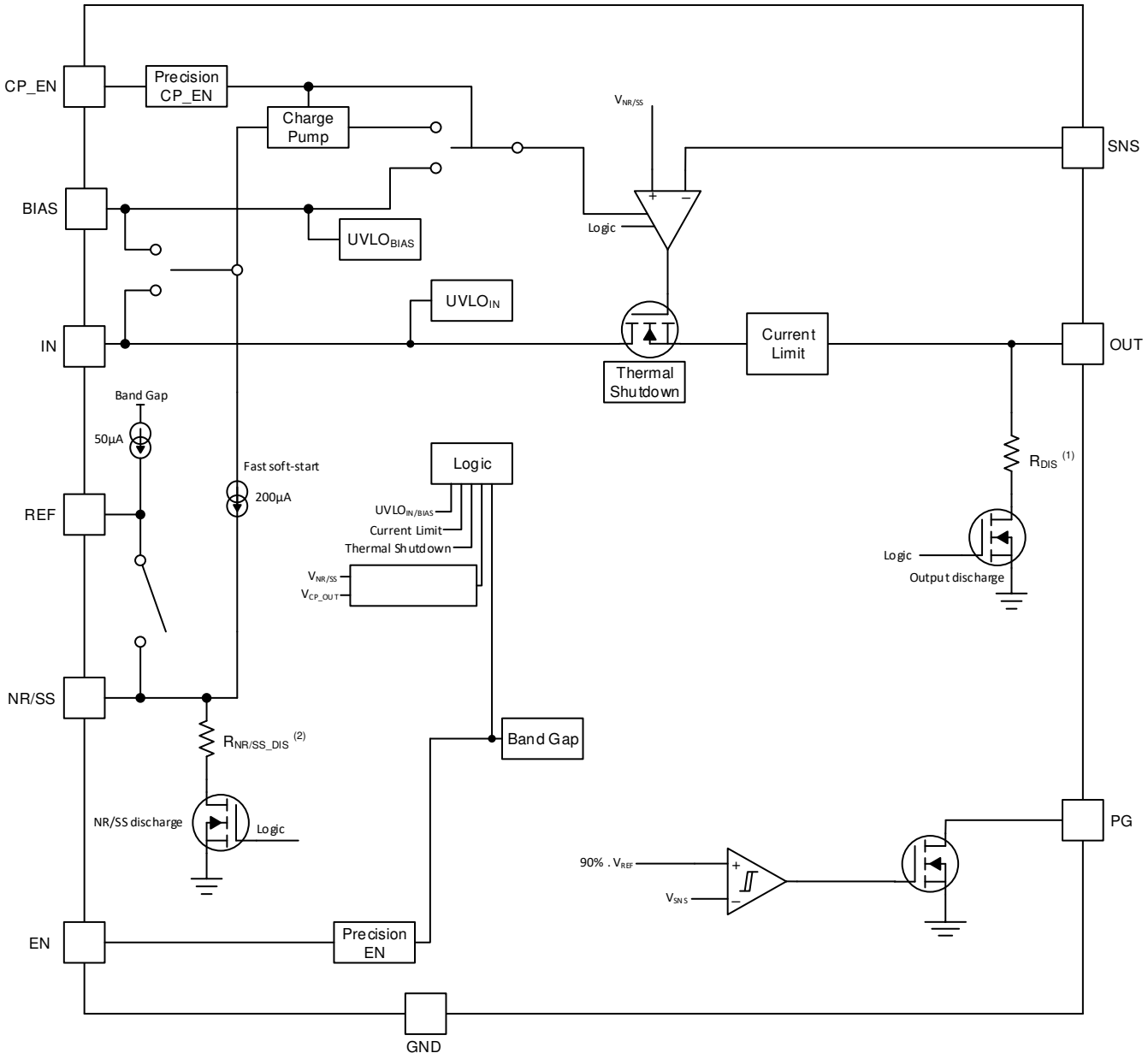
6.2 Functional Block Diagram



A. See the R_{DIS} (the output pin active discharge resistance) value in the *Electrical Characteristics* table.

B. See the R_{NR/SS_DIS} (the NR/SS pin active discharge resistance) value in the *Electrical Characteristics* table.

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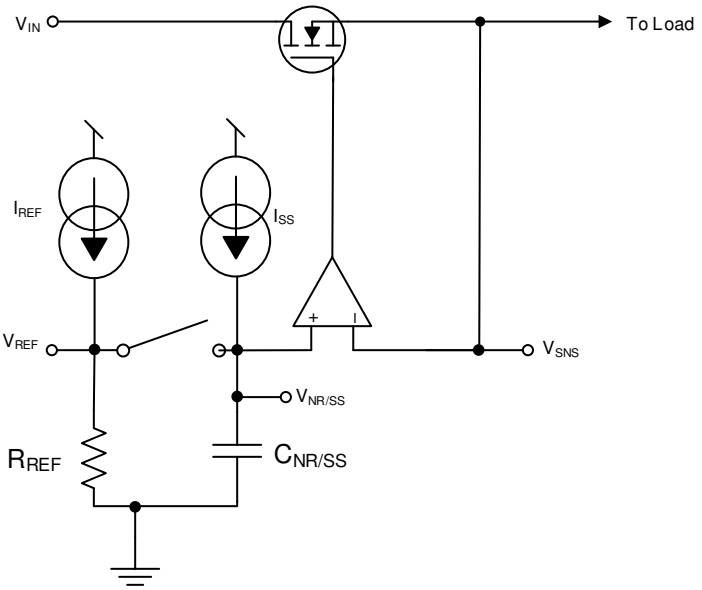
6.3 Feature Description

6.3.1 Output Voltage Setting and Regulation

Figure 6-1 shows a simplified regulation circuit. The input signal (V_{REF}) is generated by the internal current source (I_{REF}) and the external resistor (R_{REF}). The LDO output voltage is programmed by the V_{REF} voltage because the error amplifier always operates in unity-gain configuration. The V_{REF} reference voltage is generated by an internal low-noise current source driving the R_{REF} resistor. V_{REF} is designed to have very low bandwidth at the input to the error amplifier by using a low-pass filter ($C_{NR/SS}$ || R_{REF}).

The unity-gain configuration is achieved by connecting SNS to OUT. Minimize trace inductance on the output and connect C_{OUT} as close to the output as possible.



$V_{OUT} = I_{REF} \times R_{REF}$.

Figure 6-1. Simplified Regulation Circuit

This unity-gain configuration, along with the highly accurate I_{REF} reference current, allows the device to achieve excellent output voltage accuracy. The low dropout voltage (V_{DO}) provides reduced thermal dissipation and achieves robust performance. This combination of features make this device an excellent voltage source for powering sensitive analog low-voltage (≤ 5.5V) devices.

6.3.2 Low-Noise, Ultra-High Power-Supply Rejection Ratio (PSRR)

The device architecture features a highly accurate, high-precision, low-noise current reference followed by a state-of-the-art, complementary metal oxide semiconductor (CMOS) error amplifier. This CMOS error amplifier is 6nV/$\sqrt{\text{Hz}}$ at 10kHz noise for V_{OUT} ≥ 0.5V. Unlike previous-generation LDOs, the unity-gain configuration of this device provides low noise over the entire output voltage range. Additional noise reduction and higher output current is achieved by placing multiple TPS7A56 LDOs in parallel. See the *Paralleling for Higher Output Current and Lower Noise* section.

6.3.3 Programmable Soft-Start (NR/SS Pin)

The device features a programmable, monotonic, current-controlled, soft-start circuit. This circuit uses the $C_{NR/SS}$ capacitor to minimize inrush current into the output capacitor and load during start-up. This circuitry reduces the start-up time for applications that require the output voltage to reach at least 90% of the set value for fast system start-up. See the *Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)* section for more details.

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6.3.4 Precision Enable and UVLO

Depending on the circuit implementation, up to three independent undervoltage lockout (UVLO) voltage circuits are potentially active. An internally set UVLO on the input supply (IN pin) and the bias supply (BIAS pin) automatically disables the LDO when the input voltage reaches the minimum threshold. The precision EN function (EN pin) also functions as a user-programmable UVLO. This programmability includes:

1. The internal input supply voltage UVLO circuit prevents the regulator from turning on when the input voltage is not high enough. See the *Electrical Characteristics* table for more details.
2. The internal bias supply voltage UVLO circuit prevents the regulator from turning on when the bias voltage is not high enough. See the *Electrical Characteristics* table for more details.
3. The precision enable circuit allows a simple sequencing of multiple power supplies with a resistor divider from another supply. Use this enable circuit to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN pin. See the *Precision Enable (External UVLO)* section for more details.

6.3.5 Charge Pump Enable and BIAS Rail

This device allows the internal charge pump to be disabled for systems that cannot tolerate any switching noise.

When V_{IN} is less than 1.1V, the BIAS rail is required because this rail sources the current needed by the internal circuitry. The charge pump is either enabled or disabled. Consider adequate operating headroom requirements from OUT to BIAS if the charge pump is disabled. See the *Undervoltage Lockout (UVLO) Operation* section for more details.

When V_{IN} is greater than or equal to 1.1V, the CP_EN pin connection determines how the internal circuitry is powered. If CP_EN is connected to GND (CP disabled), the internal circuitry is powered from the BIAS rail. See the *Undervoltage Lockout (UVLO) Operation* section for more details. If CP_EN is connected to the supply (CP enabled), any current required to power the internal circuitry comes from the IN pin. As such, leave the BIAS pin open.

6.3.6 Power-Good Pin (PG Pin)

The PG pin is an output indicating if the LDO is ready to provide power. This pin is implemented using an open-drain architecture. During the start-up phase, the PG voltage threshold is set by the REF voltage when the fast soft-start is ongoing . The PG threshold is set by the NR/SS voltage when the fast soft-start is completed and the switch between REF and NR/SS is closed.

As shown in the *Functional Block Diagram*, the PG pin is implemented by comparing the SNS pin voltage to an internal reference voltage. As such, the PG pin is considered a voltage indicator reflecting the output voltage status.

For PG pin implementation, see the *Power-Good Functionality* section.

6.3.7 Active Discharge

To quickly discharge internal nodes, the device incorporates two internal pulldown metal-oxide semiconductor field effect transistors (MOSFETs). The first pulldown MOSFET connects a resistor (R_{DIS}) from OUT to ground when the device is disabled to actively discharge the output capacitor. The second pulldown MOSFET connects a resistor from NR/SS (R_{NR/SS_DIS}) to ground when the device is disabled and discharges the NR/SS capacitor. Both pulldown MOSFETs are activated by any of the following events:

- Driving the EN pin below the $V_{EN(LOW)}$ threshold
- The IN pin voltage falling below the undervoltage lockout $V_{UVLO(IN)}$ threshold
- The BIAS pin voltage falling below the undervoltage lockout $V_{UVLO(BIAS)}$ threshold

Note

A brownout event on BIAS during a low-input, low-output (LILO) operation (< $1.1V_{IN}$) results in incomplete $C_{NR/SS}$ discharge. Consider the time constant on both the NR/SS and OUT pins for a proper system shutdown procedure.

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6.3.8 Thermal Shutdown Protection (T_{SD})

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The bias voltage is greater than the nominal output voltage plus the OUT-to-BIAS dropout voltage. This condition occurs if the charge pump is disabled or if the input voltage is less than 1.1V. The OUT-to-BIAS dropout voltage is defined as $V_{OUT(nom)} + V_{DO(BIAS)}$.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$).
- The voltage on the EN pin has previously exceeded the $V_{IH(EN)}$ threshold voltage and has not yet decreased to less than the enable falling threshold.

Table 6-1 summarizes all valid modes of operation and shows what rail is sourcing the internal biasing current.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER					
	V_{IN}	V_{BIAS}	V_{CP_EN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT(nom)} + V_{DO}$ and $V_{IN} \geq V_{UVLO(IN)}$	$V_{BIAS} \geq V_{OUT} + 3.2V$	$V_{CP_EN} \geq V_{IH(CP_EN)}$	$V_{EN} \geq V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{BIAS} < V_{OUT} + 3.2V$	$V_{CP_EN} > V_{IH(CP_EN)}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{CP_EN} < V_{IL(CP_EN)}$	$V_{EN} < V_{IL(EN)}$	-	$T_J \geq T_{SD}$ for shutdown

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6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

Note

If the charge pump is disabled, maintain a minimum UVLO (BIAS) voltage above the REF voltage. A voltage greater than or equal to the 3V BIAS rail is required. However, this requirement is only needed when the charge pump is enabled and the IN voltage is less than 1.1V. If the charge pump is enabled and the IN voltage is greater than or equal to 1.1V, a BIAS rail is not required.

For additional information, see the *Undervoltage Lockout (UVLO) Operation* section.

6.4.3 Disabled

Shutdown the device output by forcing the voltage of the EN pin to less than the $V_{IH(EN)}$ threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and both the NR/SS and OUT pin voltages are actively discharged to ground. These pin voltages are discharged by internal discharge circuits to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

6.4.4 Current-Limit Operation

If the output current is greater than or equal to the minimum current limit ($I_{LIM(Min)}$), then the device operates in current-limit mode. Current limit is a foldback implementation.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

7.1.1 Precision Enable (External UVLO)

The precision enable circuit (EN pin) turns the device on and off. As shown in Figure 7-1, use this circuit to set an external undervoltage lockout (UVLO) voltage. This circuit turns the device on and off using a resistor divider between IN (or BIAS when the charge pump is disabled), EN, and GND.

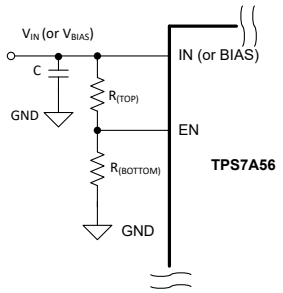

Figure 7-1. Precision EN Used as an External UVLO

Use this external UVLO solution to prevent the device from turning on when the input supply voltage is not high enough. The external UVLO places the device in dropout operation. This solution also allows simple sequencing of multiple power supplies with a resistor divider from another supply. Because this pin does not have an internal pulldown resistor, the EN pin is never left floating. This condition provides another benefit from using a resistor divider to enable or disable the device. However, place a zener diode between the EN pin and ground if needed to comply with the absolute maximum ratings on this pin.

Use Equation 1 and Equation 2 to determine the correct resistor values.

$$V_{ON} = V_{OFF} \times [(V_{IH(EN)} + V_{HYS(EN)}) / V_{EN}] \quad (1)$$

$$R_{(TOP)} = R_{(BOTTOM)} \times (V_{ON} / V_{IH(EN)} - 1) \quad (2)$$

where:

- V_{OFF} is the input or bias voltage where the regulator turns off
- V_{ON} is the input or bias voltage where the regulator turns on

Note

For the EN pin input current, I_{EN}, effects are ignored.

7.1.2 Undervoltage Lockout (UVLO) Operation

Table 7-1 lists the UVLO thresholds for different modes of operation.

Table 7-1. Relative Threshold for Different Modes of Operation

UVLO THRESHOLD	UVLO THRESHOLD (typ) WITH CHARGE PUMP OFF	UVLO THRESHOLD (typ) WITH CHARGE PUMP ON AND WITHOUT BIAS	UVLO THRESHOLD (typ) WITH CHARGE PUMP ON AND BIAS
$V_{UVLO(IN)}$ rising	0.67V	1.07V	0.67V
$V_{UVLO(BIAS)}$ rising	V_{REF} + 2.1V	N/A	Max (V_{REF} + 2.1V, 2.8V)

7.1.2.1 IN Pin UVLO

The IN pin UVLO (UVLO(IN)) circuit makes sure the device remains disabled before the input supply reaches the minimum operational voltage range. This circuit also makes sure that the device shuts down when the input supply falls too low.

The UVLO(IN) circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.67V causes the input supply UVLO(IN) to assert for a short time. However, the UVLO(IN) circuit does not have enough stored energy to fully discharge the internal circuits inside the device. The OUT and NR/SS capacitors therefore are poentially incompletely discharged.

Note

The effect of the downward line transient triggers the overshoot prevention circuit. This effect is easily mitigated by using the solution proposed in the *Precision Enable (External UVLO)* section.

7.1.2.2 BIAS UVLO

The BIAS pin UVLO (UVLO(BIAS)) circuit makes sure the device remains disabled before the input supply reaches the minimum operational voltage range. This circuit makes sure the device shuts down when the input supply falls too low.

The UVLO(BIAS) circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 2.8V or V_{REF} + 2.1V causes the input supply UVLO(BIAS) to assert for a short time. When this transient is below approximately 2.8V, enable the charge pump; when at V_{REF} + 2.1V, disable the charge pump. However, the UVLO(BIAS) circuit does not have enough stored energy to fully discharge the internal circuits inside of the device. Thus, potentially resulting in incomplete discharge of the OUT and NR/SS capacitors.

Note

The effect of the downward line transient triggers the overshoot prevention circuit. This effect is easily mitigated by using the solution proposed in the *Precision Enable (External UVLO)* section.

7.1.2.3 Typical UVLO Operation

Figure 7-2 illustrates the UVLO (IN or BIAS) circuit response to various input voltage events. The diagram is separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output potentially falls out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

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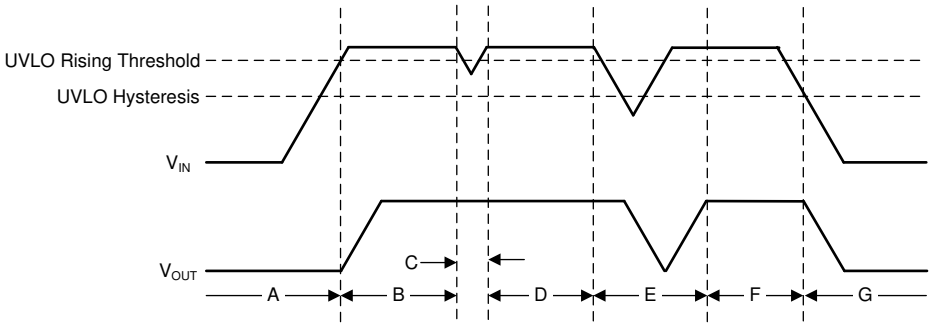

Figure 7-2. Typical UVLO Operation

7.1.2.4 UVLO(IN) and UVLO(BIAS) Interaction

A glitch potentially occurs on the output during the shutdown power-supply sequence if the BIAS rail falls prior to the IN rail. This error occurs when operating with IN between 1.07V and 1.1V with the internal charge pump on.

When the BIAS rail falls below the V_{UVLO_BIAS} threshold, the output is disabled. When the IN rail is above the minimum UVLO threshold to operate, the LDO restarts. Figure 7-3 shows this behavior.

To prevent this behavior, follow the proper turn-off power-supply sequence, or select an operating mode (such as charge pump disabled).

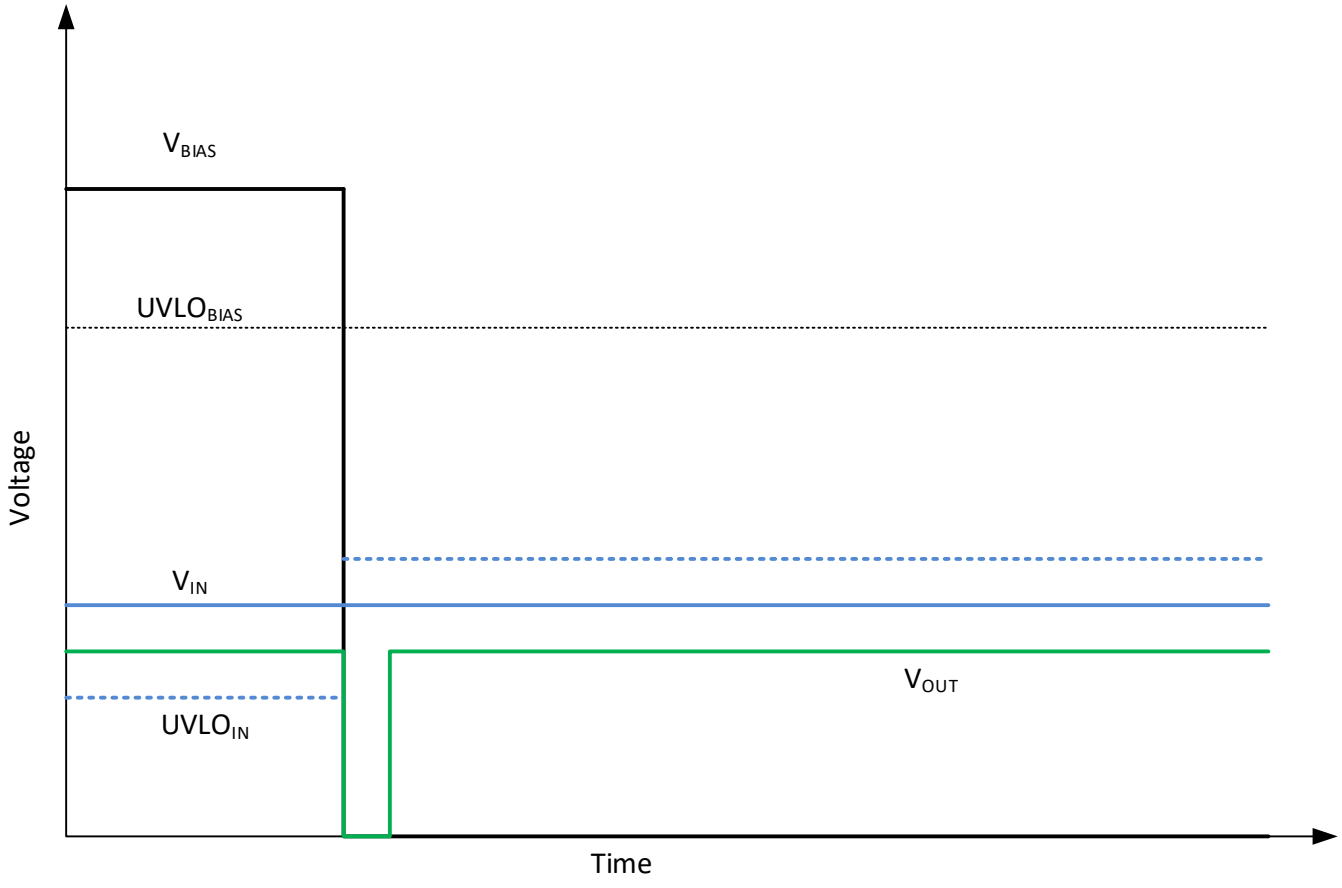

Figure 7-3. $UVLO_{IN}$ and $UVLO_{BIAS}$ Interaction

7.1.3 Dropout Voltage (V_{DO})

Generally speaking, dropout voltage (V_{DO}) often refers to the minimum voltage difference between the input and output voltage that is required for regulation. This minimum voltage difference is defined as $V_{DO} = V_{IN} – V_{OUT}$. When V_{IN} drops to or below the set V_{DO} for the given load current, the device functions as a resistive switch. In this state, the device does not regulate output voltage. When the device operates in dropout, the output voltage tracks the input voltage and dropout voltage (V_{DO}) is proportional to the output current. In this state, the device operates as a resistive switch. Operating the device at or near dropout significantly degrades the device transient performance and PSRR. Maintaining sufficient V_{OpHr} significantly improves device transient performance and PSRR.

Note

If the minimum BIAS rail is set 3.2V above V_{REF} with the internal charge pump disabled, the pass transistor cannot be in BIAS-to-OUT dropout. Thus leaving only the IN-to-OUT dropout conditions to be considered. V_{REF} is the reference pin voltage range, as defined by the *Recommended Operating Conditions* table. For other operating conditions, see the *Undervoltage Lockout (UVLO) Operation* section.

7.1.4 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A56 is designed and characterized for operation with 22µF or greater ceramic capacitors at the output and 1µF or greater at the input. Make sure the output capacitors have 15µF or greater of capacitance and the input capacitors have 5µF or greater of capacitance. Use at least a 10µF capacitor at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitics. Keep trace inductance from the input supply to the TPS7A56 low. A fast current transient causes V_{IN} to ring above the absolute maximum voltage rating and damage the device. Mitigate this situation by adding additional input capacitors to dampen the ringing, thereby keeping any voltage spike below the device absolute maximum ratings.

Note

Because of the wide bandwidth, the LDO error amplifier potentially reacts faster than the output capacitor. In such a case, the load behavior appears directly on the LDO supply, potentially dragging the supply down. To avoid such behaviors, minimize both ESR and ESL present on the output; see the *Recommended Operating Conditions* table.

7.1.5 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors. Use these capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%. At high V_{IN} and V_{OUT} conditions (V_{IN} = 5.5V to V_{OUT} = 5.0V) and temperature extremes, the derating is potentially greater than 50%. Take this derating potential into consideration.

The device requires input, output, and noise-reduction capacitors for proper device operation. Use the nominal or larger than nominal input and output capacitors. as specified in the *Recommended Operating Conditions* table. Place input and output capacitors as close as possible to the corresponding pin. Make capacitor GND connections as close as possible to the device GND pin to shorten transient currents on the return path. Using a larger input capacitor or a bank of capacitors with various values is always good design practice to counteract input trace inductance. This practice also improves transient response and reduces input ripple and noise.

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Similarly, multiple capacitors on the output reduce charge pump ripple and optimize PSRR; see the *Optimizing Noise and PSRR* section.

Use the nominal noise-reduction $C_{NR/SS}$ capacitor because using a larger C_{NRSS} capacitor lengthens the start-up time.

7.1.6 Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)

The NR/SS pin has dual functionality. This pin controls the soft-start time and reduces the noise generated by the internal band-gap reference and the external resistor R_{REF}. The NR/SS capacitor ($C_{NR/SS}$) reduces the output noise to very low levels and sets the output ramp rate to limit inrush current.

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor ($C_{NR/SS}$). In addition to the soft-start feature, the $C_{NR/SS}$ capacitor also lowers the output voltage noise of the LDO. Use the soft-start feature to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

To achieve a monotonic start up, the device output voltage tracks the $V_{NR/SS}$ reference voltage until this reference reaches the set value (the set output voltage). The $V_{NR/SS}$ reference voltage is set by the R_{REF} resistor. During start up, the device uses a fast charging current (I_{FAST_SS}), as shown in Figure 7-4, to charge the $C_{NR/SS}$ capacitor.

Note

Any leakage on the NR/SS and REF pins directly impacts the accuracy of the reference voltage.

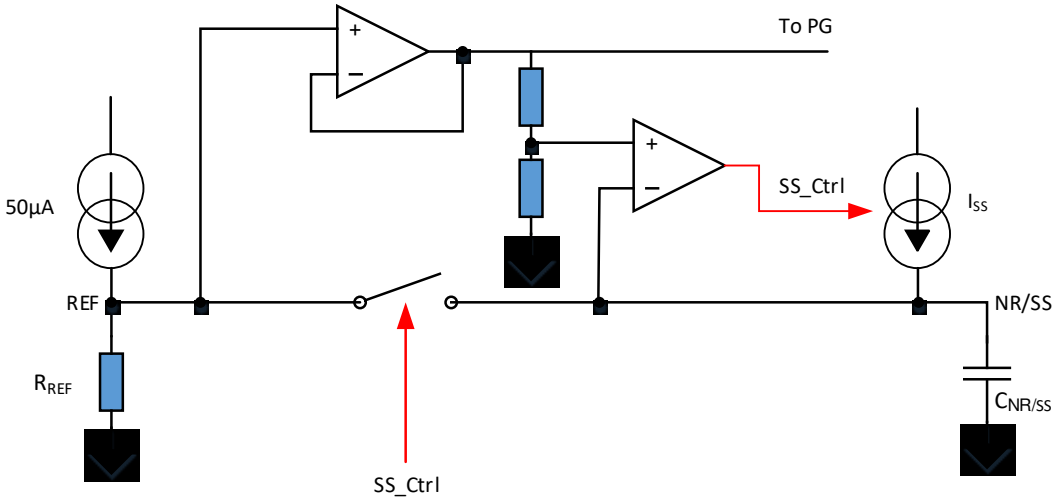

Figure 7-4. Simplified Soft-Start Circuit

The 200µA (typical) $I_{NR/SS}$ current quickly charges $C_{NR/SS}$ until the voltage reaches approximately 97% of the set output voltage. Then the I_{SS} current turns off and the switch between REF and NR/SS closes. Thus leaving only the I_{REF} current to charge $C_{NR/SS}$ to the set output voltage level.

Note

The discharge pulldown resistor on NR/SS (see the *Functional Block Diagram*) is engaged when any ground-referenced UVLOs are tripped, or when any faults occur. Such faults include overtemperature, POR, IREF bad, or OTP error faults. This resistor only engages when one of these events are active and the NRSS pin is above 50mV.

The soft-start ramp time depends on the fast start-up ($I_{NR/SS}$) charging current, the reference current (I_{REF}), $C_{NR/SS}$ capacitor value, and the targeted output voltage ($V_{OUT(target)}$). Equation 3 calculates the soft-start ramp time.

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$$\text{Soft-start time } (t_{SS}) = (V_{OUT(target)} \times C_{NR/SS}) / (I_{SS}) \quad (3)$$

The I_{SS} current is provided in the *Typical Characteristics* section and has a value of 200µA (typical). The I_{REF} current has a value of 50µA (typical). The remaining 3% of the start-up time is determined by the $R_{REF} \times C_{NR/SS}$ time constant. Figure 7-5 shows the PG threshold at start-up.

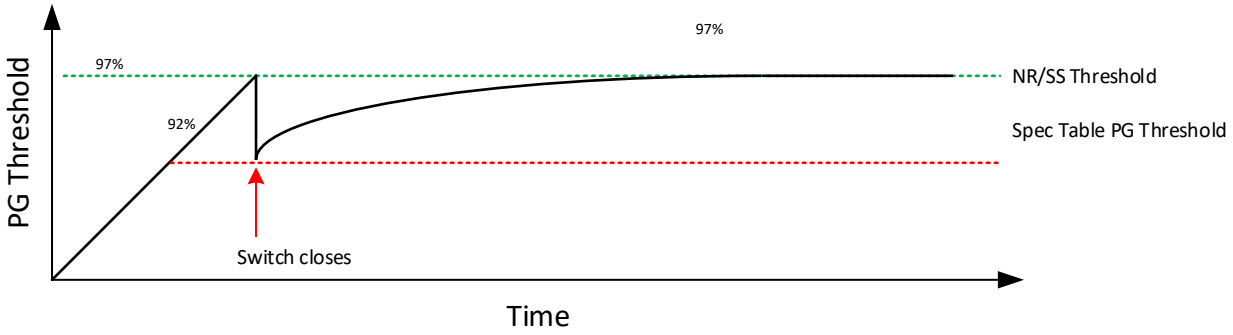


Figure 7-5. PG Threshold During Start-Up

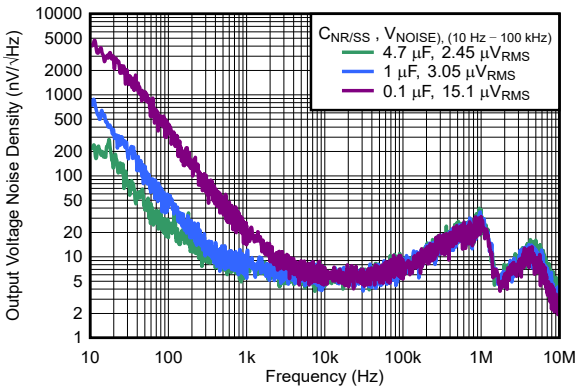
The output voltage noise is lowered significantly by increasing the $C_{NR/SS}$ capacitor. The $C_{NR/SS}$ capacitor and R_{REF} resistor form a LPF that filters out noise from the V_{REF} voltage reference, thereby reducing the device noise floor. The low-pass filter (LPF) is a single-pole filter and Equation 4 calculates the LPF cutoff frequency. Increasing the $C_{NR/SS}$ capacitor significantly lowers output voltage noise, however, doing so lengthens start-up time. For low-noise applications, use a 4.7µF $C_{NR/SS}$ for optimal noise and start-up time trade off.

$$\text{Cutoff Frequency } (f_{cutoff}) = 1 / (2 \times \pi \times R_{REF} \times C_{NR/SS}) \quad (4)$$

Note

Current limit is entered during start up with a small $C_{NR/SS}$ and large C_{OUT} because V_{OUT} no longer tracks the soft-start ramp.

Figure 7-6 shows the impact of the $C_{NR/SS}$ capacitor on the LDO output voltage noise.



C_{IN} = 4.7µF, C_{OUT} = 22µF, V_{CP_EN} = V_{EN}, V_{IN} = 5.3V,
V_{OUT} = 5V, I_{OUT} = 6A

Figure 7-6. Output Voltage Noise Density vs $C_{NR/SS}$ With Charge Pump Enabled

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7.1.7 Optimizing Noise and PSRR

Noise is generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output) that results in degraded power-supply source quality. Noise is easily noticed in audio as a hissing or popping sound. Extrinsic and intrinsic are the two basic groups that noise is categorized into. Noise produced from an external circuit or natural phenomena such as 50Hz to 60Hz power-line noise (spikes), with harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry, such as resistors and transistors. For this device, the two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage (V_{REF}). Another term that sometimes combines with extrinsic noise is PSRR. PSRR refers to the ability of the circuit or device to reject or filter out input supply noise. PSRR is expressed as a ratio of output voltage noise ripple to input voltage noise ripple.

Optimize the device intrinsic noise and PSRR by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range up to the device bandwidth
- C_{OUT} for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, $V_{IN} – V_{OUT}$ (V_{OpHr}), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a less effect

Device noise performance is significantly improved by using a larger $C_{NR/SS}$ capacitor to filter out noise coupling from the input into the device V_{REF} reference. This coupling is especially apparent from low frequencies up to the device bandwidth. The low-pass filter formed by $C_{NR/SS}$ and R_{REF} is designed to target low-frequency noise originating in the input supply. One downside of a larger $C_{NR/SS}$ capacitor is a longer start-up time. The device unity-gain configuration eliminates the noise performance degradation that other LDOs suffer from because of the feedback network. Furthermore, increasing the device load current has little to no effect on the device noise performance.

Further improvement to the device noise at a higher frequency range than the device bandwidth is achieved by using a larger C_{OUT} capacitor. However, a larger C_{OUT} increases inrush current and slows down the device transient response.

These behaviors are described in the *Typical Characteristics* section. Figure 5-6 and Figure 5-8 list the measured 10Hz to 100kHz RMS noise for a 5V device. These curves illustrate a 0.5V output voltage with a 300mV headroom for different $C_{NR/SS}$ and C_{OUT} conditions with a 6A load current. Table 7-2 and Table 7-3 list the typical output noise for these capacitors.

Increasing the operational headroom between V_{IN} and V_{OUT} has little to no effect on improving noise performance. However, this increase does improve PSRR significantly for frequency ranges up to the device bandwidth. Higher headroom also improves transient performance of the device as well. Although C_{OUT} has little to no affect on improving PSRR at low frequency, C_{OUT} improves PSRR for higher frequencies beyond the device bandwidth. A larger C_{OUT} also lengthens start-up time and increases start-up inrush current. A combination of capacitors, such as 470µF || 22µF is more effective because a combination provides lower ESR and ESL.

Table 7-2. Output Noise for $0.5V_{OUT}$ vs C_{OUT}, and Typical Start-Up Time

V_n (μV_{RMS}), 10Hz to 100kHz BW	$C_{NR/SS}$ (µF)	C_{OUT} (µF)	START-UP TIME (ms)
2.19	4.7	22	11.75
2.07	4.7	470	11.75

Table 7-3. Output Noise for $5V_{OUT}$ vs $C_{NR/SS}$, C_{OUT}, and Typical Start-Up Time for V_{CP_EN} = 5.3V

V_n (μV_{RMS}), 10Hz to 100kHz BW	$C_{NR/SS}$ (µF)	C_{OUT} (µF)	START-UP TIME (ms)
15.2	0.1	22	2.5
3.05	1	22	25
2.45	4.7	22	117.5

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7.1.8 Adjustable Operation

As shown in Figure 7-7, the output voltage of the device is able to be set using a single external resistor (R_{REF}).

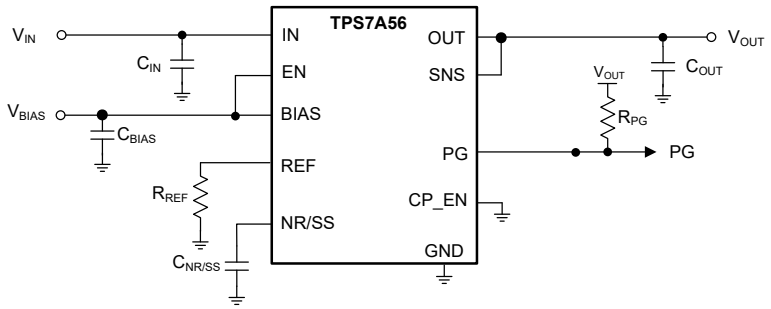

Figure 7-7. Typical Circuit

Use Equation 5 to calculate the R_{REF} value needed for the desirable output voltage.

$$V_{OUT} = I_{REF(NOM)} \times R_{REF} \quad (5)$$

Table 7-4 shows the recommended R_{REF} resistor values to achieve several common rails using a standard 1%-tolerance resistor.

Table 7-4. Recommended R_{REF} Values

TARGETED OUTPUT VOLTAGE (V)	R_{REF} (kΩ)(1)	CALCULATED OUTPUT VOLTAGE (V)
0.5	10.0	0.500
0.6	12.1	0.605
0.7	14.0	0.700
0.8	16.2	0.810
0.9	18.2	0.910
1.0	20.0	1.000
1.2	24.3	1.215
1.5	30.1	1.505
2.5	49.9	2.495
3.0	60.4	3.020
3.3	66.5	3.325
3.6	71.5	3.575
4.7	95.3	4.765
5.0	100.0	5.000

(1) 1% resistors.

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7.1.9 Load Transient Response

The load-step transient response is the LDO output voltage response to load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response. These are the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in Figure 7-8 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

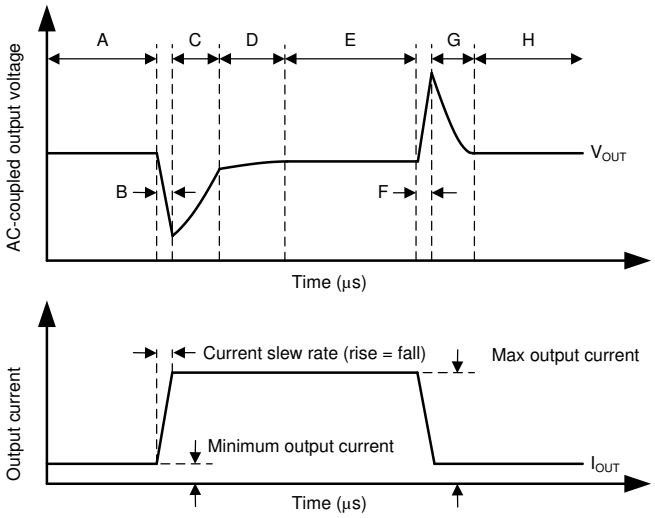

Figure 7-8. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks. This condition occurs because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

Note

The TPS7A56, with such high bandwidth, potentially reacts faster than the output capacitors. Make sure that there is sufficient capacitance at the input of the LDO.

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7.1.10 Charge Pump Operation

As discussed in the *Charge Pump Enable and BIAS Rail* section, the internal charge pump is enabled or disabled using the CP_EN pin. Thus, allowing for operation as low as 1.1V without a BIAS rail.

The CP_EN pin voltage threshold and hysteresis are defined in the *Electrical Characteristics* table.

Depending on the circuit implementation, the internal charge pump is powered from either the IN or the BIAS rails. This pin is not designed to be digitally controlled with a digital I/O pin. Instead, this pin is intended to be tied on the printed circuit board (PCB) to an analog rail.

Although not intended to be controlled dynamically, the CP_EN pin is controlled with a low impedance source. Make sure to provide adequate sequencing between EN and CP_EN because the CP_EN pin is latched when the EN pin is turned on. Only an EN reset or a power cycle clears and resets the CP_EN latch.

Figure 7-9 shows the switching frequency of the charge pump at no-load and full load.

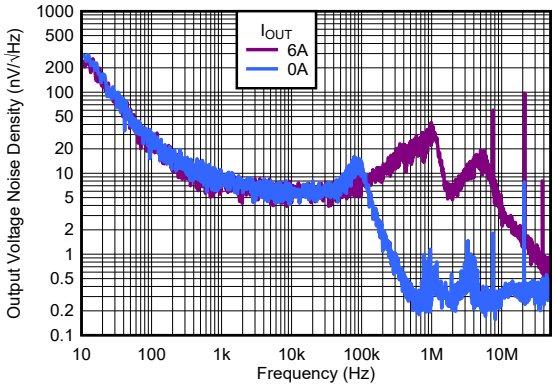

Figure 7-9. Charge Pump Noise

7.1.11 Sequencing

There is no sequencing requirement between IN, BIAS, and EN. CP_EN is an analog signal and is required to be connected to either IN, BIAS, or GND.

A false PG is triggered during shutdown if the BIAS rail is faster than the IN rail takes to discharge. This same scenario occurs with devices having an internal MUX and charge pump.

When the bias rail decreases below $V_{UVLO(BIAS)}$, the internal MUX between IN and BIAS switches over. This condition causes the LDO to be fully powered from the IN rail.

When the BIAS rail goes below UVLO(BIAS) with the IN rail greater than 1.1V and the charge pump enabled, the LDO restarts. The LDO restarts because IN is still a valid condition for operations.

7.1.12 Power-Good Functionality

As described in the *Functional Block Diagram*, the PG pin is a open-drain MOSFET driven by a Schmitt trigger. The Schmitt trigger compares the SNS pin voltage to a preselected voltage equal to 90% that of the reference voltage.

As mentioned in the *Recommended Operating Conditions* table, make sure the pullup resistance is between 10kΩ and 100kΩ for best performance. If PG functionality is not desired, either leave the PG pin floating or connected to GND.

There are two UVLO circuits present on the BIAS rail, one referenced to GND ($V_{UVLO(BIAS)}$) and one referenced to V_{REF} ($V_{UVLO(BIAS)} – V_{REF}$). A false PG event occurs as a result of logic priorities when the charge pump is disabled.

To eliminate any false PG events, consider setting V_{BIAS} 3.2V above V_{OUT}.

Table 7-5 describes the various UVLO behaviors.

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Table 7-5. UVLO Triggered PG Events

V_{IN}	$V_{UVLO(BIAS)}$ RISING	$V_{UVLO(BIAS)}$ FALLING	$V_{UVLO(BIAS)} – V_{REF}$ RISING	$V_{UVLO(BIAS)} – V_{REF}$ FALLING
0.5V	2.8V	2.685V	2.1 + 0.5 = 2.6V	1.86 + 0.5 = 2.36V
0.7V	2.8V	2.685V	2.1 + 0.7 = 2.8V	1.86 + 0.7 = 2.56V
1.4V	2.8V	2.685V	2.1 + 1.4 = 3.5V	1.86 + 1.4 = 3.26V
5.2V	2.8V	2.685V	2.1 + 5.2 = 7.3V	1.86 + 5.2 = 7.06V

7.1.13 Paralleling for Higher Output Current and Lower Noise

Achieving higher output current and lower noise is achievable by paralleling two or more LDOs. Carefully plan out implementation to optimize performance and minimize output current imbalance.

Because the TPS7A56 output voltage is set by a resistor driven by a current source, adjust the REF resistor and capacitor. The following equations calculate the resistor and capacitor settings.

$$R_{REF} = V_{OUT_TARGET} / (n \times I_{REF}) \quad (6)$$

$$C_{NR/SS_parallel} = n \times C_{NR/SS_single} \quad (7)$$

where:

- n is the number of LDOs in parallel
- I_{REF} is the REF current as provided in the *Electrical Characteristics* table
- $C_{NR/SS_}$single is the NR/SS capacitor for a single LDO; make sure each LDO has a separate $C_{NR/SS}$ capacitor

The LDO functions as a buffer when connecting the IN pins together. Thus, the current imbalance is only affected by the error offset voltage of the error amplifier. As such, express the current imbalance as:

$$\varepsilon_I = V_{OS} \times 2 \times R_{BALLAST} / (R_{BALLAST}^{\ 2} – \Delta R_{BALLAST}^{\ 2}) \quad (8)$$

where:

- ε_I is the current imbalance
- V_{OS} is the LDO error offset voltage
- $R_{BALLAST}$ is the ballast resistor
- $\Delta R_{BALLAST}$ is the deviation of the ballast resistor value from the nominal value

Figure 7-10 shows a diagram of multiple devices in parallel.

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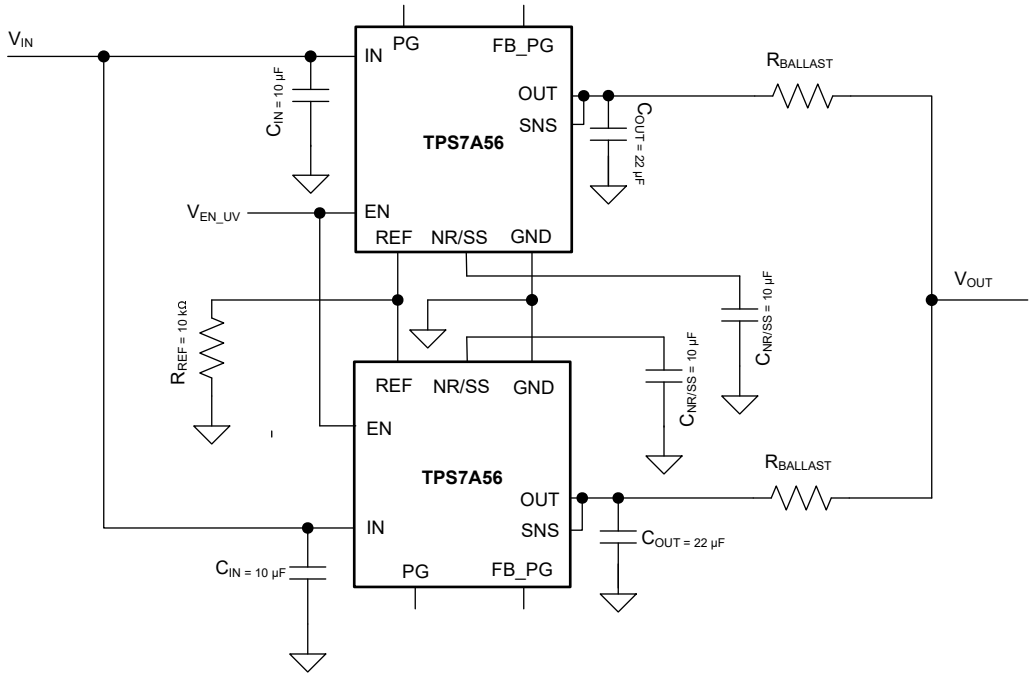

Figure 7-10. Paralleling Multiple TPS7A56 Devices

Using the configuration described, the LDO output noise is reduced by:

$$e_{O_parallel} = (1 / \sqrt{n}) \times e_{O_single} \quad (9)$$

where:

- n is the numbers of LDOs in parallel
- e_{O_single} is the output noise density from a single LDO
- $e_{O_parallel}$ is the output noise density for the resulting parallel LDO

In Figure 7-10, the noise is reduced by $1/\sqrt{2}$.

For more information in paralleling LDOs see:

- *Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors* technical white paper
- *A Scaleable, High-Current, Low-Noise Parallel LDO Reference Design* design guide
- *Parallel LDO Architecture Design Using Ballast Resistors* technical white paper

7.1.14 Power Dissipation (P_D)

Circuit reliability requires proper consideration pf the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (10)$$

Note

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

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The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation through the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A = (R_{\theta JA} \times P_D) \tag{11}$$

The following equation rearranges this relationship for output current.

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{12}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area. $R_{\theta JA}$ is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the RTE package $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the junction-to-case (bottom) thermal resistance, as given in the *Thermal Information* table.

7.1.15 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the LDO junction temperatures when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 13 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \tag{13}$$

where:

- P_D is the power dissipated as explained in Equation 10
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

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7.1.16 TPS7A57EVM-056 Thermal Analysis

The TPS7A57EVM-056 was used to develop the TPS7A5601RTE thermal model. The RTE package is a 3mm × 3mm, 16-pin WQFN with 25µm plating on each via. The EVM is a 3.5 inch × 3.5 inch (89mm × 89mm) PCB comprised of six layers. Table 7-6 lists the layer stackup for the EVM. Figure 7-11 to Figure 7-18 illustrate the various layer details for the EVM.

Table 7-6. TPS7A57EVM-056 PCB Stackup

LAYER	NAME	MATERIAL	THICKNESS (mil)
1	Top overlay	—	—
2	Top solder	Solder resist	0.4
3	Top layer	Copper	2.756
4	Dielectric 1	FR-4 high Tg	9
5	Mid layer 1	Copper	2.756
6	Dielectric 2	FR-4 high Tg	9
7	Mid layer 2	Copper	2.756
8	Dielectric 3	FR-4 high Tg	9
9	Mid layer 3	Copper	2.756
10	Dielectric 4	FR-4 high Tg	9
11	Mid Layer 4	Copper	2.756
12	Dielectric 5	FR-4 high Tg	9
13	Bottom layer	Copper	2.756
14	Bottom solder	Solder resist	0.4

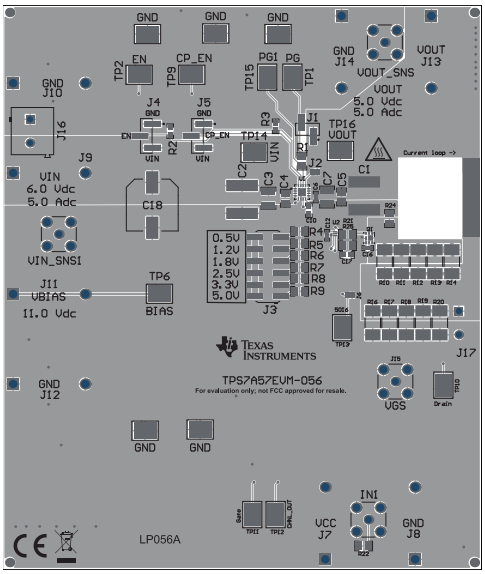

Figure 7-11. Top Assembly Layer and Silkscreen

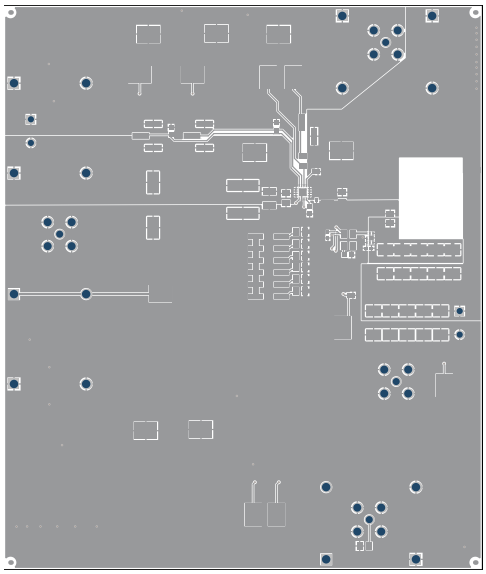

Figure 7-12. Top Layer Routing

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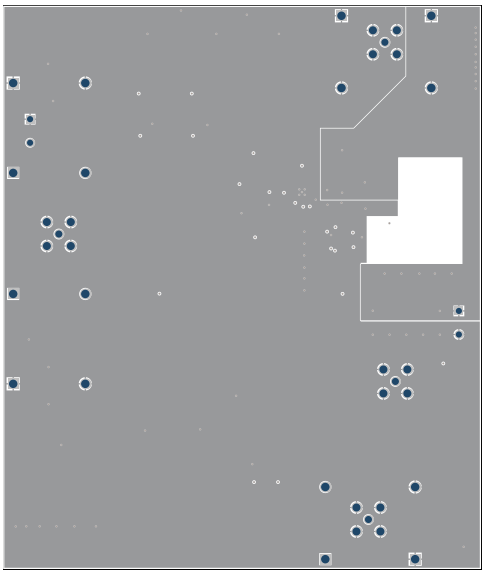

Figure 7-13. Layer 2 Routing



Figure 7-14. Layer 3 Routing

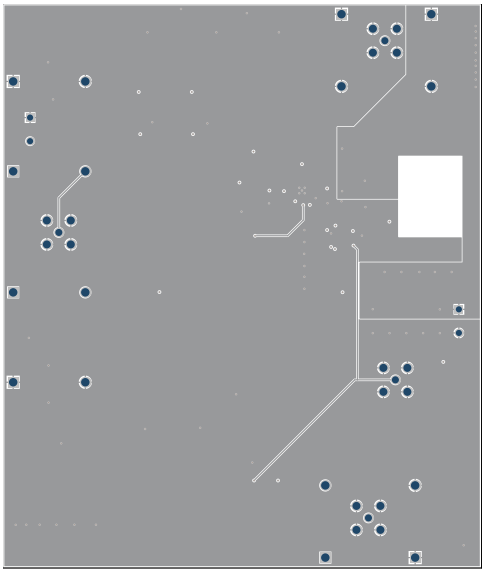

Figure 7-15. Layer 4 Routing



Figure 7-16. Layer 5 Routing

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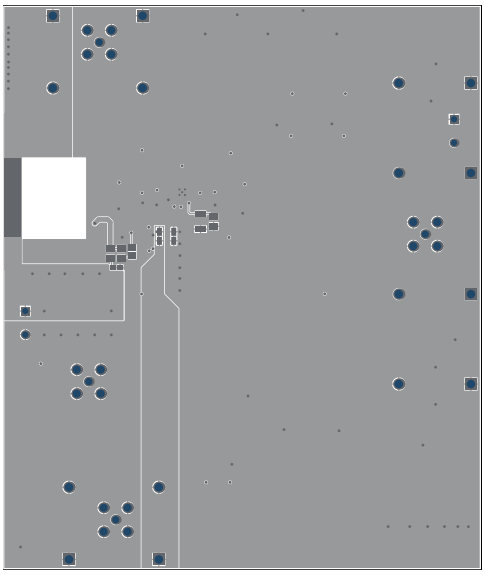

Figure 7-17. Bottom Layer Routing

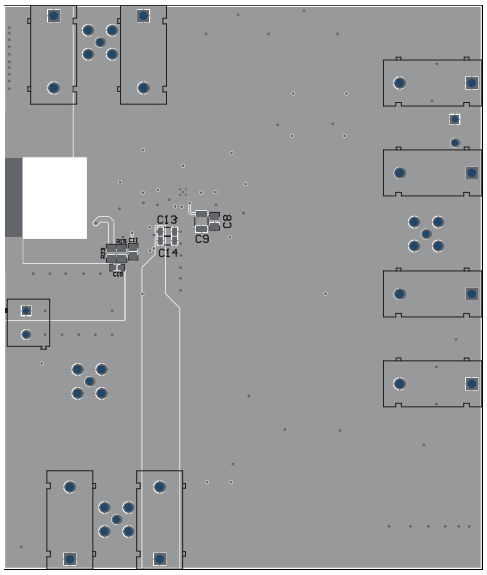

Figure 7-18. Bottom Assembly Layer and Silkscreen

Table 7-7 shows thermal simulation data for the TPS7A57EVM-056. Figure 7-19 and Figure 7-20 show the thermal gradient on the PCB and device. This thermal radiant results when using a 1W power dissipation through the pass transistor with a 25°C ambient temperature.

Table 7-7. TPS7A57EVM-081 Thermal Simulation Data

DUT	$R_{\theta JA}$(°C/W)	Ψ_{JB}(°C/W)	Ψ_{JT}(°C/W)
TPS7A57EVM-056	21.9	11.9	0.4

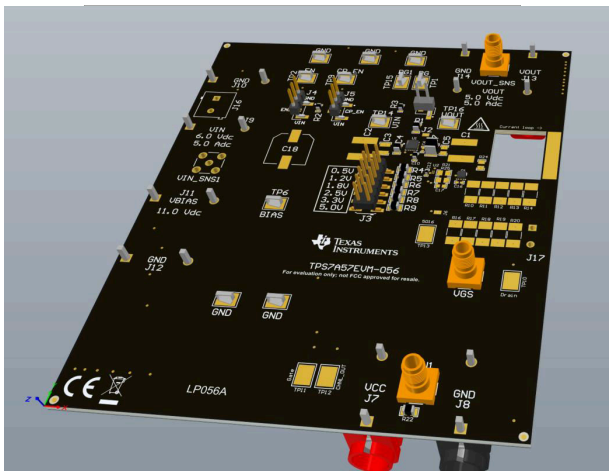

Figure 7-19. TPS7A57EVM-081 3D View

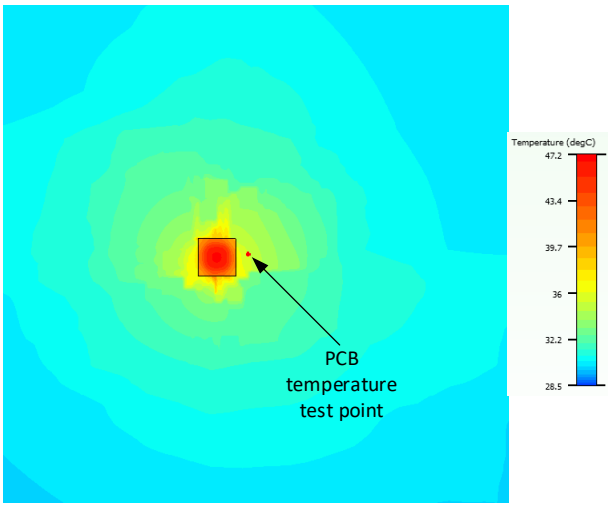

Figure 7-20. TPS7A57EVM-081 PCB Thermal Gradient

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7.2 Typical Application

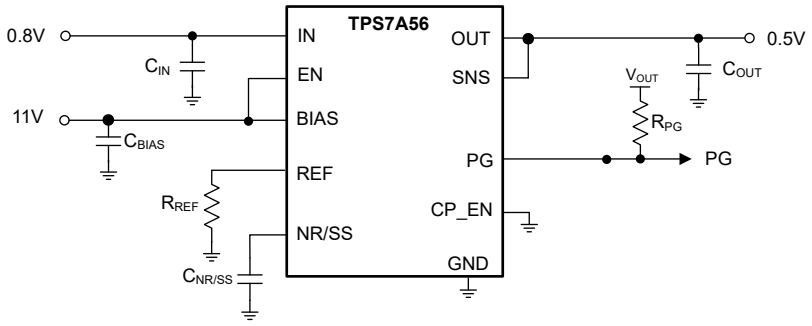

Figure 7-21. Typical Application Schematic

7.2.1 Design Requirements

Table 7-8 lists the required application parameters for this design example.

Table 7-8. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	0.8V, ±3%, provided by the dc/dc converter switching at 1MHz
Bias voltage	11V
Output voltage	0.5V, 1%
Charge pump	Disabled
Output current	4.2A (maximum), 3.5A (minimum)
Noise	Less than 5μV_{RMS}
PSRR at 10kHz	80dB at max load current
PSRR at 1MHz	> 35dB at max load current
Maximum load transient	±5mV, 100mA to 3.5A
Start-up environment	Start-up time < 15ms

7.2.2 Detailed Design Procedure

In this design example, the device is powered by a dc/dc convertor switching at 1MHz. The load requires a 0.5V clean rail with less than 5μV_{RMS}. Use typical 22μF input and output capacitors and 4.7μF NR/SS capacitors. These capacitors achieve a good balance between fast start-up time and excellent noise, and PSRR performance and load transient.

The output voltage is set using a 10kΩ, thin-film resistor value calculated as described in the *Output Voltage Setting and Regulation* section. The PG pin is not used and is thus connected to ground to help with thermals. The enable voltage is provided by a external I/O. Figure 7-23 illustrates that the device meets all design noise requirements. Figure 7-22 depicts adequate PSRR performance.

As illustrated in Figure 7-24, the load transient is adequate to the power-supply requirement.

Figure 7-21 depicts the implementation of these components.

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7.2.3 Application Curves

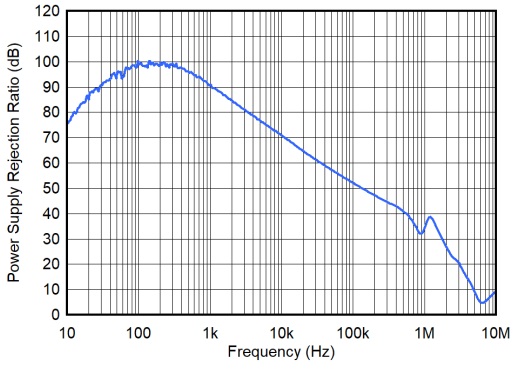

Figure 7-22. PSRR vs Frequency

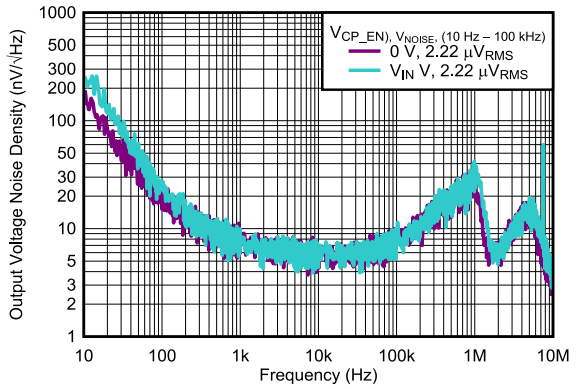

Figure 7-23. Noise vs Frequency

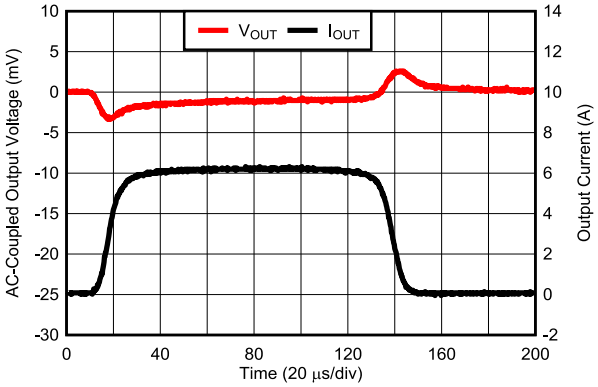

Figure 7-24. Load Transient

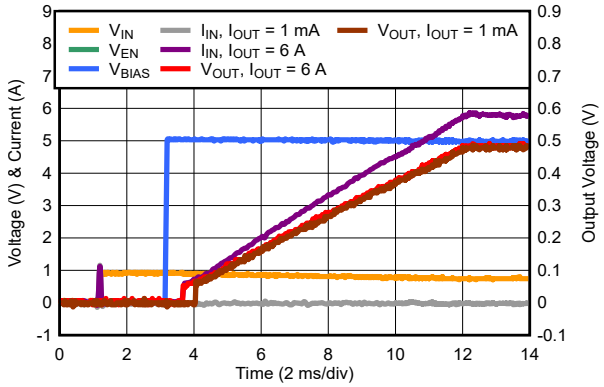

Figure 7-25. Start-Up Rail Sequence

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging from 0.7V to 6.0V and a BIAS rail up to 11V. Make sure the input voltage range provides adequate operational headroom for the device to have a regulated output. Make sure this input supply is well regulated and low impedance. If the input supply is noisy, use additional input capacitors with low ESR. Increase the operating headroom to achieve the desired output noise, PSRR, and load transient performance.

There is no sequencing requirement between IN, BIAS, and EN. CP_EN is an analog signal and is required to be connected to either IN, BIAS, or GND.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board. Place these components as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible. Use wide, component-side, copper surface for these connections. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in Figure 7-26 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

Because of the wide bandwidth and high output current capability, inductance present on the output negatively impacts load transient response. For best performance, minimize trace inductance between the output and load. A low ESL capacitor combined with low trace inductance limits the total inductance present on the output and optimizes the high-frequency PSRR.

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To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage and shields noise. This plane behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Example

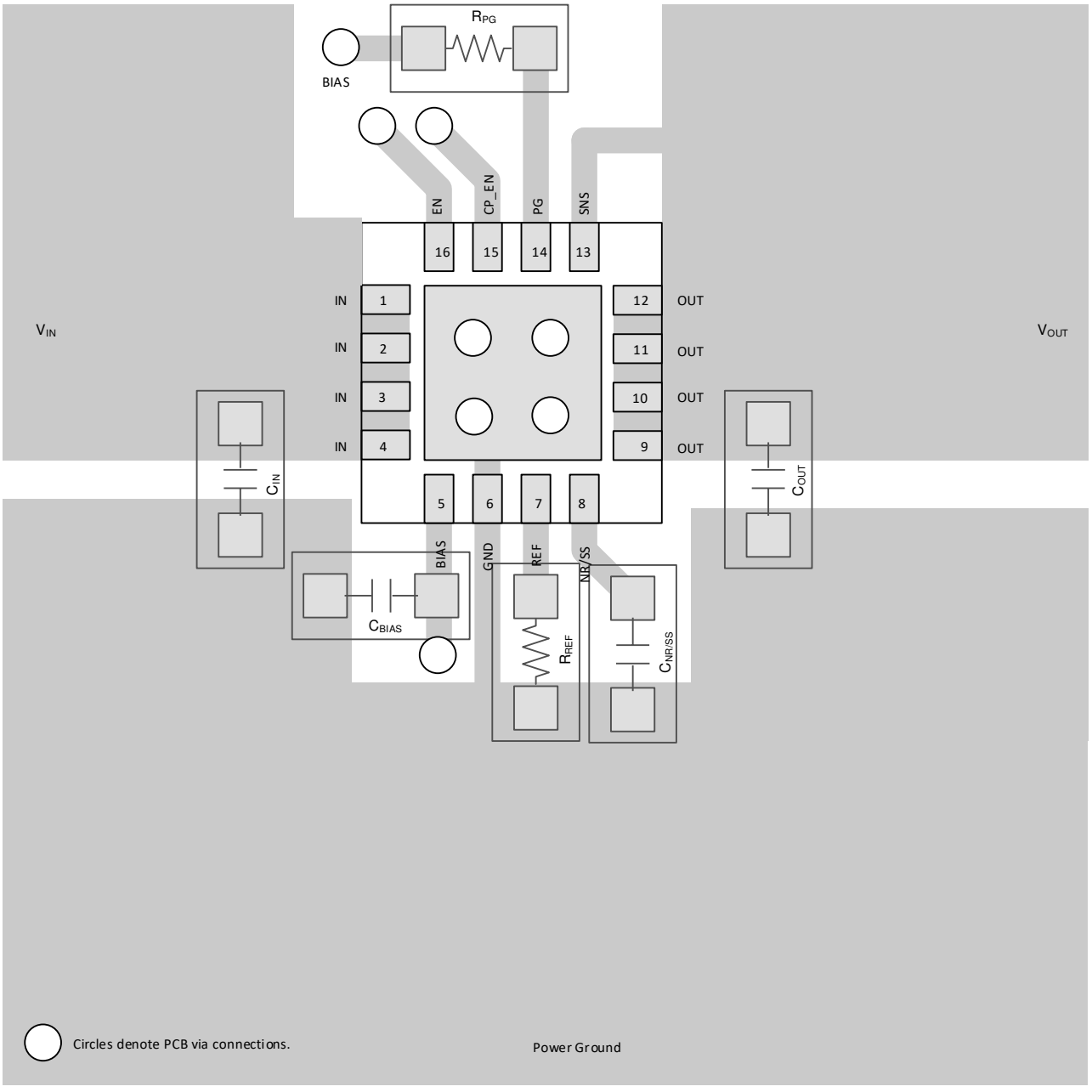

Figure 7-26. Recommended Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

Use the TPS7A57EVM-056 to install and evaluate the TPS7A56. This evaluation module (EVM) is available to assist in the initial circuit performance evaluation. Request or purchase the TPS7A56 (and related user guide TPS7A57EVM-056) at the Texas Instruments website through the product folders or directly from the TI eStore.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TPS7A56**01yyyz**	**01** indicates that this device is offered as an adjustable option. **yyy** is the package designator. **z** is the package quantity. R is for large reel.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7A57EVM-056 Evaluation Module* user guide
- Texas Instruments, *High-Current, Low-Noise Parallel LDO Reference Design* design guide
- Texas Instruments, *Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors* technical white paper
- Texas Instruments, *A Scaleable, High-Current, Low-Noise Parallel LDO Reference Design* design guide
- Texas Instruments, *Parallel LDO Architecture Design Using Ballast Resistors* technical white paper

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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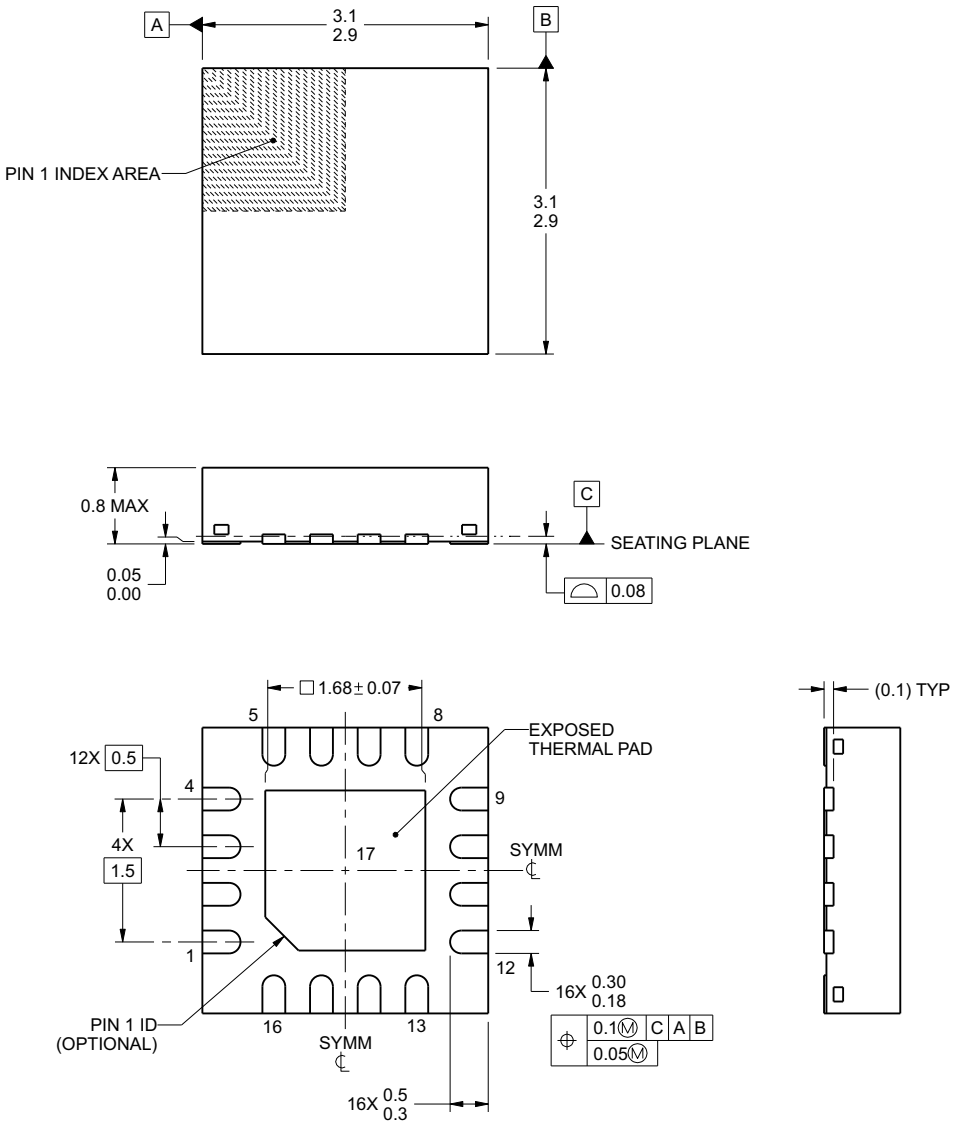
10.1 Mechanical Data

RTE0016C

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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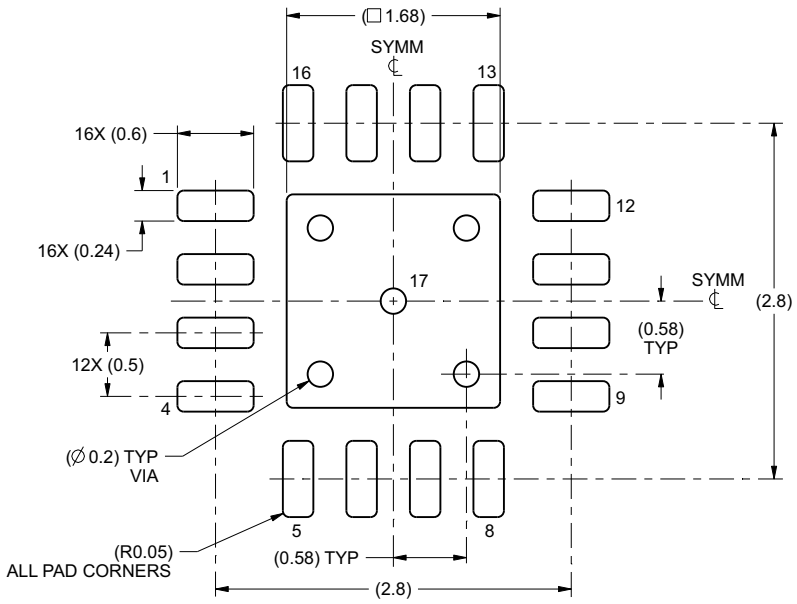
EXAMPLE BOARD LAYOUT

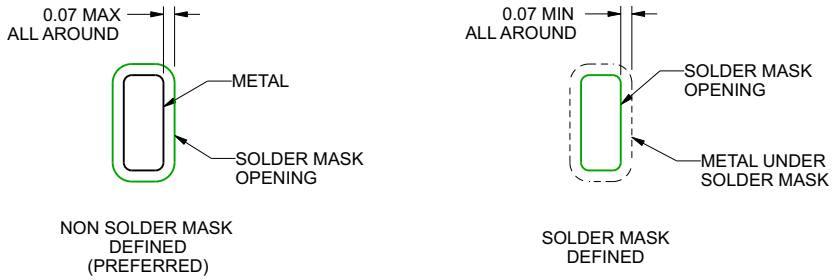
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219117/A 09/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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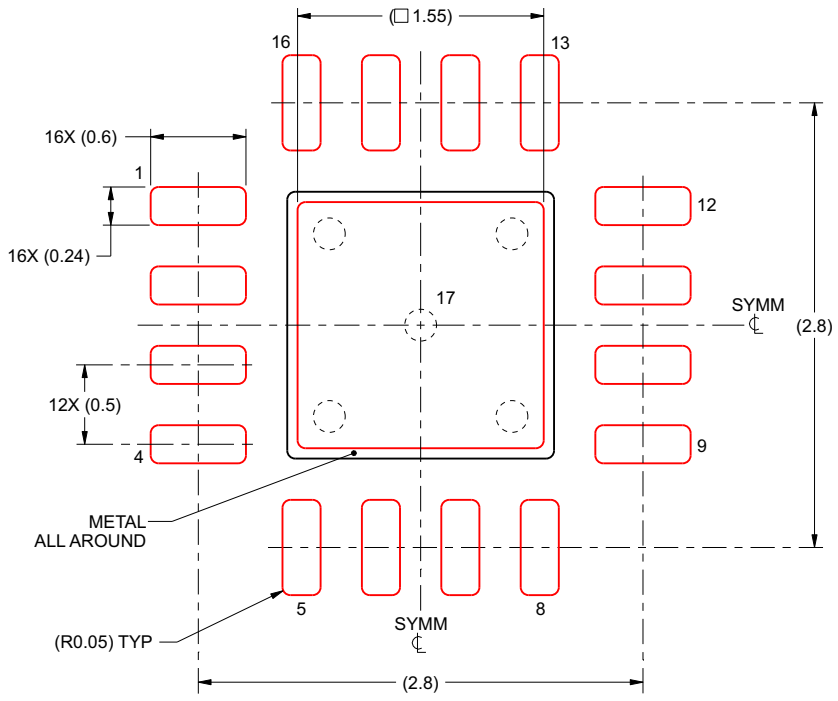
EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A5601RTER	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A5601
TPS7A5601RTER.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A5601

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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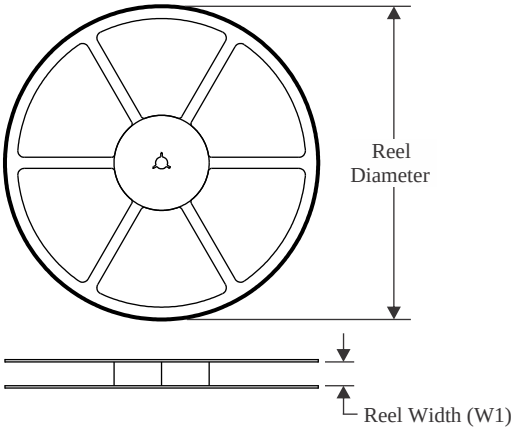
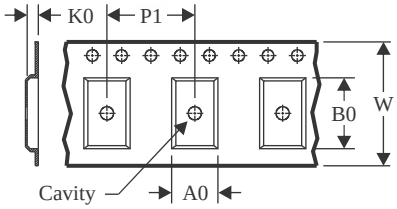
TAPE AND REEL INFORMATION

REEL DIMENSIONS

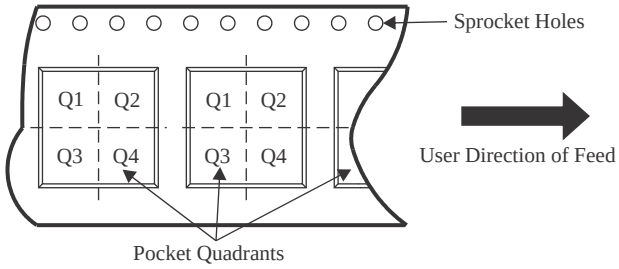


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

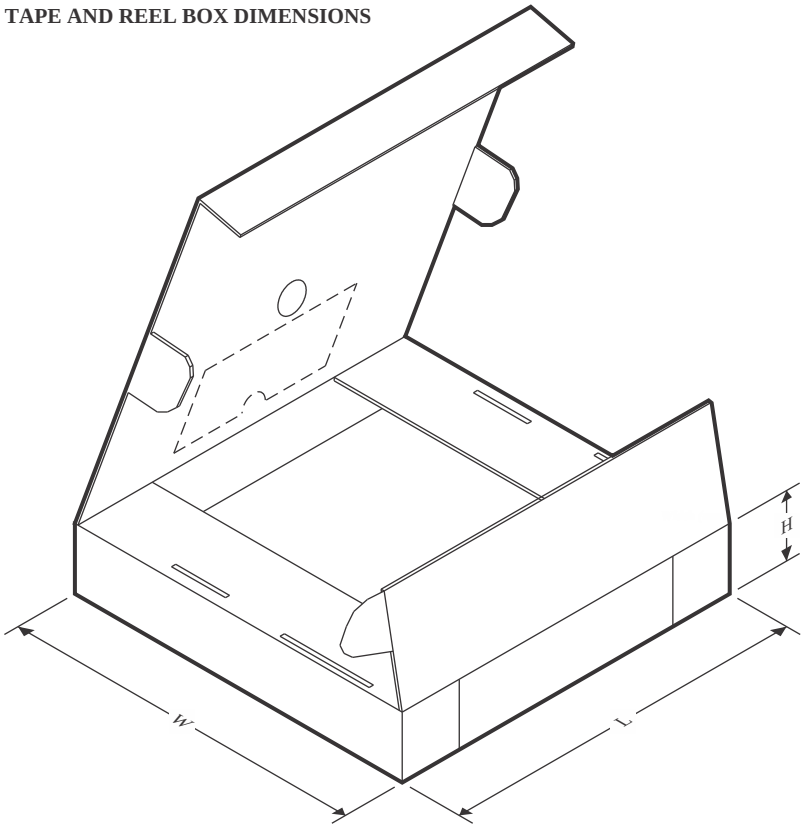
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A5601RTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A5601RTER	WQFN	RTE	16	5000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

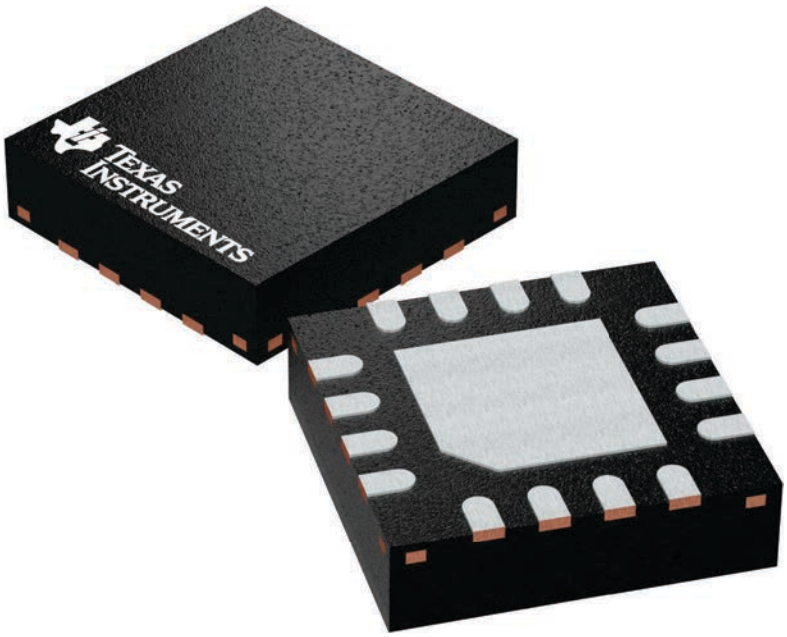
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

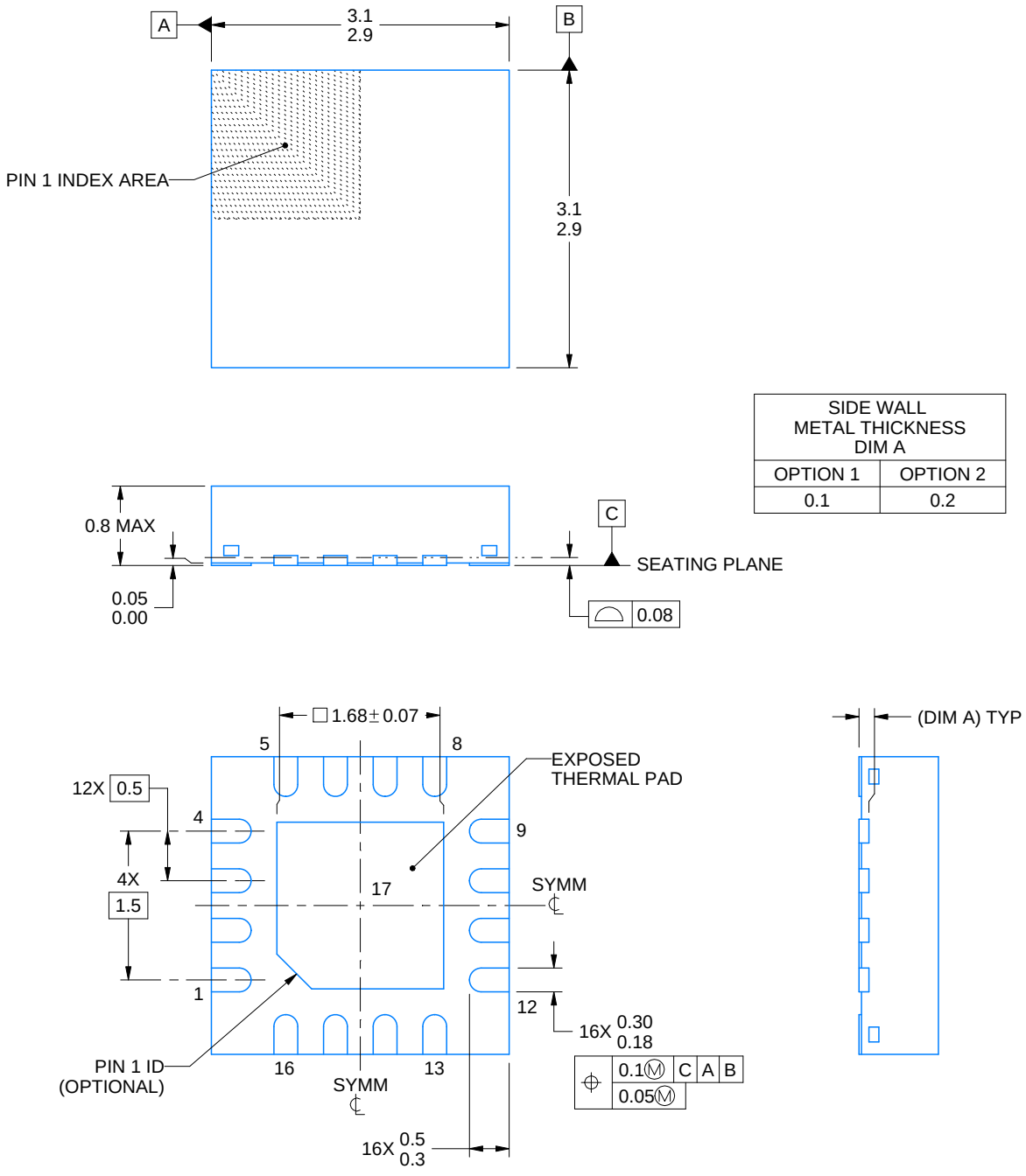


RTE0016C

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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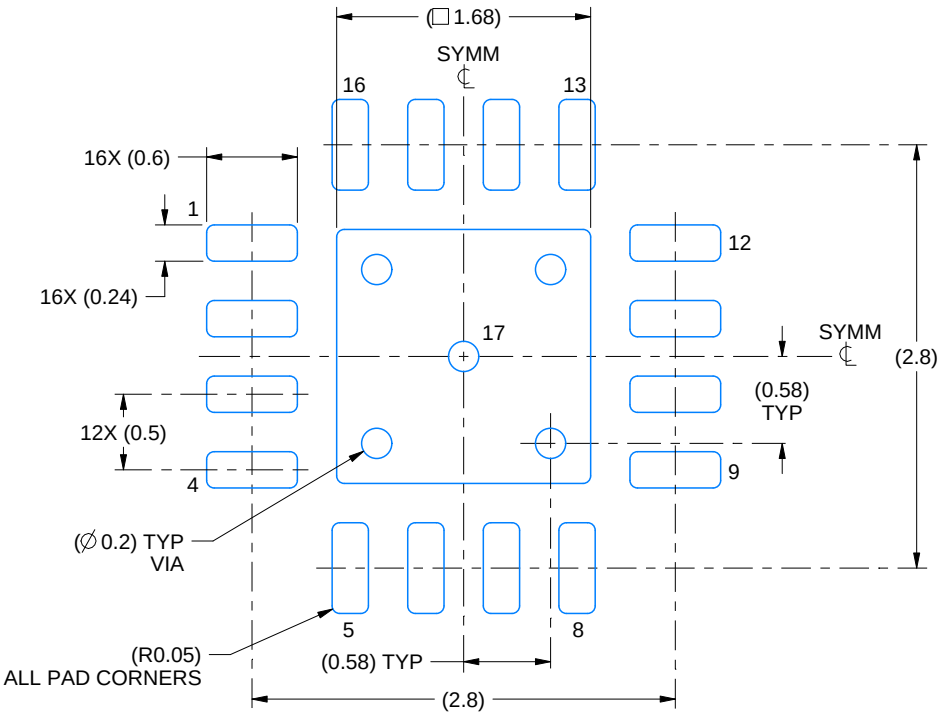
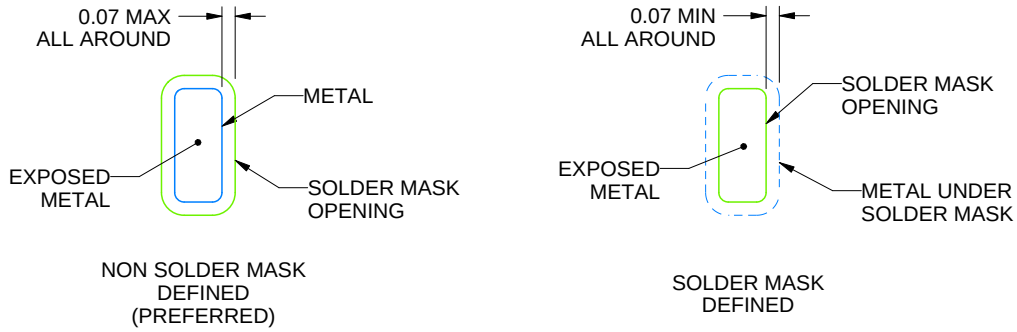


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

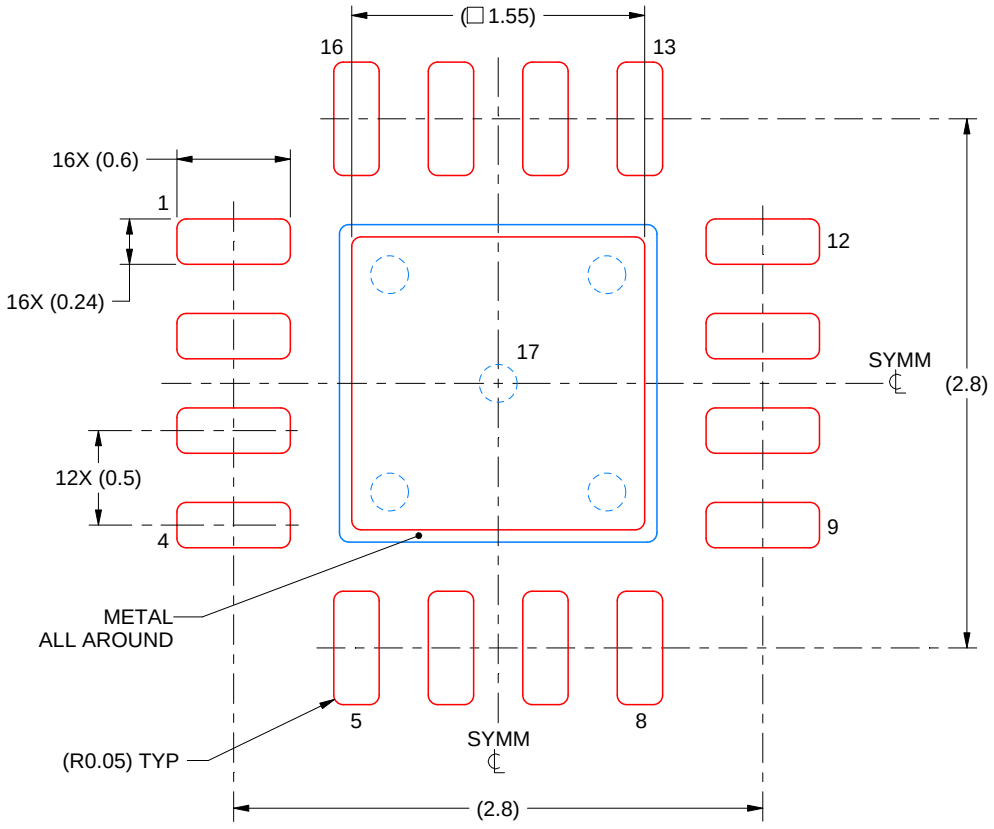


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025

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