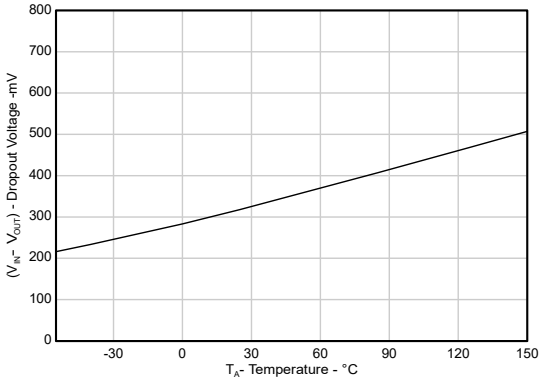
# TPS7C84-Q1 Automotive, 150mA, 40V, Adjustable, Low-Dropout Regulator With Power-Good

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: −40°C to +125°C, $T_A$
  - Junction temperature: −40°C to +150°C, $T_J$
- Wide input voltage range:
  - $V_{IN}$ range: 2.1V to 40V
- Wide output voltage range ($V_{OUT}$):
  - Fixed option: 3.3V, 5.0V
  - Adjustable option: 1.2V to 39V
- Output current: up to 150mA
- $V_{OUT}$ accuracy:
  - ±1% over line, load, and temperature
- Quiescent current ($I_Q$): 45µA (typical)
- Low dropout: 350mV (typical)
- Open-drain, power-good output
- Output current limiting and thermal shutdown
- Stable over a wide range of ceramic output capacitor values:
  - $C_{OUT}$ range: 1µF to 100µF
  - ESR range: 0Ω to 2Ω
- Package options:
  - D (8-pin SOIC)
  - DRB (8-pin VSON)

## 2 Applications

- Traction inverters
- Body control modules (BCM)
- Onboard chargers
- Telematics controls




**Dropout Voltage vs Temperature ($V_{IN}$ = 4.9V, $I_{OUT}$ = 150mA)**

## 3 Description

The TPS7C84-Q1 is a wide input, low-dropout regulator (LDO) supporting from 2.1V to 40V input voltage range and up to 150mA of load current. The TPS7C84-Q1 has both fixed and adjustable output types. Fixed output options include 3.3V and 5V. The output is able to be set between from 1.2V and 39V with the adjustable device.

This device has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output sequence multiple power supplies in the system.

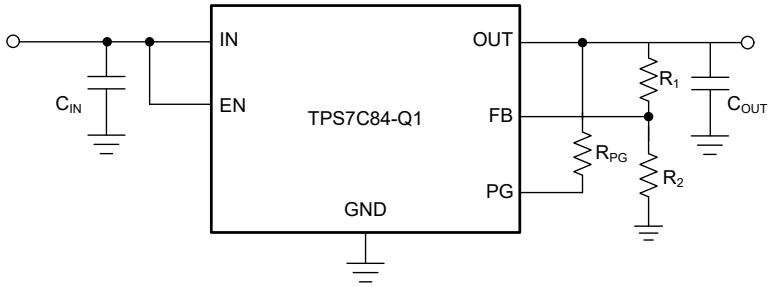
The TPS7C84-Q1 is designed for up to 40V $V_{IN}$ battery-connected applications. The wide output voltage range allows the device to generate the bias voltage for silicon carbide (SiC) gate drivers and microphones, as well as power MCUs and processors.

The device is available in both an SOIC package and a small VSON package with wettable flanks that facilitates a compact printed circuit board (PCB) design. The low thermal resistance enables sustained operation despite significant dissipation across the device.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS7C84-Q1 | D (SOIC, 8) | 4.9mm × 6mm |
| | DRB (VSON, 8) | 3mm × 3mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Circuit**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Pin Configuration and Functions**....3
**5 Specifications**....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....5
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Timing Requirements....6
5.7 Typical Characteristics....7
**6 Detailed Description**....12
6.1 Overview....12
6.2 Functional Block Diagrams....12
6.3 Feature Description....13
6.4 Device Functional Modes....14
**7 Application and Implementation**....15
7.1 Application Information....15
7.2 Typical Application....17
7.3 Power Supply Recommendations....20
7.4 Layout....20
**8 Device and Documentation Support**....21
8.1 Device Support....21
8.2 Documentation Support....21
8.3 Receiving Notification of Documentation Updates....21
8.4 Support Resources....21
8.5 Trademarks....21
8.6 Electrostatic Discharge Caution....21
8.7 Glossary....21
**9 Revision History**....21
**10 Mechanical, Packaging, and Orderable Information**....22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# 4 Pin Configuration and Functions

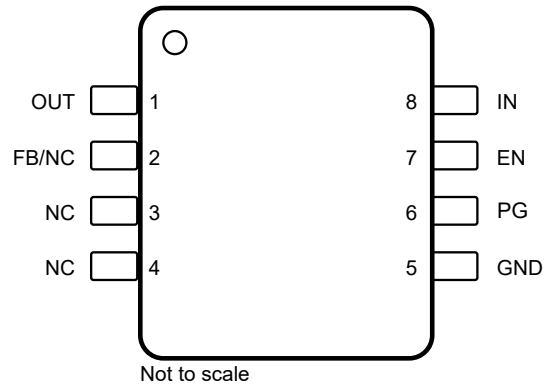


**Figure 4-1. D Package, 8-Pin SOIC (Top View)**

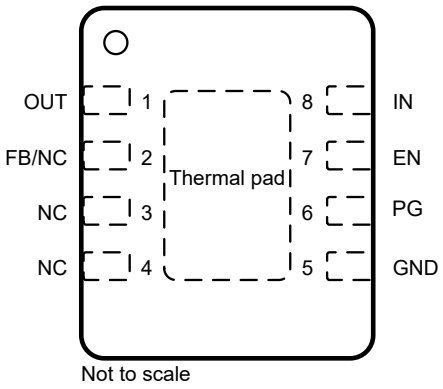


**Figure 4-2. DRB Package, 8-Pin VSON (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 7 | I | Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level ($V_{IL}$). To make sure the device is enabled, drive the EN pin above the logic high level ($V_{IH}$). Do not leave this pin floating because this pin is high impedance. If this pin is left floating, the pin state becomes undefined and the device potentially enables or disables. |
| FB/NC | 2 | I | This pin is a feedback pin when using an external resistor divider or an NC pin when using the device with a fixed output voltage. When using the adjustable device, connect this pin through a resistor divider to the output for the device to function. See the *Feedback Resistor Selection* section for more information. If using a fixed output, leave this pin floating or connected to GND. |
| GND | 5 | — | Ground |
| IN | 8 | I | Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section. Place the input capacitor as close to the input of the device as possible. |
| NC | 3, 4 | — | No internal connection. Leave this pin floating or tied to GND for best thermal performance. |
| OUT | 1 | O | Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND. Place the output capacitor as close to the device output as possible. See the *Input and Output Capacitor Requirements* section for more details. |
| PG | 6 | O | Active-high, open-drain power-good output. This pin goes low when $V_{OUT}$ drops by 6% of the nominal value. |

(1) I = input; O = output.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| IN | Continuous input voltage | –0.3 | 42 | V |
| OUT | Output voltage | –0.3 | VIN+0.3(3) | V |
| EN | EN input voltage | –0.3 | 42 | V |
| PG | PG comparator output voltage(2) | –0.3 | 42 | V |
| FB | FEEDBACK input voltage | –0.3 | 5 | V |
| $T_J$ | Operating junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) Can exceed input supply voltage.
(3) The absolute maximum rating is VIN + 0.3V or 42V, whichever is smaller.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2500 | V |
| | | Charged-device model (CDM), per AEC V Q100-011 | All pins | ±1000 | |
| | | | Corner pins | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.


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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.1 | | 40 | V |
| $V_{EN}$ | Enable voltage | 0 | | 40 | V |
| $V_{OUT}$ | Output voltage | 1.2 | | 39 | V |
| $I_{OUT}$ | Output current | 0 | | 150 | mA |
| $C_{OUT}$ | Output capacitor(1) | 1 | 2.2 | 100 | µF |
| $C_{OUT}$ ESR | Output capacitor ESR | 0 | | 2 | Ω |
| $C_{IN}$ | Input capacitor | | 1 | | µF |
| $C_{FF}$ | Feed-forward capacitor (optional(2), for adjustable device only) | | 10 | | pF |
| $I_{FB_DIVIDER}$ | Feedback divider current(2) (adjustable device only) | 12 | | | µA |
| $T_J$ | Junction temperature | –40 | | 150 | °C |

(1) Effective output capacitance of 0.5µF minimum required for stability.
(2) $C_{FF}$ required for stability if the feedback divider current < 12µA. Feedback divider current = $V_{OUT}$ / ($R_1$ + $R_2$). See the *Feed-Forward Capacitor ($C_{FF}$)* section for details.

## 5.4 Thermal Information

| THERMAL METRIC(1) (2) | | DRB | D | UNIT |
|---|---|---|---|---|
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 50.2 | 123 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 68.6 | 67.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 24.1 | 70.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 5.5 | 18.0 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 24.2 | 69.8 | °C/W |

(1) The thermal data is based on the JEDEC standard high K profile,JESD 51-7. Two-signal, two-plane, four-layer board with 2oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

specified at TJ = –40°C to +150°C, at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, $V_{EN}$ ≥ 2V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output voltage accuracy | $V_{IN}$ = [$V_{OUT(NOM)}$ + 1V] to 40V, $I_{OUT}$ = 100µA to 150mA | $T_J$ = 25°C | –0.5 | | 0.5 | % |
| | | | $T_J$ = –40°C to 150°C | –1 | | 1 | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation | $V_{IN}$ = [$V_{OUT(NOM)}$ + 1V] to 40V | $T_J$ = –40°C to 150°C | | 0.0004 | 0.01 | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | $I_{OUT}$ = 100 µA to 150mA | $T_J$ = –40°C to 150°C | | 0.02 | 0.2 | % |
| $V_{FB}$ | Feedback voltage | Reference voltage for FB | $T_J$ = –40°C to 150°C | 1.188 | 1.2 | 1.212 | V |
| $I_{FB}$ | FEEDBACK bias current | | $T_J$ = 25°C | | 2 | 10 | nA |
| | | | $T_J$ = –40°C to 150°C | | | 15 | |
| $V_{DO}$ | Dropout voltage adjustable output | $V_{IN}$ = 3.5V, $I_{OUT}$ = 150mA | $T_J$ = –40°C to 150°C | | 350 | 660 | mV |
| | Dropout voltage fixed 3.3V output | $V_{IN}$= $V_{OUT}$ (nominal)= 3.3V, $I_{OUT}$ = 150mA | | | | 670 | |
| | Dropout voltage fixed 5V output | $V_{IN}$= $V_{OUT}$ (nominal)= 5V, $I_{OUT}$ = 150mA | | | | 580 | |

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specified at TJ = –40°C to +150°C, at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, $V_{EN}$ ≥ 2V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent current | $I_{OUT}$ = 0 | $T_J$ = –40°C to 150°C | | | 56 | µA |
| | | $I_{OUT}$ = 100µA | | | 45 | 68 | |
| | | $I_{OUT}$ = 150mA | | | | 1.15 | mA |
| UVLO | UVLO $V_{IN}$ rising | $I_{OUT}$ = 100µA | $T_J$ = –40°C to 150°C | 1.8 | 1.9 | 2.0 | V |
| | UVLO $V_{IN}$ falling | | | 1.7 | 1.8 | 1.9 | |
| | Hysteresis | | | | 100 | | mV |
| $V_{IL}$ | Enable logic input low level | Low (regulator OFF) | $T_J$ = –40°C to 150°C | | | 0.7 | V |
| $V_{IH}$ | Enable logic input high level | High (regulator ON) | | 1.9 | | | |
| $I_{EN}$ | EN pin current | $V_{EN}$ = 40V | $T_J$ = –40°C to 150°C | | | 0.8 | µA |
| $I_{CL}$ | Current limit | $V_{IN}$ ≥ 3V, $V_{OUT}$ = 0V | $T_J$ = –40°C to 150°C | 165 | 235 | 280 | mA |
| $V_n$ | Output noise (RMS), 10Hz to 100KHz | $C_{OUT}$ = 1µF | $T_J$ = 25°C | | 265 | | $µV_{rms}$ |
| PSRR | Power supply ripple rejection | $V_{IN}$ - $V_{OUT}$ = 1V, frequency = 100Hz, $I_{OUT}$ = 5mA | $T_J$ = 25°C | | 80 | | dB |
| $V_{PG(OL)}$ | PG pin low level output voltage | $V_{IN}$ ≥ 2V, $I_{OL}$ = 400µA | $T_J$ = 25°C | | 180 | 230 | mV |
| | | | $T_J$ = –40°C to 150°C | | | 280 | |
| $V_{PG(TH,RISING)}$ | $V_{OUT}$ rising | | $T_J$ = –40°C to 150°C | | | 97 | $%V_{OUT}$ |
| $V_{PG(TH,FALLING)}$ | $V_{OUT}$ falling | | | 92 | | | |
| $V_{PG(HYST)}$ | Hysteresis | | $T_J$ = 25°C | | 2 | | |
| $I_{SHUTDOWN}$ | Shutdown supply current ($I_{GND}$) | $V_{EN}$ ≤ 0.7V, $V_{IN}$ ≤ 40V, $V_{OUT}$ = 0V | $T_J$ = 25°C | | 3 | 4.5 | µA |
| | | | $T_J$ = –40°C to 150°C | | | 6 | |
| $T_{SD(SHUTDOWN)}$ | Junction shutdown temperature | | | | 177 | | °C |
| $T_{SD(HYST)}$ | Hysteresis of thermal shutdown | | | | 15 | | °C |

## 5.6 Timing Requirements

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{PGDH}$ | PG delay time rising, time from 92% $V_{OUT}$ to 20% of PG(1) | 25 | 50 | 65 | µs |
| $t_{PGDL}$ | PG delay time falling, time from 90% $V_{OUT}$ to 80% of PG(1) | 6 | 13 | 18 | µs |

(1) Output Overdrive = 10%


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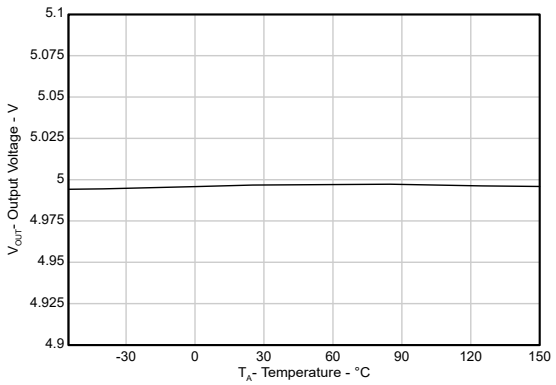
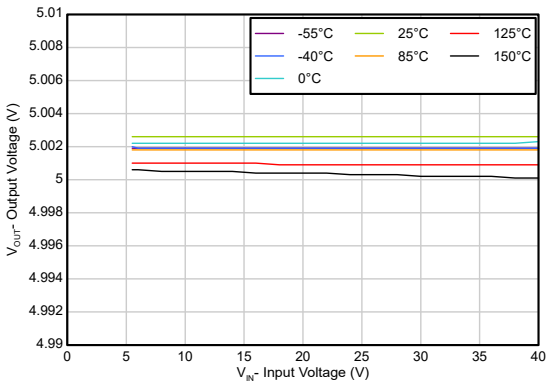
## 5.7 Typical Characteristics

at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, and $V_{EN}$ ≥ 2V (unless otherwise noted)



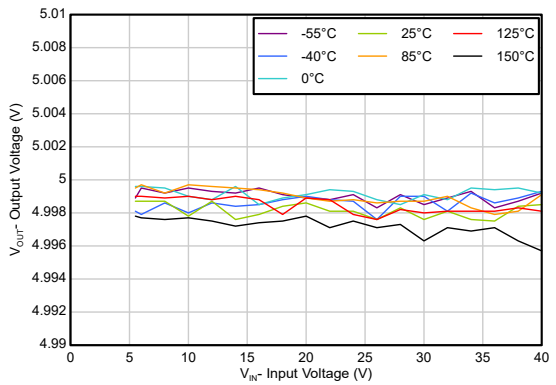

$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 150mA

**Figure 5-1. Output Voltage vs Temperature**



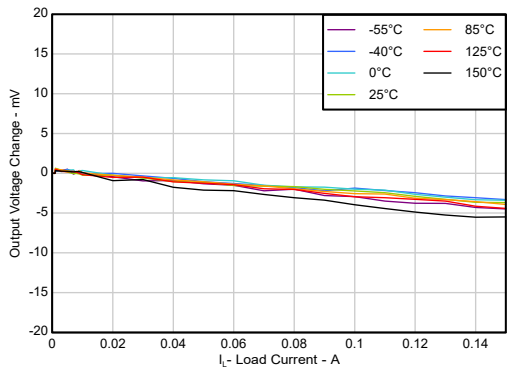

$V_{OUT}$ = 5V, $I_{OUT}$ = 100µA

**Figure 5-2. Line Regulation vs Input Voltage**



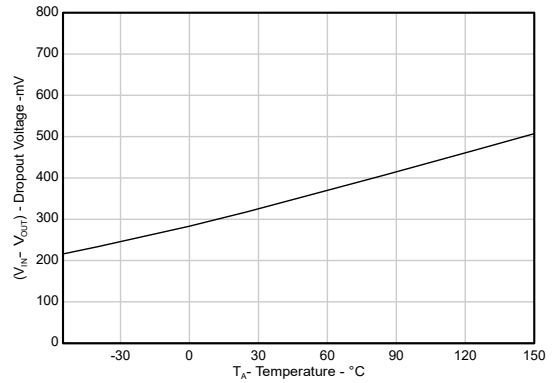

$V_{OUT}$ = 5V, $I_{OUT}$ = 150mA

**Figure 5-3. Line Regulation vs Input Voltage**



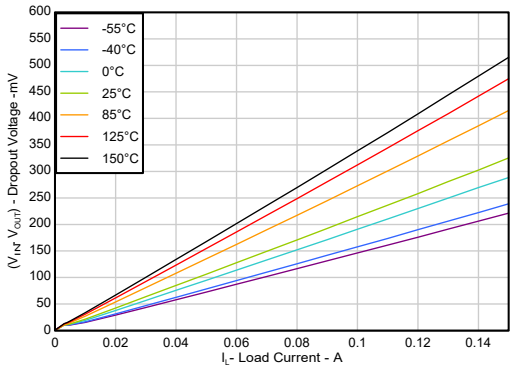

$V_{IN}$ = 6V, $V_{OUT}$ = 5V

**Figure 5-4. Load Regulation vs Load Current**




$V_{IN}$ = 4.9V, $I_{OUT}$ = 150mA

**Figure 5-5. Dropout Voltage vs Temperature**




$V_{IN}$ = 4.9V

**Figure 5-6. Dropout Voltage vs Output Current**

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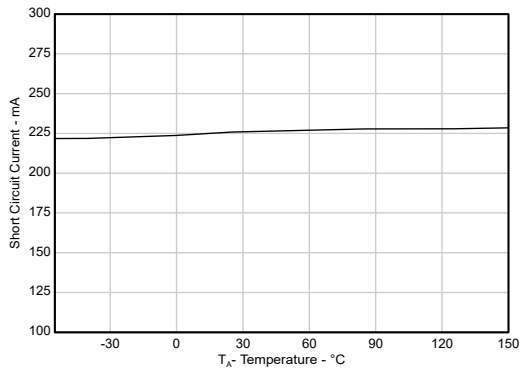
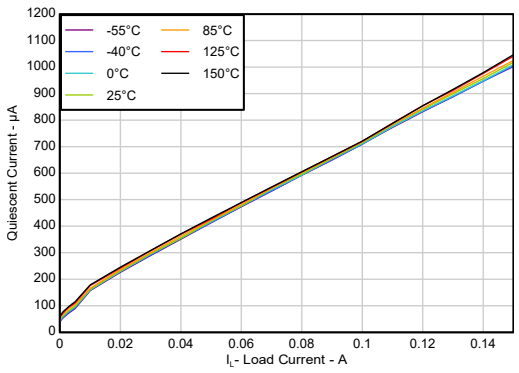
## 5.7 Typical Characteristics (continued)

at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, and $V_{EN}$ ≥ 2V (unless otherwise noted)



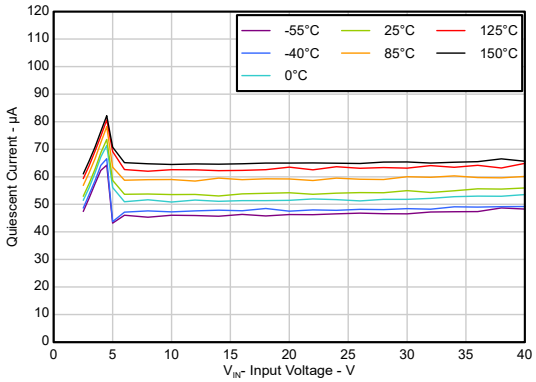

$V_{IN}$ = 6V, $V_{OUT}$ = 0V

**Figure 5-7. Short-Circuit Current vs Temperature**



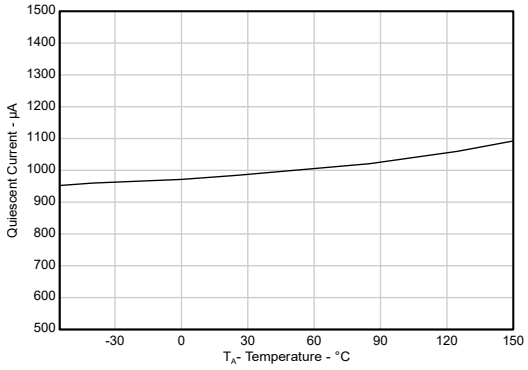

$V_{IN}$ = 6V, $V_{OUT}$ = 5V

**Figure 5-8. Quiescent Current vs Load Current**



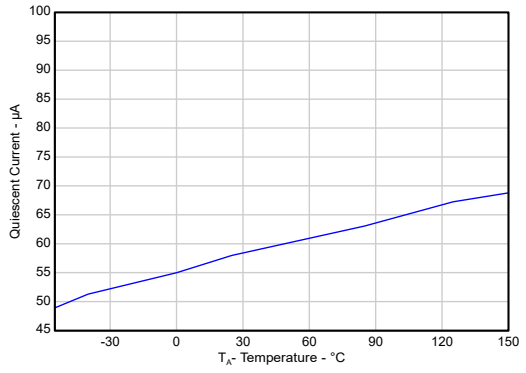

$V_{OUT}$ = 5V

**Figure 5-9. Quiescent Current vs Input Voltage ($I_{OUT}$ = 0mA)**




$V_{IN}$ = 6V, $V_{OUT}$ = 5V

**Figure 5-10. Quiescent Current vs Temperature ($I_{OUT}$ = 150mA)**




$V_{IN}$ = 6V, $V_{OUT}$ = 5V

**Figure 5-11. Quiescent Current vs Temperature ($I_{OUT}$ = 100µA)**

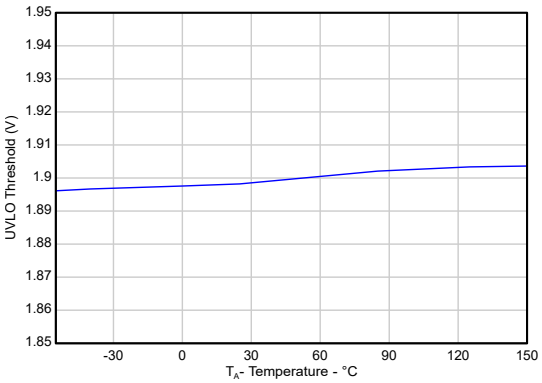



**Figure 5-12. Undervoltage Lockout (UVLO) Threshold vs Temperature**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## 5.7 Typical Characteristics (continued)

at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, and $V_{EN}$ ≥ 2V (unless otherwise noted)

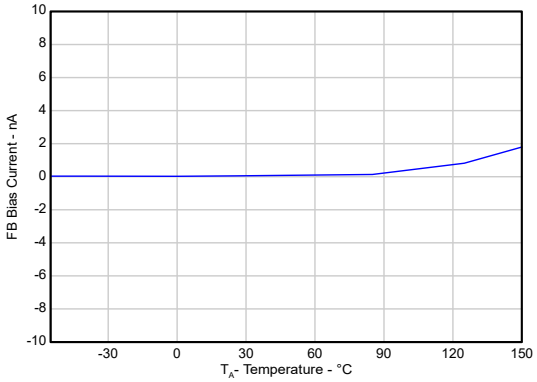



**Figure 5-13. FB Bias Current vs Temperature**

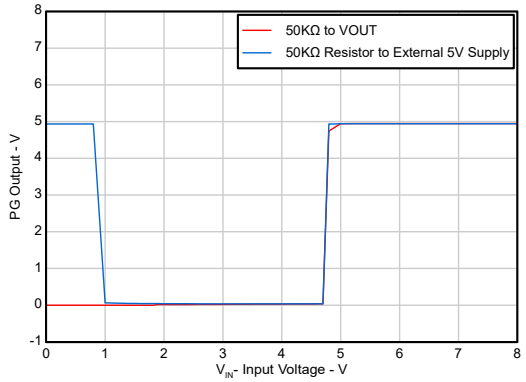



**Figure 5-14. PG Comparator Output vs Input Voltage**

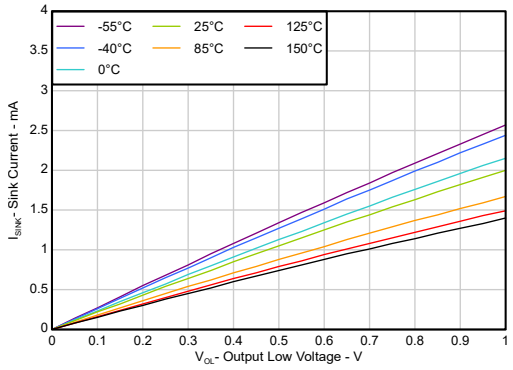



**Figure 5-15. PG Comparator Sink Current vs Output Low Voltage**

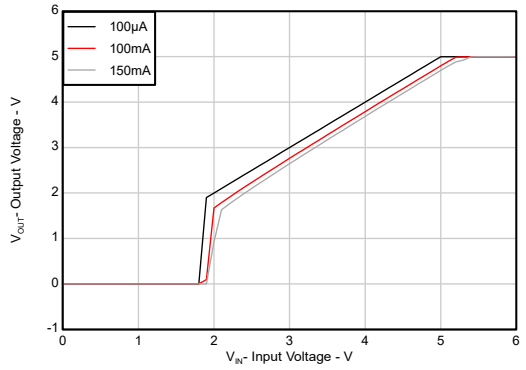
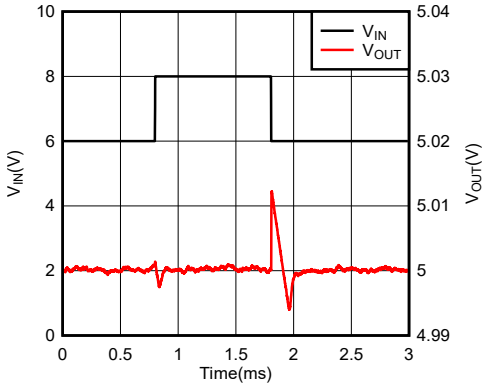
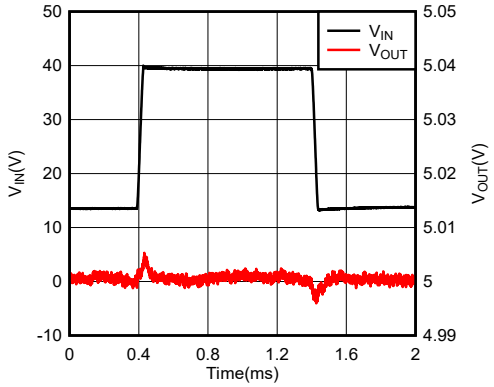



**Figure 5-16. Output Voltage vs Input Voltage**




$V_{IN}$ = 6V to 8V, slew rate = 1V/µs, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF, $I_{OUT}$ = 100µA

**Figure 5-17. Line Transient Response vs Time**




$V_{IN}$ = 13.5V to 40V, slew rate = 1V/µs, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF, $I_{OUT}$ = 1mA

**Figure 5-18. Line Transient Response vs Time**

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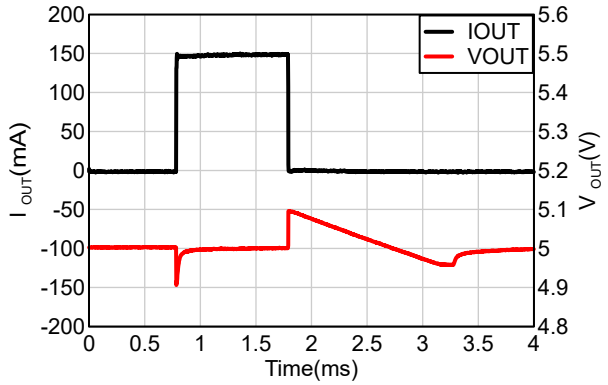
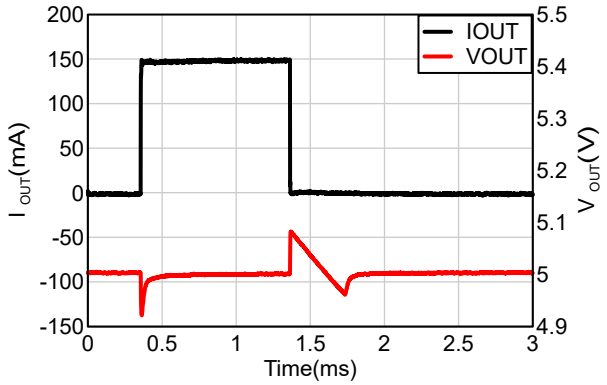
## 5.7 Typical Characteristics (continued)

at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, and $V_{EN}$ ≥ 2V (unless otherwise noted)



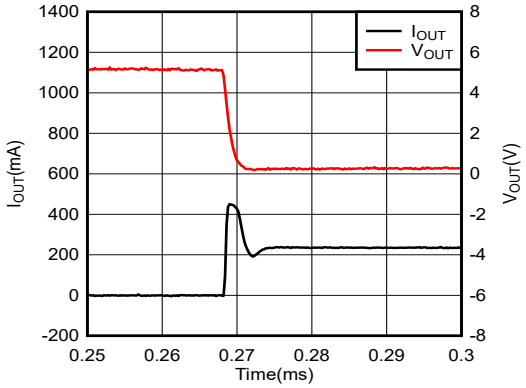

$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0mA to 150mA, slew rate = 1A/µs, $C_{OUT}$ = 1µF

**Figure 5-19. Load Transient Response vs Time**



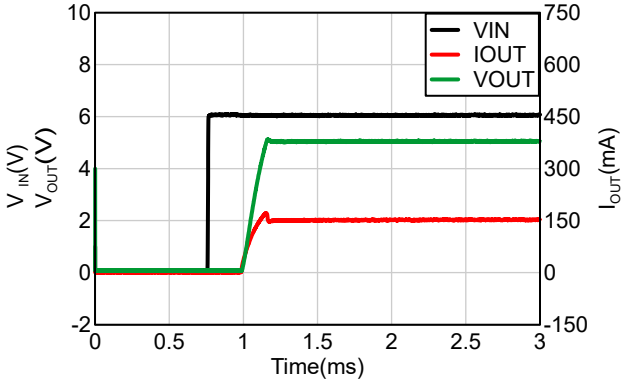

$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0mA to 150mA, slew rate = 1A/µs, $C_{OUT}$ = 10µF

**Figure 5-20. Load Transient Response vs Time**



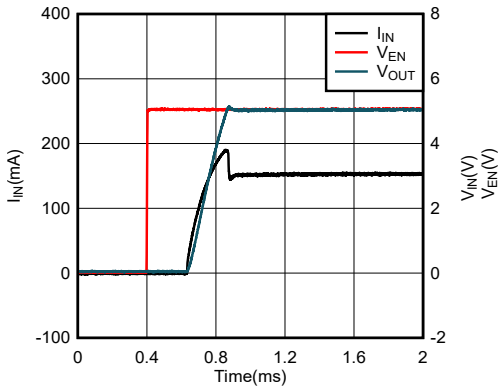

$V_{IN}$ = 6V, $C_{OUT}$ = 1µF

**Figure 5-21. Short-Circuit Current vs Time**



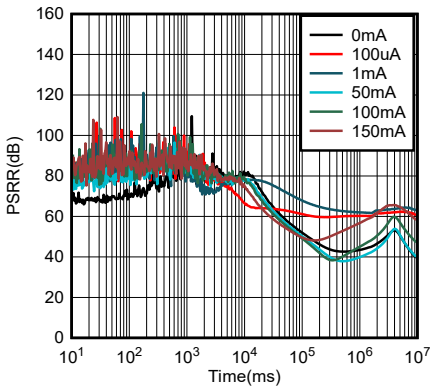

$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF, $R_L$ = 33.3Ω

**Figure 5-22. Power-Up Waveform**




$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF, $R_L$ = 33.3Ω

**Figure 5-23. Startup Plot With EN**




$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF

**Figure 5-24. Ripple Rejection vs Frequency**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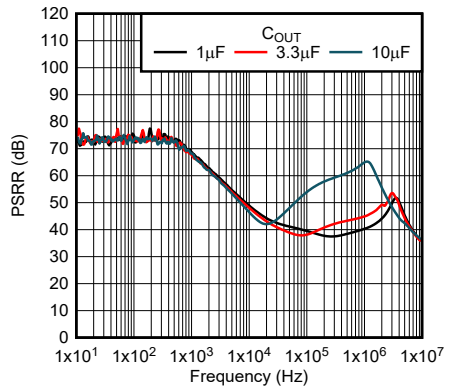
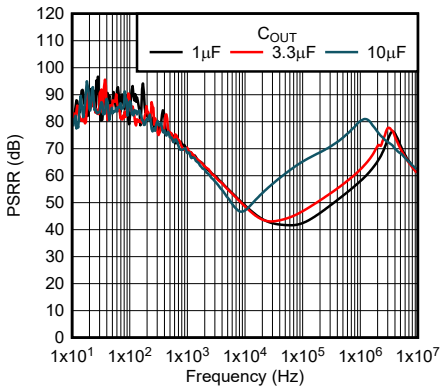
## 5.7 Typical Characteristics (continued)

at $V_{IN}$ = $V_{OUT}$ (nominal) + 1V, $I_{OUT}$ = 100µA, $C_{OUT}$ = 2.2µF, and $V_{EN}$ ≥ 2V (unless otherwise noted)



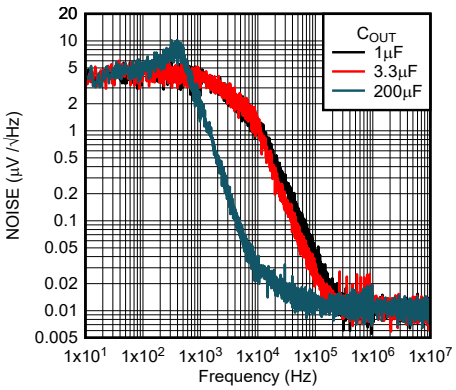

$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 100mA

**Figure 5-25. Ripple Rejection vs Frequency**



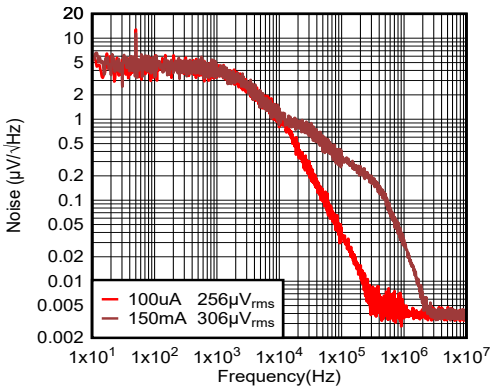

$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 1mA

**Figure 5-26. Ripple Rejection vs Frequency**




$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 100µA

**Figure 5-27. Output Noise vs Frequency**




$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF

**Figure 5-28. Output Noise vs Frequency**

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# 6 Detailed Description

## 6.1 Overview

The TPS7C84-Q1 is a low-dropout linear regulator (LDO) designed to connect to the battery in automotive applications. The device accommodates a wide input supply voltage range up to 40V. The TPS7C84-Q1 is available in 3.3V and 5V fixed output voltages. Alternatively, by connecting the FB pin to an external resistor divider, the output is able to be set to any value between 1.2V to 39V.

The TPS7C84-Q1 has a power-good output (PG) that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output are used for sequencing multiple power supplies in the system. The TPS7C84-Q1 is stable with small ceramic output capacitors, allowing for a small overall solution size. This device has an output tolerance of 1% across line, load, and temperature variation and is capable of delivering 150mA of continuous load current. This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. This device delivers excellent line and load transient performance. The operating junction temperature range of the device is from –40°C to +150°C.

## 6.2 Functional Block Diagrams

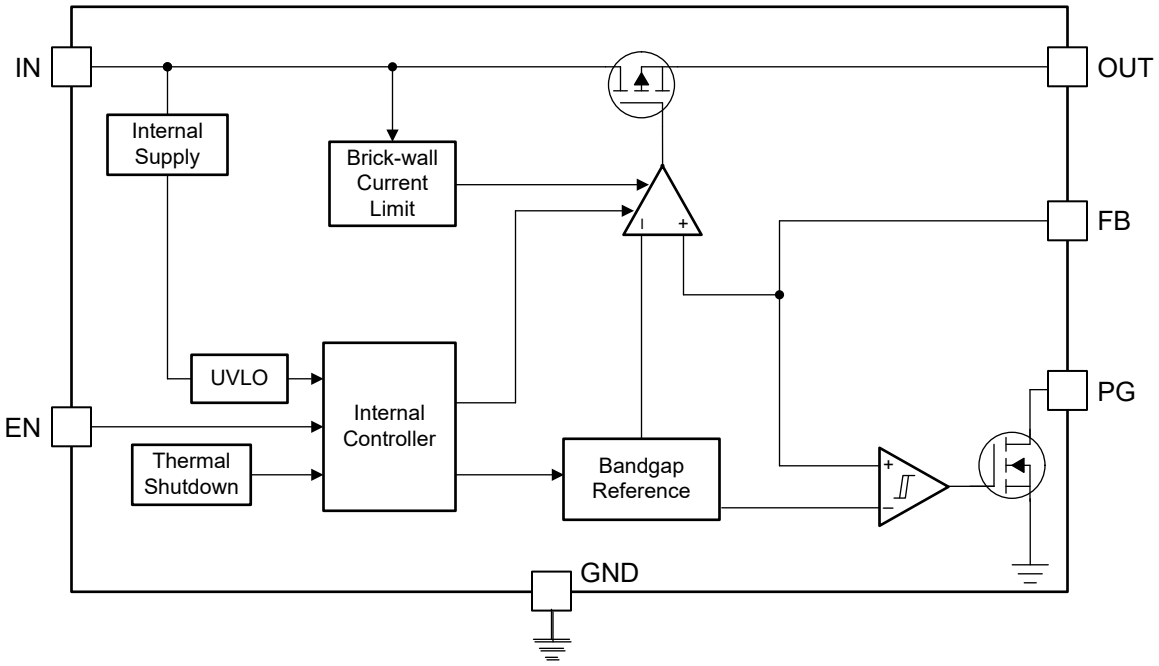


**Figure 6-1. Adjustable Output Block Diagram**


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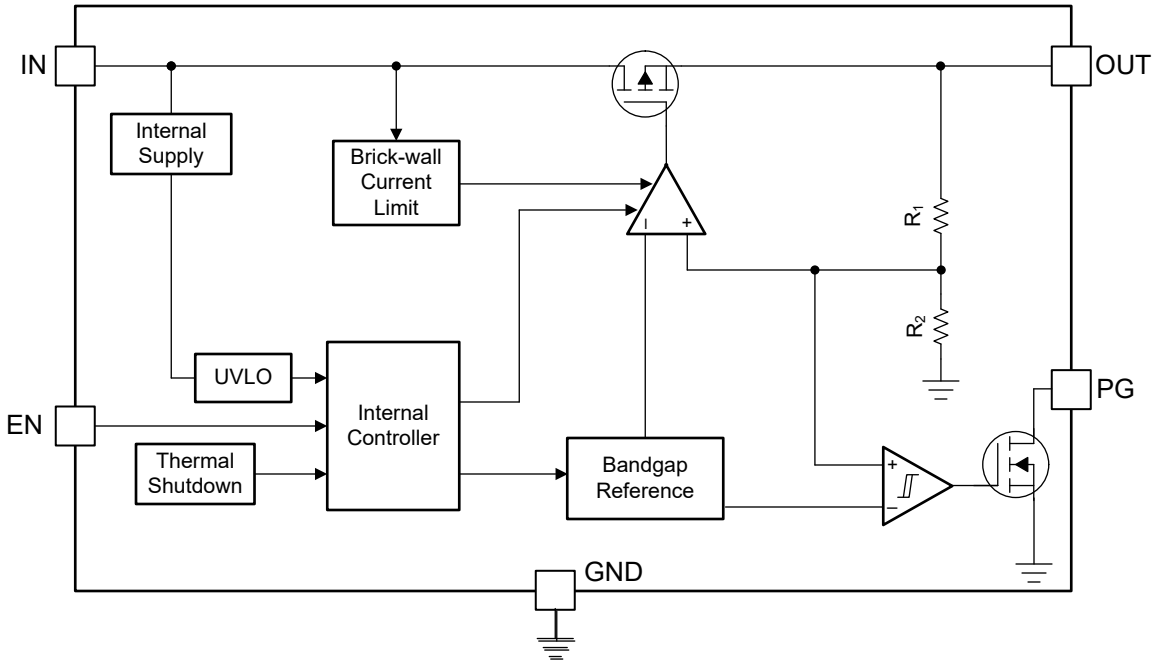


**Figure 6-2. Fixed Output Block Diagram**

## 6.3 Feature Description

### *6.3.1 Output Enable*

The EN pin for the device is an active-high pin. The output voltage is enabled when the EN pin voltage is greater than the high-level input voltage of the EN pin. Conversely, the output voltage is disabled when the EN pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the EN pin to the device input voltage.

### *6.3.2 Dropout Voltage*

Dropout voltage ($V_{DO}$) is defined as $V_{IN} – V_{OUT}$ at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, and $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### *6.3.3 Current Limit*

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). $I_{CL}$ is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the

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output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-3 shows a diagram of the current limit.

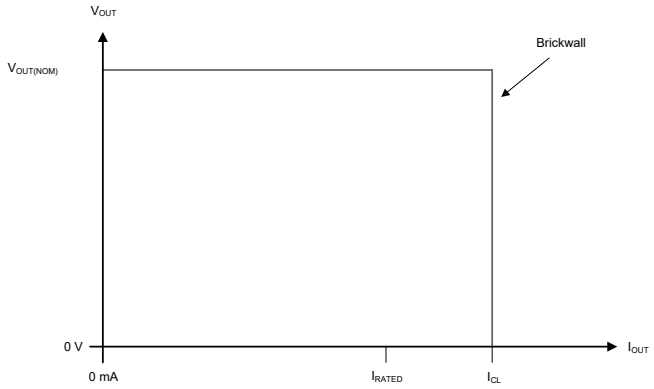


**Figure 6-3. Current Limit**

### 6.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. This circuit allows for a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 6.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

## 6.4 Device Functional Modes

### 6.4.1 Shutdown Mode

Place this device in shutdown mode with a logic low at the EN pin. Return the logic level high to restore operation or tie EN to $V_{IN}$ if this mode is not used.


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# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

### *7.1.1 Reverse Current*

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

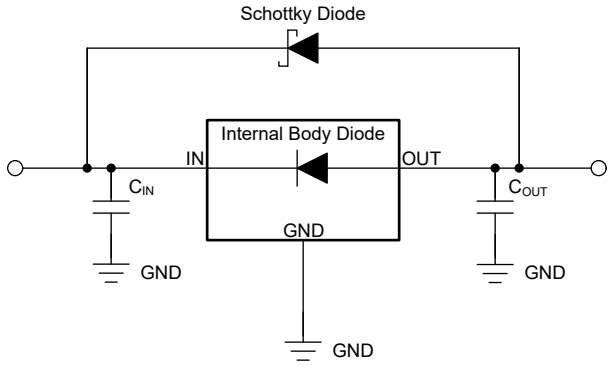


**Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### *7.1.2 Input and Output Capacitor Requirements*

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

### *7.1.3 Estimating Junction Temperature*

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are

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determined to be significantly independent of the copper area available for heat-spreading. The Section 5.4 table lists the primary thermal metrics, which are the junction-to-top characterization parameter ($\psi_{JT}$) and junction-to-board characterization parameter ($\psi_{JB}$). These parameters provide two methods for calculating the junction temperature ($T_J$), as described in the following equations. Use the junction-to-top characterization parameter ($\psi_{JT}$) with the temperature at the center-top of device package ($T_T$) to calculate the junction temperature. Use the junction-to-board characterization parameter ($\psi_{JB}$) with the printed circuit board (PCB) surface temperature 1mm from the device package ($T_B$) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \quad (2)$$

where:

- $P_D$ is the dissipated power
- $T_T$ is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \quad (3)$$

where:

- $T_B$ is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

### 7.1.4 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the PCB, and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation ($P_D$).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

**Note**

Power dissipation is minimized, and therefore greater efficiency achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the $T_A$. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and $T_A$ is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A = \left(R_{\theta JA} \times P_D\right) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Section 5.4* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance.


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## 7.2 Typical Application

Figure 7-2 shows a typical application circuit for the TPS7C84-Q1. Use different values of external components, depending on the end application. If needed, use a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low-ESR ceramic capacitor with an X5R or X7R dielectric.

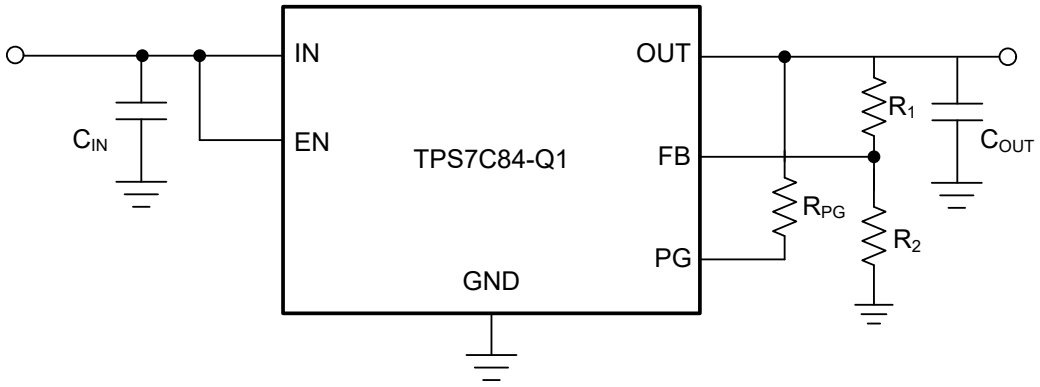


**Figure 7-2. Typical Application Schematic for the TPS7C84-Q1**

### *7.2.1 Design Requirements*

Table 7-1 summarizes the design requirements for Figure 7-2.

**Table 7-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage range | 6V to 40V |
| Output voltage | 5V |
| Output current | 150mA |
| Output capacitor | 1µF |

#### 7.2.1.1 Recommended Capacitor Types

##### *7.2.1.1.1 Recommended Capacitors*

The TPS7C84-Q1 requires an output capacitor of at least 1µF for stability and an equivalent series resistance (ESR) between 0Ω and 2Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 100µF. An input capacitor is not required for stability. However, good analog practice is to connect a capacitor (500nF or higher) between the GND and IN pins. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

### *7.2.2 Detailed Design Procedure*

#### 7.2.2.1 Feedback Resistor Selection

$V_{OUT}$ is set by the external feedback resistors $R_1$ and $R_2$, according to the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (6)$$

To ignore the FB pin current error in the $V_{OUT}$ equation, set the feedback divider current to 100 times the FB pin current ($I_{FB}$) listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq \frac{V_{OUT}}{(I_{FB} \times 100)} \quad (7)$$

#### 7.2.2.2 Feedforward Capacitor

Connect a feedforward capacitor ($C_{FF}$) between the OUT pin and the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance. If a higher capacitance $C_{FF}$ is used, the start-up time increases. For a detailed description of the $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

As shown in Figure 7-3, poor layout practices and using long traces at the FB pin results in the formation of a parasitic capacitor ($C_{FB}$).

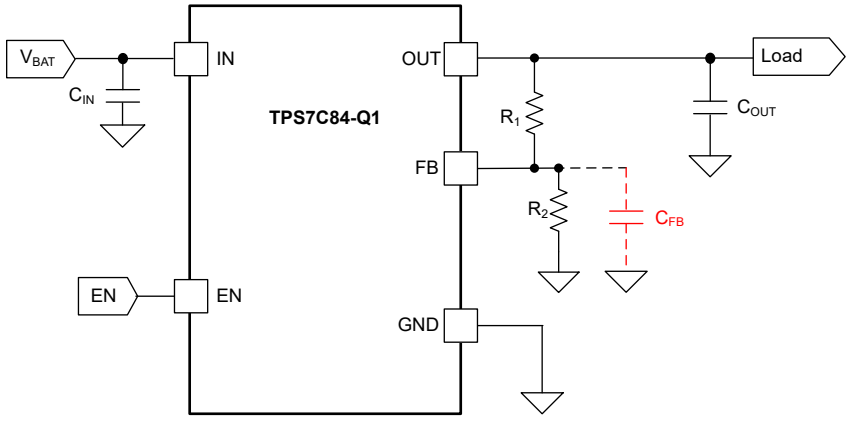


**Figure 7-3. Formation of a Parasitic Capacitor at the FB Pin**

$C_{FB}$, along with the feedback resistors $R_1$ and $R_2$ potentially results in the formation of an uncompensated pole in the transfer function of the loop gain. A $C_{FB}$ value as small as 6pF potentially causes the parasitic pole frequency, given by Equation 8, to fall within the LDO bandwidth and result in instability.

$$f_P = \frac{1}{(2 \times \pi \times C_{FB} \times (R_1 \parallel R_2))} \quad (8)$$

Adding a feedforward capacitor ($C_{FF}$) creates a zero in the loop gain transfer function that compensates for the parasitic pole created by $C_{FB}$. Figure 7-4 shows this compensation. Equation 9 and Equation 10 calculate the pole and zero frequencies.


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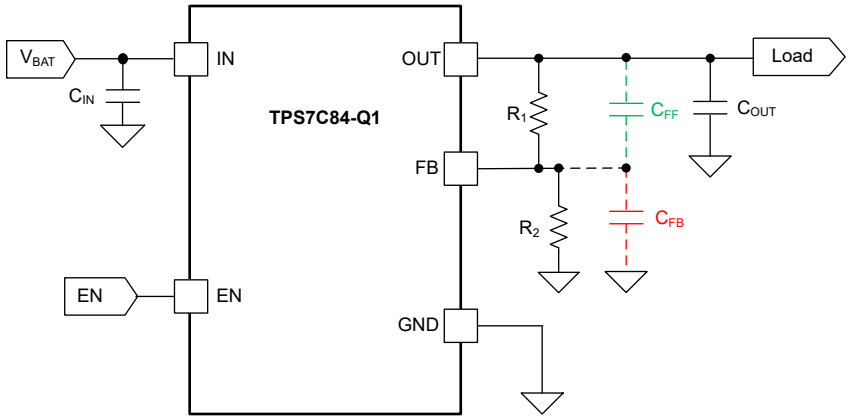



**Figure 7-4. A Feedforward Capacitor Compensates the Effects of the Parasitic Capacitor**

$$f_P = \frac{1}{(2 \times \pi \times (R_1 \parallel R_2) \times (C_{FF} + C_{FB}))} \quad (9)$$

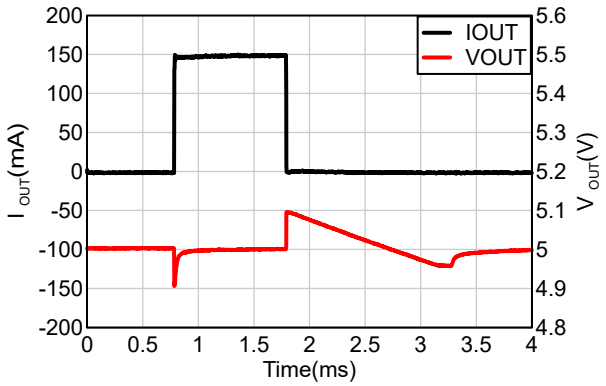
$$f_Z = \frac{1}{(2 \times \pi \times C_{FF} \times R_1)} \quad (10)$$

The $C_{FF}$ value that makes $f_P$ equal to $f_Z$ depends on the values of $C_{FB}$ and the feedback resistors used in the application. This $C_{FF}$ value also results in a pole-zero cancellation. Alternatively, if the feedforward capacitor is selected so that $C_{FF} \gg C_{FB}$, then the pole and zero frequencies from Equation 9 and Equation 10 are related as:

$$\frac{f_p}{f_z} \cong \left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT}}{V_{FB}} \quad (11)$$

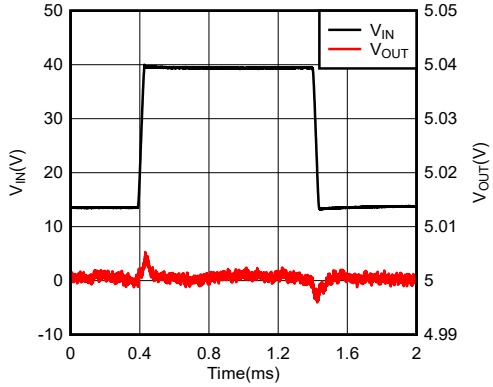
In most applications, particularly where a 3.3V or 5V $V_{OUT}$ is generated, this ratio is not very large. Thus implying that the frequencies are located close to each other and therefore the parasitic pole is compensated. A $C_{FF}$ value of approximately 100pF ≤ $C_{FF}$ ≤ 10nF typically helps prevent instability caused by the parasitic capacitance on the feedback node. This $C_{FF}$ range helps even for large $V_{OUT}$ values, where this ratio is potentially as large as 20.

### 7.2.3 Application Curves




$V_{IN}$ = 6V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0mA to 150mA, slew rate = 1A/µs, $C_{OUT}$ = 1µF

**Figure 7-5. Load Transient Response vs Time**




$V_{IN}$ = 13.5V to 40V, slew rate = 1V/µs, $V_{OUT}$ = 5V, $C_{OUT}$ = 1µF, $I_{OUT}$ = 1mA

**Figure 7-6. Line Transient Response vs Time**

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## 7.3 Power Supply Recommendations

Limit maximum input voltage to 40V for proper operation. Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

- Verify that the traces on the input and outputs of the device are wide enough to handle the desired currents. For this device, use a larger output trace to accommodate the larger available current.
- Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

### *7.4.2 Layout Example*

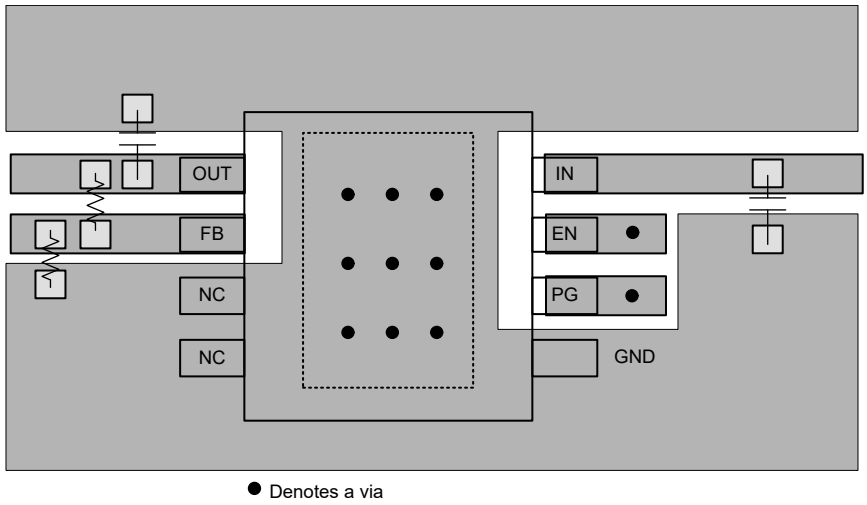


**Figure 7-7. SOIC (D) Package Adjustable Output**


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# 8 Device and Documentation Support

## 8.1 Device Support

### 8.1.1 Device Nomenclature

**Table 8-1. Device Nomenclature**

| PRODUCT[1] | $V_{OUT}$ |
|---|---|
| TPS7C84**xx**Q ***(W) yyyz***Q1 | **xx** is the nominal output voltage (for example, 50 = 5.0V, 33 = 3.3V).<br>**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard.<br>**W** indicates the package has wettable flanks.<br>**yyy** is the package designator.<br>**z** is the reel quantity.<br>**Q1** indicates that this device is an automotive grade (AEC-Q100) device. |
| TPS7C84**01**Q ***(W) yyyz***Q1 | **01** indicates that this device is the adjustable option.<br>**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard<br>**W** indicates the package has wettable flanks.<br>**yyy** is the package designator.<br>**z** is the reel quantity.<br>**Q1** indicates that this device is an automotive grade (AEC-Q100) device. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## 8.2 Documentation Support

### 8.2.1 Related Documentation

- Texas Instruments, *TPS7C84-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.5 Trademarks

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## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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| Changes from Revision C (November 2025) to Revision D (March 2026) | Page |
|---|---|
| • Changed from *Production Mix* to *Production Data* | 1 |

| Changes from Revision B (February 2025) to Revision C (November 2025) | Page |
|---|---|
| • Changed from *Production Data* to *Production Mix* | 1 |
| • Removed "TEST" from IN pin description | 3 |
| • Added DRB (VSON-8) with wettable flanks data to the *Thermal Information* table | 4 |
| • Updated wording of how to manage the I_FB error term for clarity | 17 |
| • Updated Device Nomenclature table to include "W" for package variants with wettable flanks | 21 |
| • Added the *Documentation Support* and *Related Documentation* sections | 21 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7C8401QDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C8401D |
| TPS7C8401QDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C8401D |
| TPS7C8401QWDRBRQ1 | Active | Production | SON (DRB) \| 8 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7C8401 |
| TPS7C8433QDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C8433D |
| TPS7C8433QDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C8433D |
| TPS7C8433QWDRBRQ1 | Active | Production | SON (DRB) \| 8 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7C8433 |
| TPS7C8450QDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C8450D |
| TPS7C8450QDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C8450D |
| TPS7C8450QWDRBRQ1 | Active | Production | SON (DRB) \| 8 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7C8450 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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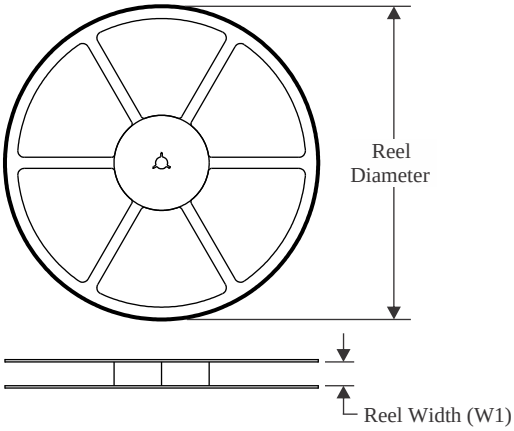
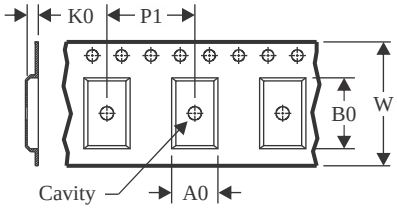
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

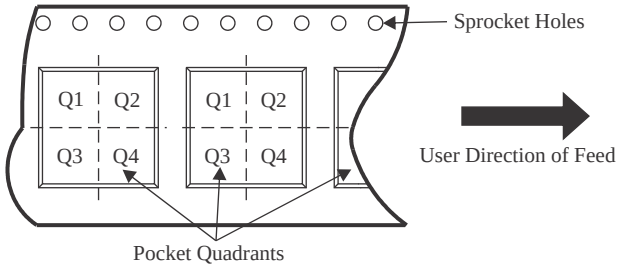



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

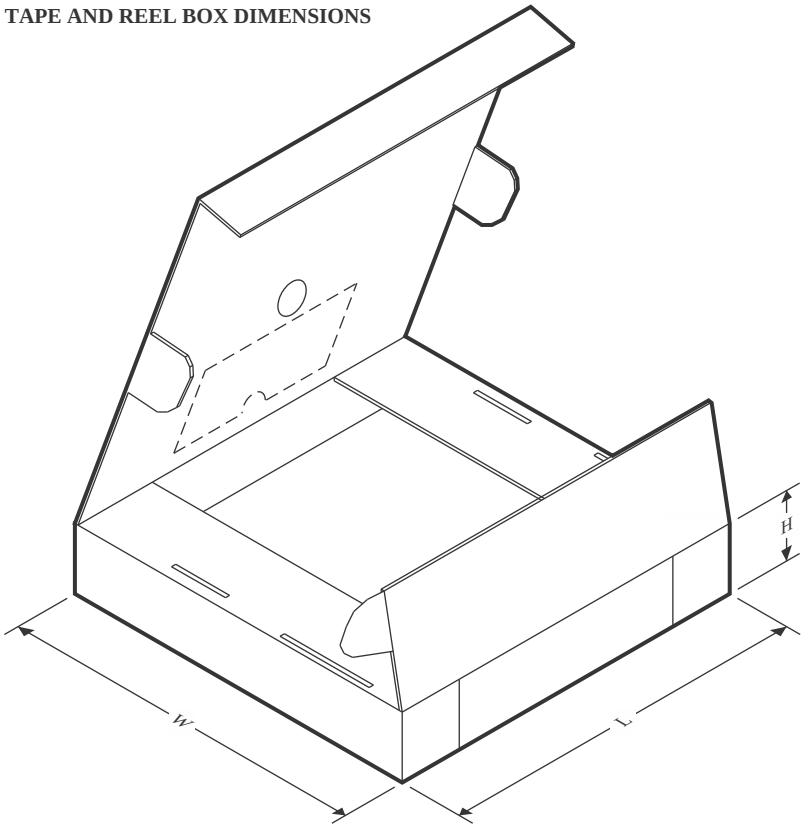
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7C8401QDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7C8401QWDRBRQ1 | SON | DRB | 8 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7C8433QDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7C8433QWDRBRQ1 | SON | DRB | 8 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7C8450QDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7C8450QWDRBRQ1 | SON | DRB | 8 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7C8401QDRQ1 | SOIC | D | 8 | 3000 | 340.5 | 338.1 | 20.6 |
| TPS7C8401QWDRBRQ1 | SON | DRB | 8 | 5000 | 360.0 | 360.0 | 36.0 |
| TPS7C8433QDRQ1 | SOIC | D | 8 | 3000 | 340.5 | 338.1 | 20.6 |
| TPS7C8433QWDRBRQ1 | SON | DRB | 8 | 5000 | 360.0 | 360.0 | 36.0 |
| TPS7C8450QDRQ1 | SOIC | D | 8 | 3000 | 340.5 | 338.1 | 20.6 |
| TPS7C8450QWDRBRQ1 | SON | DRB | 8 | 5000 | 360.0 | 360.0 | 36.0 |

## GENERIC PACKAGE VIEW

# DRB 8

# VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

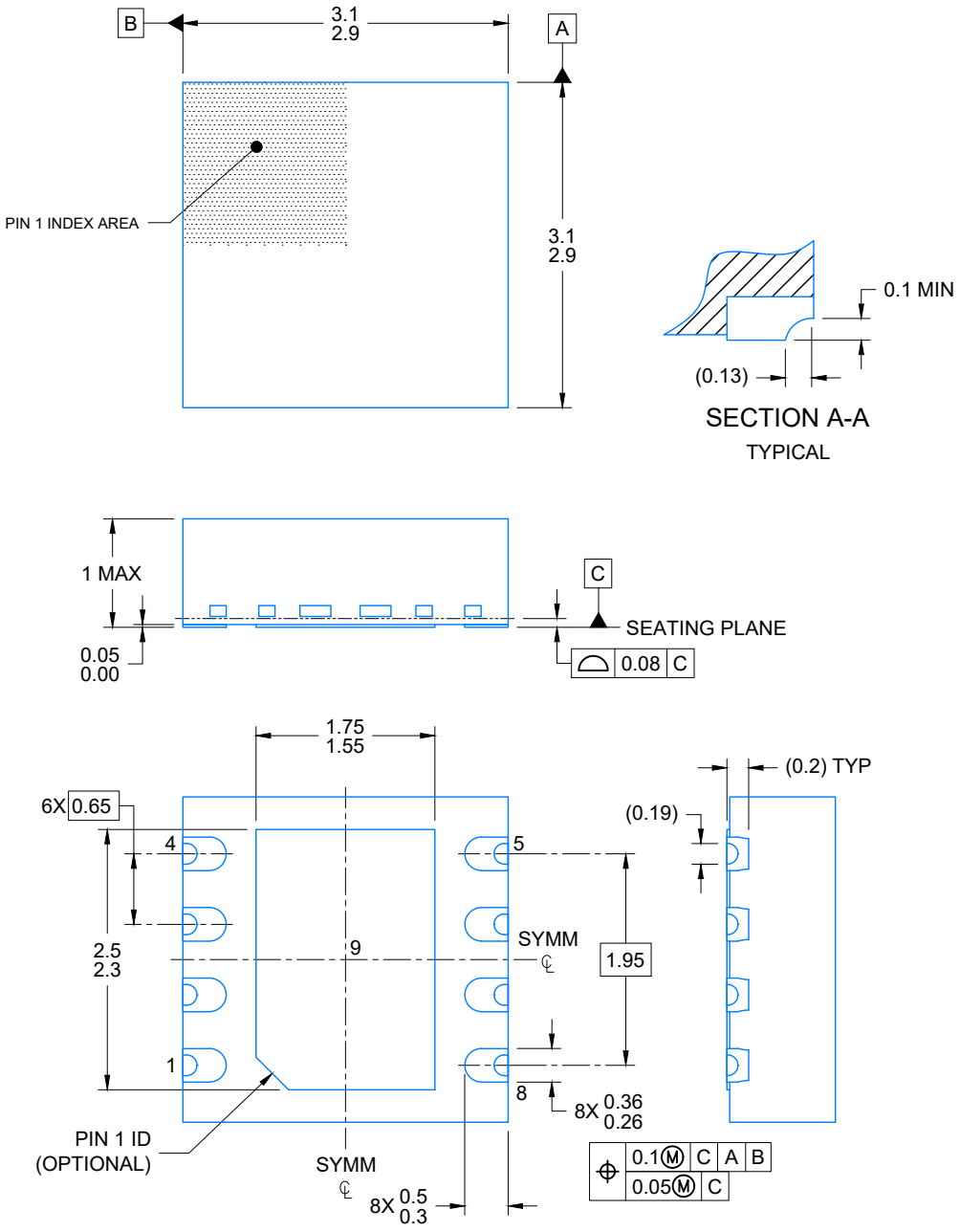
4203482/L

# PACKAGE OUTLINE

## DRB0008J

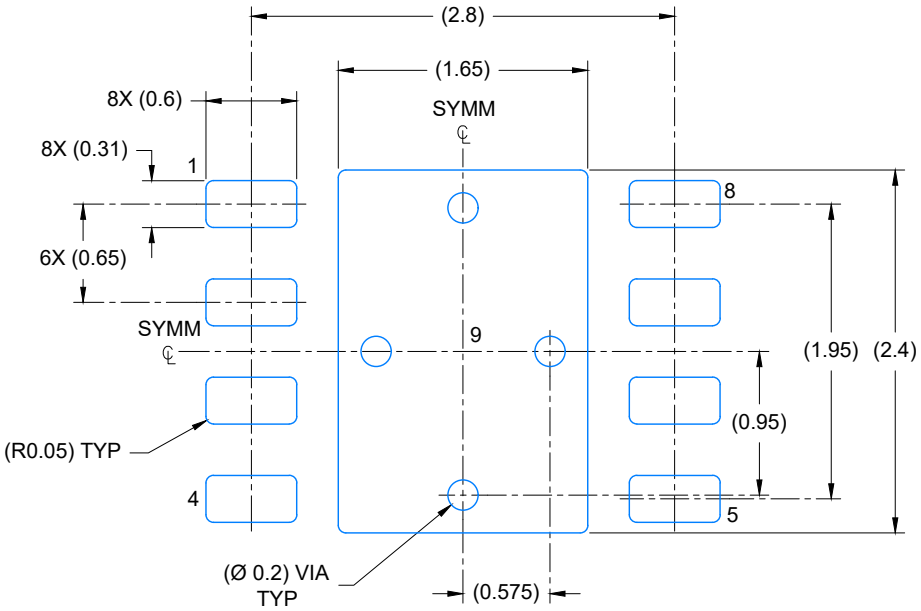
## VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

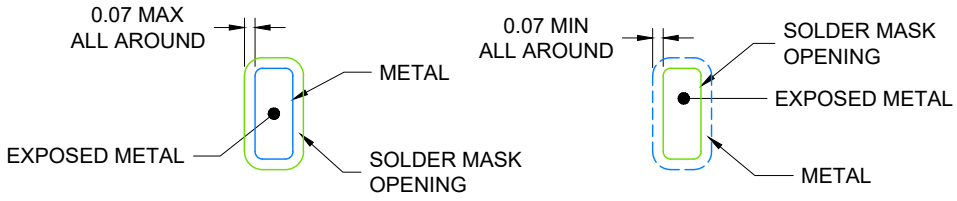



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




NON- SOLDER MASK
DEFINED
(PREFERRED)

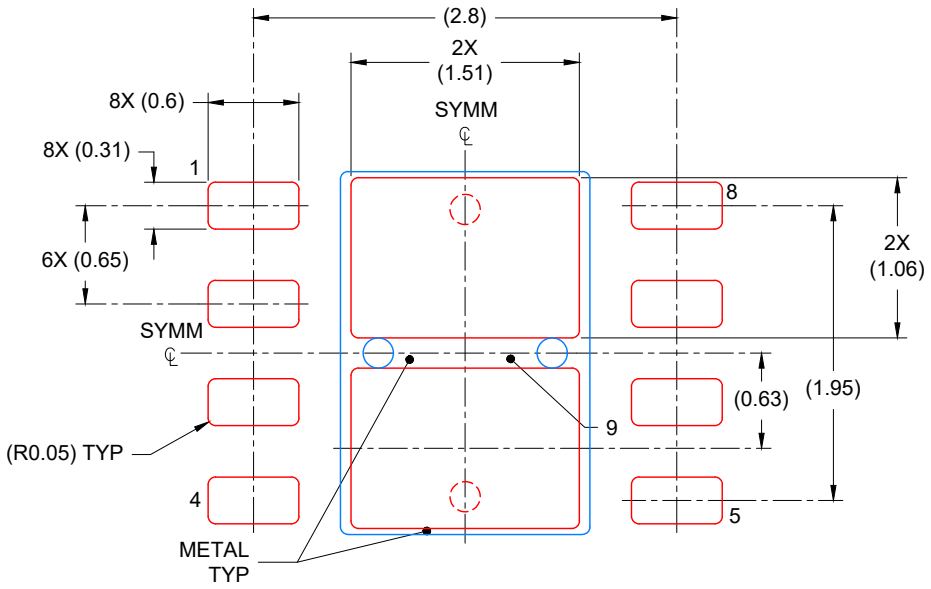
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



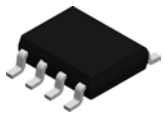

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

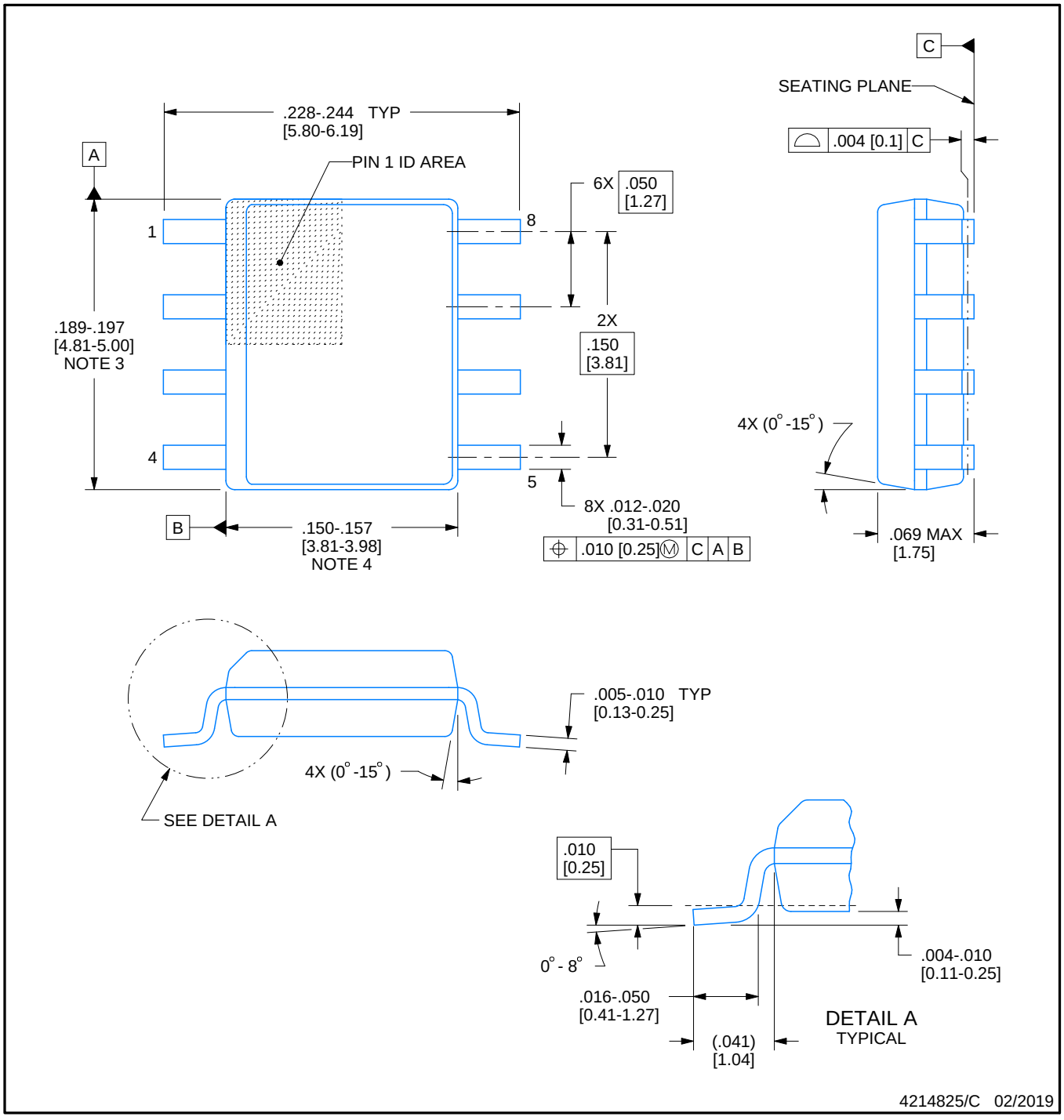


# PACKAGE OUTLINE

## D0008A

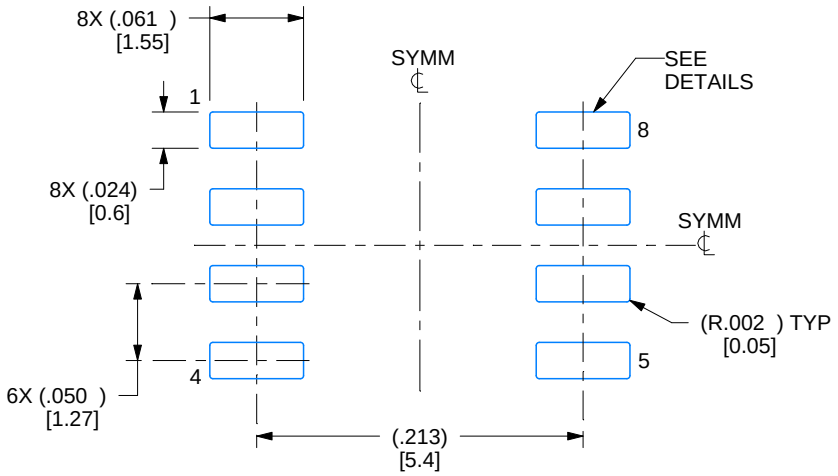
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

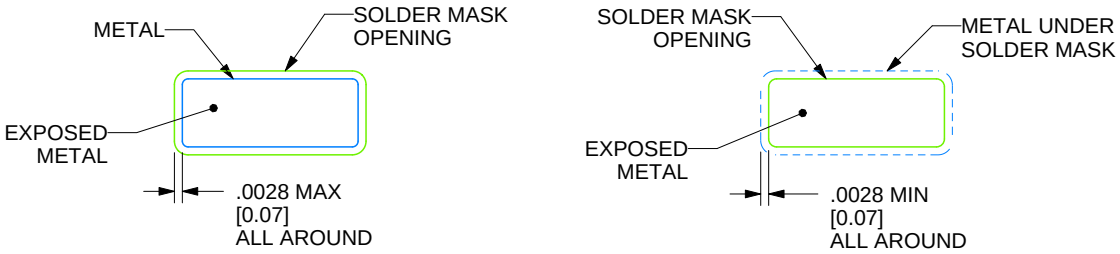



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

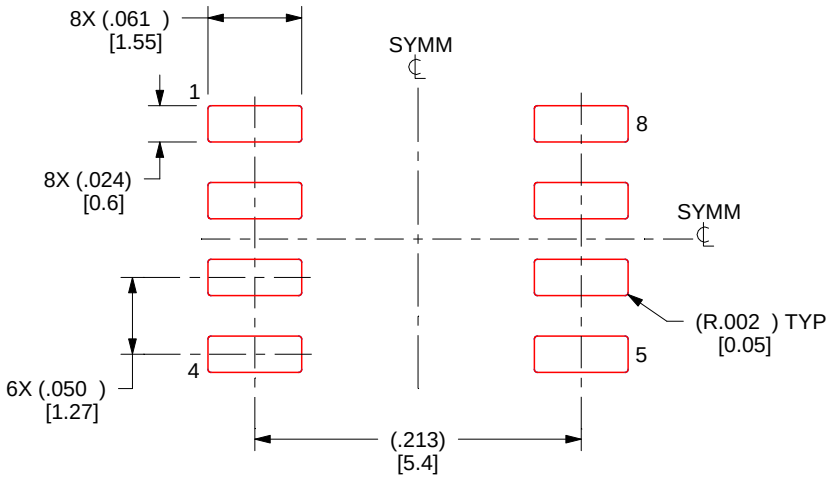
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025

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